

Ordering Information

Extended Type Number	Package	Remarks
U2008B-A	DIP8	
U2008B-AFP	SO8	
U2008B-AFPG3	SO8	Taped and reeled

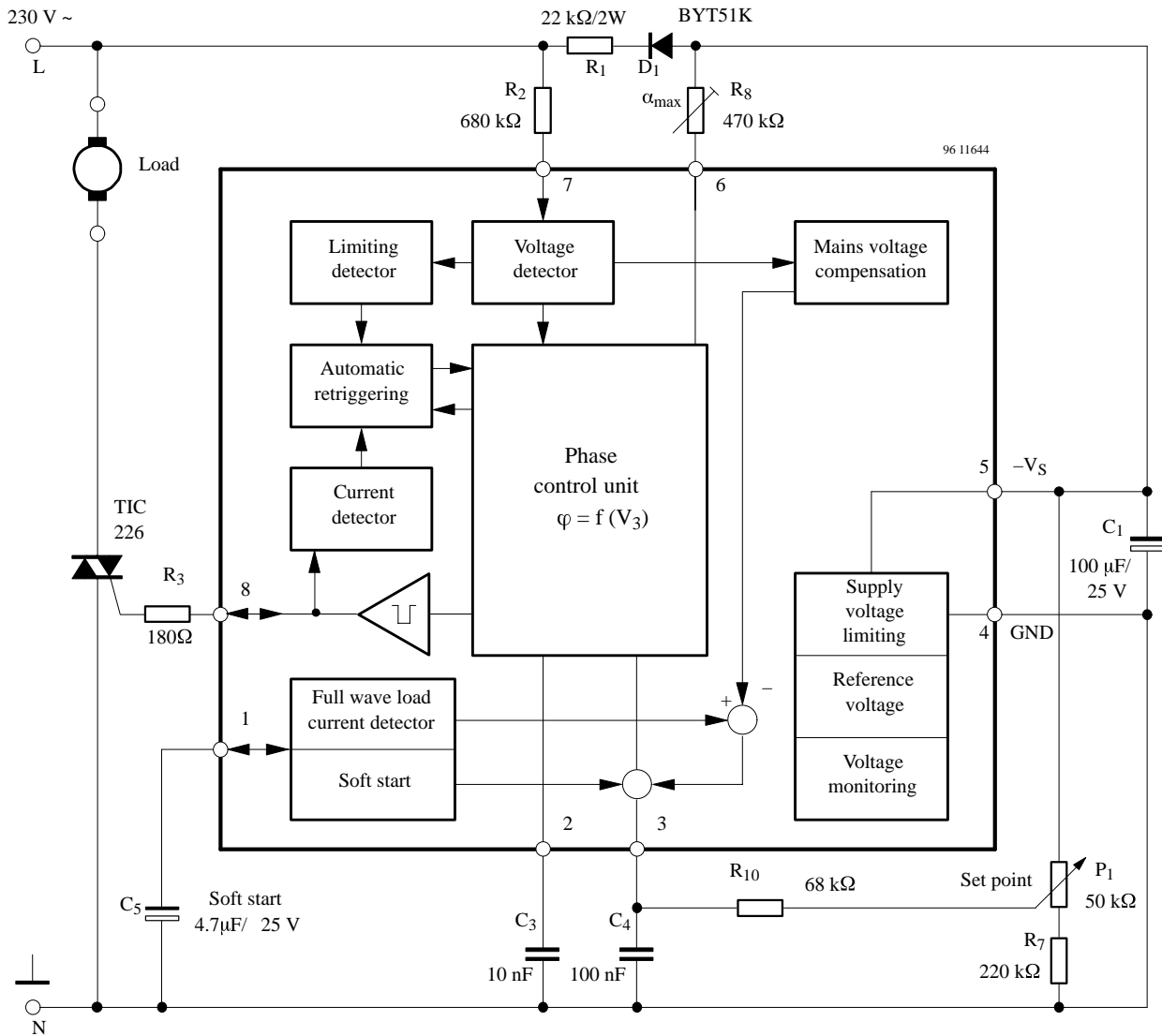


Figure 2. Block diagram with typical circuit: Soft start

Pin Description

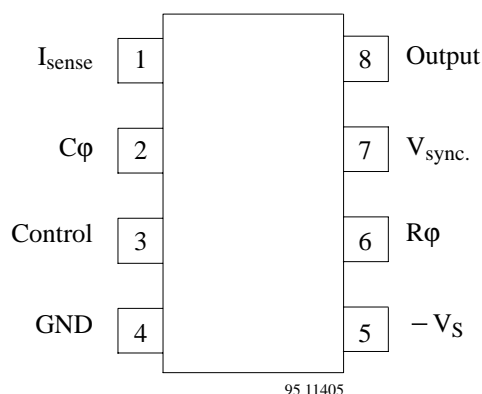


Figure 3. Pinning

Pin	Symbol	Function
1	I_{sense}	Load current sensing
2	$C\phi$	Ramp voltage
3	Control	Control input / compensation output
4	GND	Ground
5	$-V_S$	Supply voltage
6	$R\phi$	Ramp current adjustment
7	$V_{sync.}$	Voltage synchronization
8	Output	Trigger output

Mains Supply, Pin 5, Figure 2

The integrated circuit U2008B, which also contains voltage limiting, can be connected via D_1 and R_1 via the mains supply. Supply voltage $-$ between Pin 4 (pos., \perp) and Pin 5 $-$ is smoothed by C_1 .

Series resistance R_1 can be calculated as follows:

$$R_{1max} = 0.85 \times \frac{V_M - V_{Smax}}{2 \times I_{tot}}$$

whereas

V_M = Mains voltage

V_{Smax} = Maximum supply voltage

I_{tot} = $I_{Smax} + I_x$ = Total current compensation

The appendix provides further information regarding the design (see figures 11, 12 and 13). An operation with external stabilized DC voltage is not recommended.

Voltage Monitoring

As the voltage is built up, uncontrolled output pulses are avoided by internal voltage monitoring. Apart from that all the latches in the circuit (phase control, load limit regulation) are reset and the soft-start capacitor is short circuited. This guarantees a specified start-up behavior each time the supply voltage is switched on or after short interruptions of the mains supply. Soft-start is initiated after the supply voltage has been built up. This behavior guarantees a gentle start-up for the motor and automatically ensures the optimum run-up time.

Phase Control, Pin 6

The function of the phase control is largely identical to the well known IC family TEA1007. The phase angle of the

trigger pulse is derived by comparing the ramp voltage V_2 at Pin 2 with the set value on the control input, Pin 3. The slope of the ramp is determined by C_3 and its charging current I_{ϕ} .

The charging current can be regulated, changed, altered using R_8 at Pin 6. The maximum phase angle, α_{max} , (minimum current flow angle ϕ_{min}) can also be adjusted by using R_8 (see figure 5).

When the potential on Pin 2 reaches the set point level of Pin 3, a trigger pulse is generated whose pulse width, t_p , is determined from the value of C_3 ($t_p = 9 \mu s/nF$, see figure 7). At the same time, a latch is set with the output pulse, as long as the automatic retriggering has not been activated, then no more pulses can be generated in that half cycle. Control input at Pin 3 (with respect to Pin 4) has an active range from -9 V to -2 V. When $V_3 = -9$ V, then the phase angle is at its maximum α_{max} i.e., the current flow angle is minimum. The minimum phase angle α_{min} is set with $V_3 \geq -1$ V.

Automatic Retriggering

The current-detector circuit monitors the state of the triac after triggering by measuring the voltage drop at the triac gate. A current flow through the triac is recognized, when the voltage drop exceeds a threshold level of typ. 40 mV.

If the triac is quenched within the relevant half-wave after triggering; for example owing to low load currents before or after the zero crossing of current wave or; for commutator motors, owing to brush lifters. Then the automatic retriggering circuit ensures immediate retriggering, if necessary with a high repetition rate, t_{pp}/t_p , until the triac remains reliably triggered.

Current Synchronization, Pin 8

Current synchronization fulfils two functions:

- Monitoring the current flow after triggering.
In case the triac extinguishes again or it does not switch on, automatic triggering is activated as long as triggering is successful.
- Avoiding triggering due to inductive load.
In the case of inductive load operation the current synchronization ensures that in the new half wave no pulse is enabled as long as there is a current available from the previous half-wave, which flows from the opposite polarity to the actual supply voltage.

A special feature of the IC is the realization of current synchronization. The device evaluates the voltage at the pulse output between the gate and reference electrode of the triac. This results in saving separate current synchronization input with specified series resistance.

Voltage Synchronization with Mains Voltage Compensation, Pin 7

The voltage detector synchronizes the reference ramp with the mains supply voltage. At the same time, the mains dependent input current at Pin 7 is shaped and rectified internally. This current activates the automatic retriggering and at the same time is available at Pin 3 (see figure 9). By suitable dimensioning, it is possible to attain the specified compensation effect. Automatic retriggering and mains voltage compensation are not activated until $|V_{7-4}|$ increases to 8 V. Resistance, $R_{sync.}$, defines the width of the zero voltage cross-over pulse, synchronization current, and hence the mains supply voltage compensation current. If the mains voltage compensation and the automatic retriggering are not required, both functions can be suppressed by limiting $|V_{7-4}| \leq 7$ V (see figure 4).

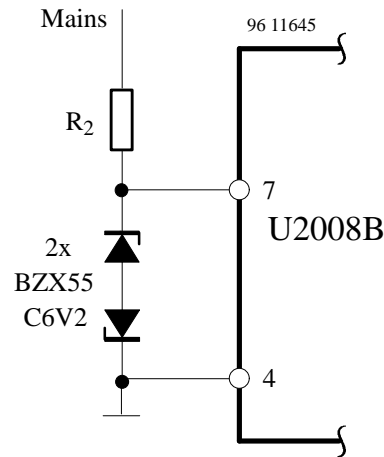


Figure 4. Suppression of automatic retriggering and mains voltage compensation

A further feature of the IC is the selection between soft-start or load-current compensation. Soft-start is possible by connecting a capacitor between Pin 1 and Pin 4, see figure 8. In the case of load current compensation, Pin 1 is directly connected with resistance R_6 , which is used for sensing load current.

Load Current Detection, Pin 1

The circuit continuously measures the load current as a voltage drop at resistance R_6 . The evaluation and use of both half waves results in a quick reaction to load current change. Due to voltage at resistance R_6 , there is an increase of input current at Pin 1. This current increase controls the internal current source, whose positive current values is available at Pin 3 (see figure 10). The output current generated at Pin 3 contains the difference from the load-current detection and from the mains-voltage compensation (see figure 1).

The effective control voltage is the final current at Pin 3 together with the desired value network. An increase of mains voltage causes the increase of control angle α . An increase of load current results in a decrease in the control angle. This avoids a decrease in revolution by increasing the load as well as the increase of revolution by the increment of mains supply voltage.

Absolute Maximum Ratings

$V_S = 14\text{ V}$, reference point Pin 4, unless otherwise specified

Parameters	Symbol	Value	Unit
Current limitation Pin 5 $t \leq 10\ \mu\text{s}$	$-I_S$ $-i_S$	30 100	mA mA
Sync. currents Pin 7 $t \leq 10\ \mu\text{s}$	$\pm I_{\text{syncV}}$ $\pm i_{\text{syncV}}$	5 20	mA mA
Phase control Pin 3			
Control voltage	$-V_I$	V_S to 0	V
Input current	$\pm I_I$	500	μA
Charge current Pin 6	$-I_{\phi\text{max}}$	0.5	mA
Load current monitoring / Soft-start Pin 1			
Input current	I_I	1	mA
Input voltage	V_I	-40 to +125	V
Pulse output			
Input voltage Pin 8	$+V_I$ $-V_I$	2 V_S	V V
Storage temperature range	T_{stg}	-40 to +125	$^{\circ}\text{C}$
Junction temperature range	T_j	-10 to +125	$^{\circ}\text{C}$

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient DIP8 SO8 on p.c. SO8 on ceramic	R_{thJA}	110 220 140	K/W K/W K/W

Electrical Characteristics

$V_S = -13\text{ V}$, $T_{\text{amb}} = 25^{\circ}\text{C}$, reference point Pin 4, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply Pin 5						
Supply voltage limitation	$-I_S = 3.5\text{ mA}$ $-I_S = 30\text{ mA}$	$-V_S$	14.5 14.6		16.5 16.8	V V
Current requirement	Pins 1, 4 and 7 open	$-I_S$			3.0	mA
Voltage monitoring Pin 5						
Turn-on threshold		$-V_{\text{TON}}$		11.3	12.3	V
Phase control						
Input current	Voltage sync. Pin 7 Current sync. Pin 8	$\pm I_{\text{syncV}}$ $\pm I_{\text{syncI}}$		0.15	2 30	mA μA
Voltage limitation	$\pm I_L = 2\text{ mA}$ Pin 7	$\pm V_{\text{syncV}}$	8.0	8.5	9.0	V

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Reference ramp , see figure 5						
Charge current	Pin 7	I_{ϕ}	1		100	μA
Start voltage	Pin 2	$-V_{\text{max}}$	1.85	1.95	2.05	V
Temperature coefficient of start voltage	Pin 2	$-TC_R$		-0.003		%/K
R_{ϕ} – reference voltage	$I_{\phi} = 10 \mu\text{A}$ Pins 6 – 5	$V_{R\phi}$	0.96	1.02	1.10	V
Temperature coefficient	$I_{\phi} = 10 \mu\text{A}$ Pin 6	$TC_{VR\phi}$		0.03		%/K
	$I_{\phi} = 1 \mu\text{A}$			0.06		%/K
Pulse output , see figure 6 Pin 8						
Output pulse current	$V_8 = -1.2$, $R_{GT} = 0 \Omega$	I_0	100	125	150	mA
Output pulse width	$C_3 = 3.3 \text{ nF}$, $V_S = V_{\text{limit}}$	t_p		30		μs
Automatic retriggering Pin 8						
Turn-on threshold voltage		$\pm V_{\text{ION}}$	20		60	mV
Repetition rate	$I_7 \geq 150 \mu\text{A}$	t_{pp}	3	5	7.5	t_p
Soft start , see figure 8 Pin 1						
Starting current	$V_{1-4} = 8 \text{ V}$	I_0	5	10	15	μA
Final current	$V_{1-4} = -2 \text{ V}$	I_0	15	25	40	μA
Discharge current		$-I_0$	0.5			mA
Output current	Pin 3	$-I_0$	0.2		2	mA
Supply voltage compensation , see figure 9						
Current transfer gain I_7/I_3	Pins 7, Pin 3 Pins 1 and 2 open	G_i	14	17	20	
Reverse current	$V_{(R6)} = V_3 = V_7 = 0$, Pin 3	$\pm I_R$			2	μA
Load current detection , $V_7 = 0$, see figure 10						
Transfer gain	I_3/V_1	G	0.280	0.320	0.370	$\mu\text{A/mV}$
Offset current	$V_1 = 0, V_3 = -8 \text{ V}$, Pin 3	I_0	0	3	6	μA
Input voltage	Pin 1	$-V_I$	300		400	mV
Input offset voltage	Pin 1	$\pm V_0$			6	mV

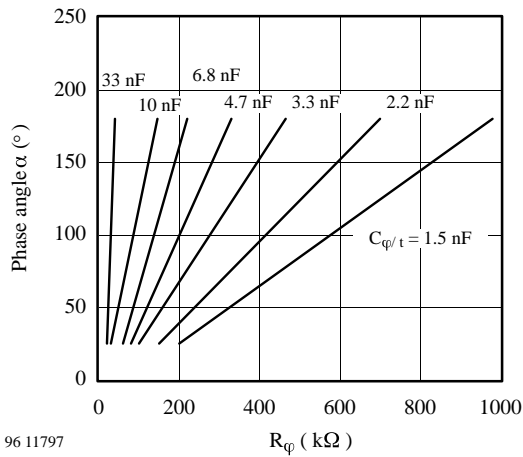


Figure 5.

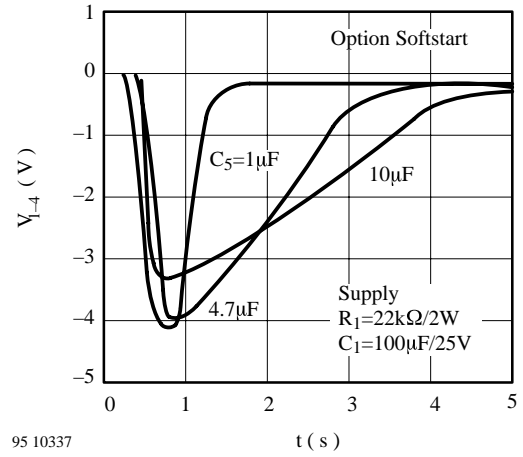


Figure 8.

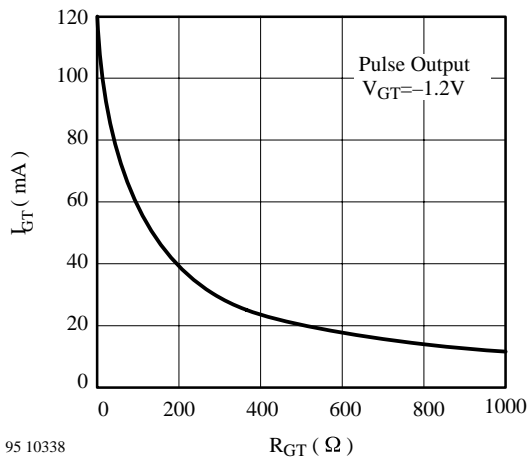


Figure 6.

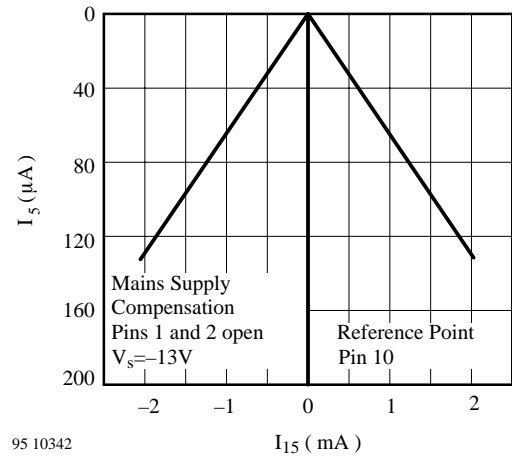


Figure 9.

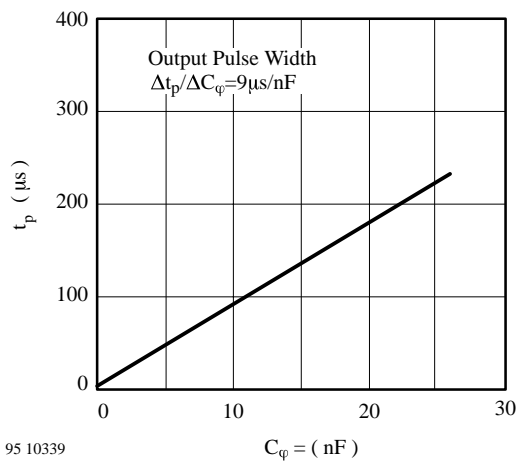


Figure 7.

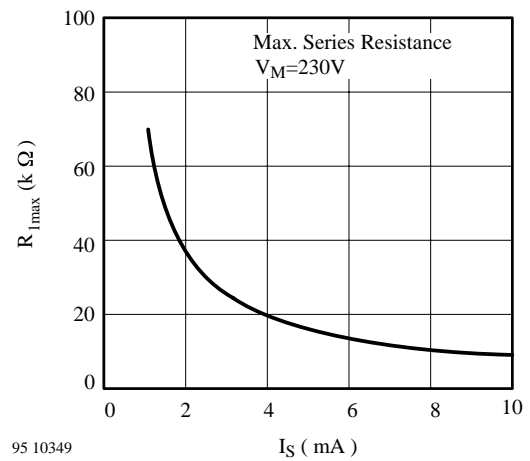


Figure 10.

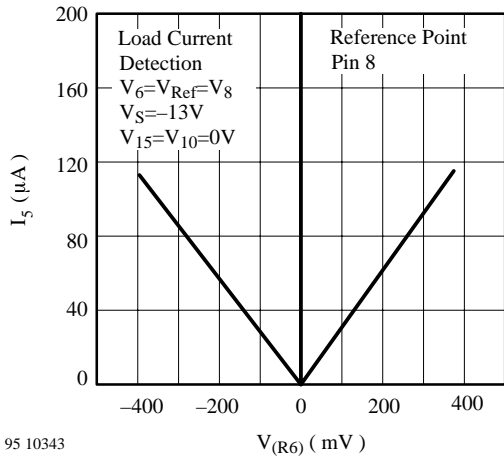


Figure 11.

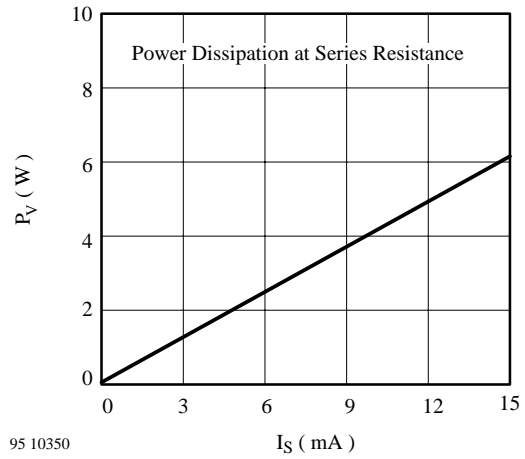


Figure 13.

revolution

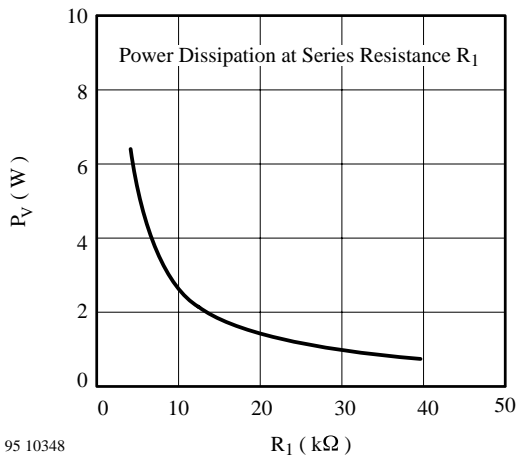
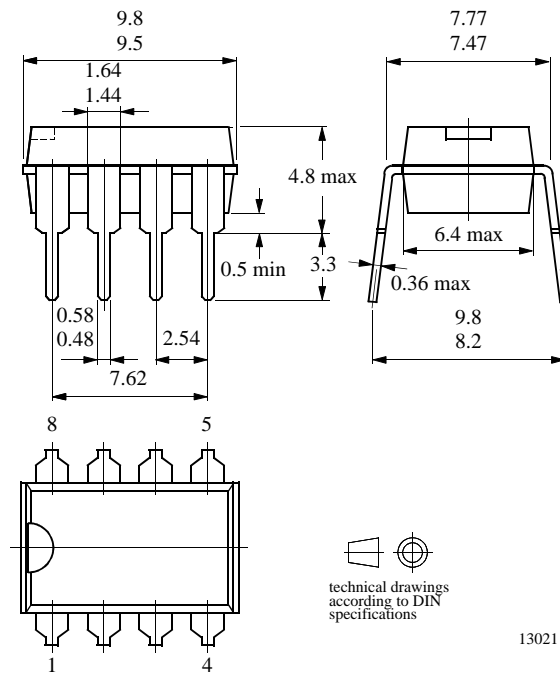


Figure 12.

Package Information

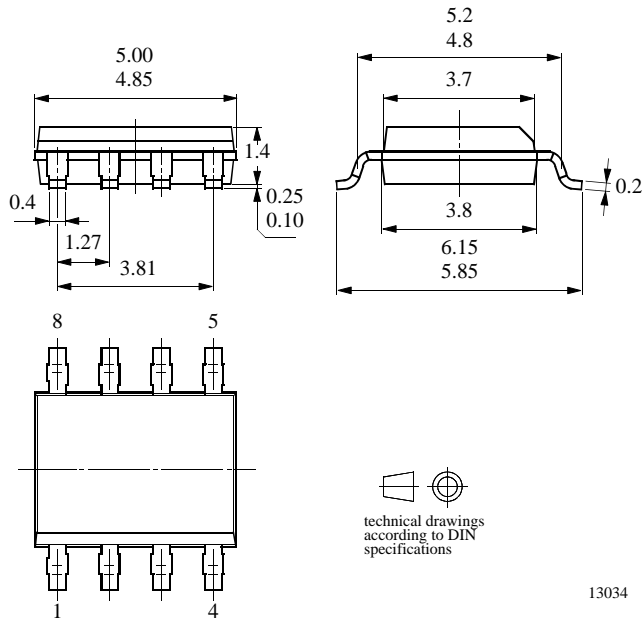
Package DIP8

Dimensions in mm



Package SO8

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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