TF Semiconductor Solutions

ADVANCE INFO

TF2304M

Half-Bridge Gate Driver

Features:

- **Drives two N-channel MOSFETs or IGBTs in a half bridge configuration**
- **Floating high-side driver in bootstrap operation to 600V**
- **290mA source/600mA sink output current capability**
- **Outputs tolerant to negative transients**
- **Internal logic and deadtime (100ns) to protect MOSFETs**
- **Logic input (HIN and LIN) 3.3V capability**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for high and low side drivers**
- **Extended temperature range:-40°C to +124°C**

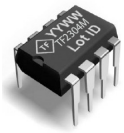
Description

The TF2304M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. TF Semi's high voltage process enables the TF2304M's high side to switch to 600V in a bootstrap operation.

The TF2304M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. An internal deadtime of 100ns protects high-voltage MOSFETs from shoot-through.

The TF2304M is offered in 8-pin PDIP and SOIC narrow package and operates over an extended -40°C to +125°C temperature range.

SOIC-8(N)



PDIP-8

Applications

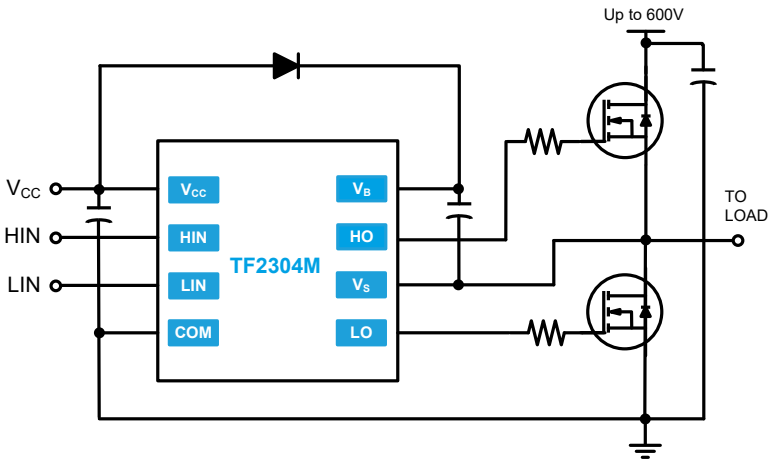
- Motor Controls
- AC-DC Inverters
- DC-DC Converters
- Class D Power Amplifiers

Ordering Information

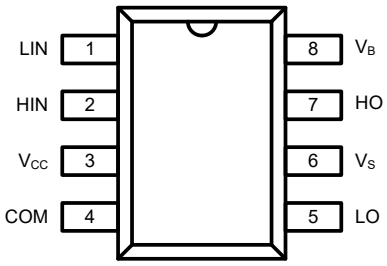
Year Year Week Week

PART NUMBER	PACKAGE	PACKING / Qty	MARK
TF2304M-3AS	PDIP-8	Tube / 50	YYWW TF2304M Lot ID
TF2304M-TAU	SOIC-8(N)	Tube / 100	YYWW TF2304M Lot ID
TF2304M-TAH	SOIC-8(N)	Tape & Reel / 2500	

Typical Application



Pin Diagrams



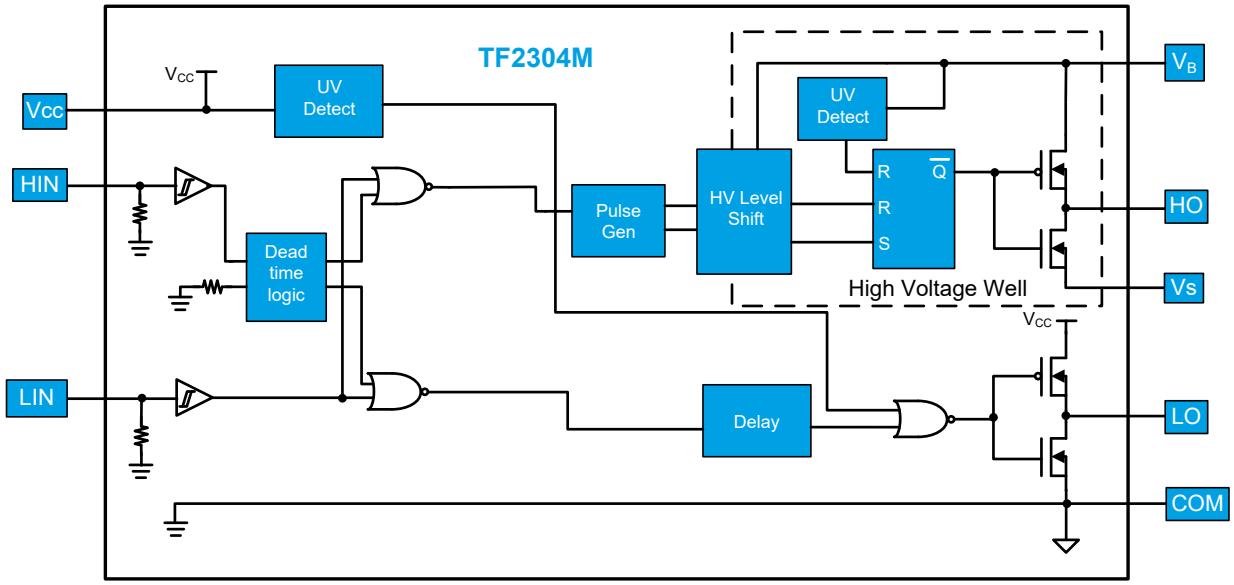
Top View: SOIC-8, PDIP-8

TF2304M

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output, in phase with HO
LIN	Logic input for low side gate driver output, in phase with LO
COM	Low-side and logic return
LO	Low-side gate drive output
V_{CC}	Low-side and logic fixed supply
V_S	High-side floating supply return
HO	High-side gate drive output
V_B	High-side floating supply

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage.....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side and logic fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN).....V_{SS}- 0.3V to V_{cc}+0.3V

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....1.25W
PDIP-8.....1.6W

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

PDIP-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....15 °C/W
θ_{JA}.....45 °C/W

SOIC-8(N) Thermal Resistance ***(NOTE2)***
θ_{JC}.....25 °C/W
θ_{JA}.....55 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***(NOTE 3)***	600	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side and logic fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5 V to +600 V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10 V to 20 V *NOTE 5*	2.3			V
V_{IL}	Logic "0" input voltage				0.7	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.05	0.2	
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.02	0.1	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V	20	60	150	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V	50	260	400	µA
I_{IN+}	Logic "1" input bias current	VIN = 5V		5	40	µA
I_{IN-}	Logic "0" input bias current	VIN = 0V		1.0	5.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		7.7	8.7	9.7	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.0	8.0	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.7	8.7	9.7	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.0	8.0	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 µs	60	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 µs	130	600		

NOTE4 *The V_{IN}, V_{Th}, I_{IN} parameters are referenced to COM and are applicable to the two logic input pins: HIN and LIN. The V_0 and I_0 parameters are referenced to COM and are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.3V minimum with a pulse width of 200ns minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V and C_L = 1000 pF, and T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		95	210	ns
t_{OFF}	Turn-off propagation delay	V_S = 0 V or 600V		100	210	
$t_{DM\ ON}$	Delay matching HS & LS turn on/off				50	
t_r	Turn-on rise time			70	120	
t_f	Turn-off fall time			35	60	
t_{DT}	Deadtime: $t_{DT\ LO\text{-}HO}$ & $t_{DT\ HO\text{-}LO}$		80	100	190	

Timing Waveforms

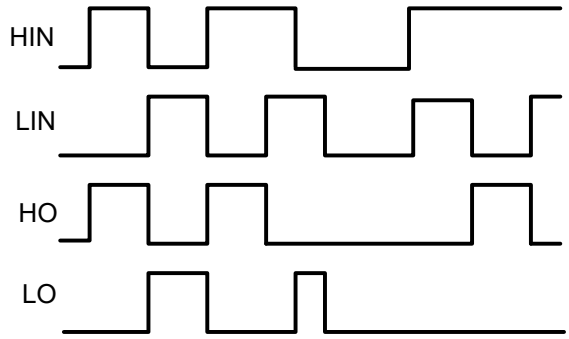


Figure 1. Input / Output Timing Diagram

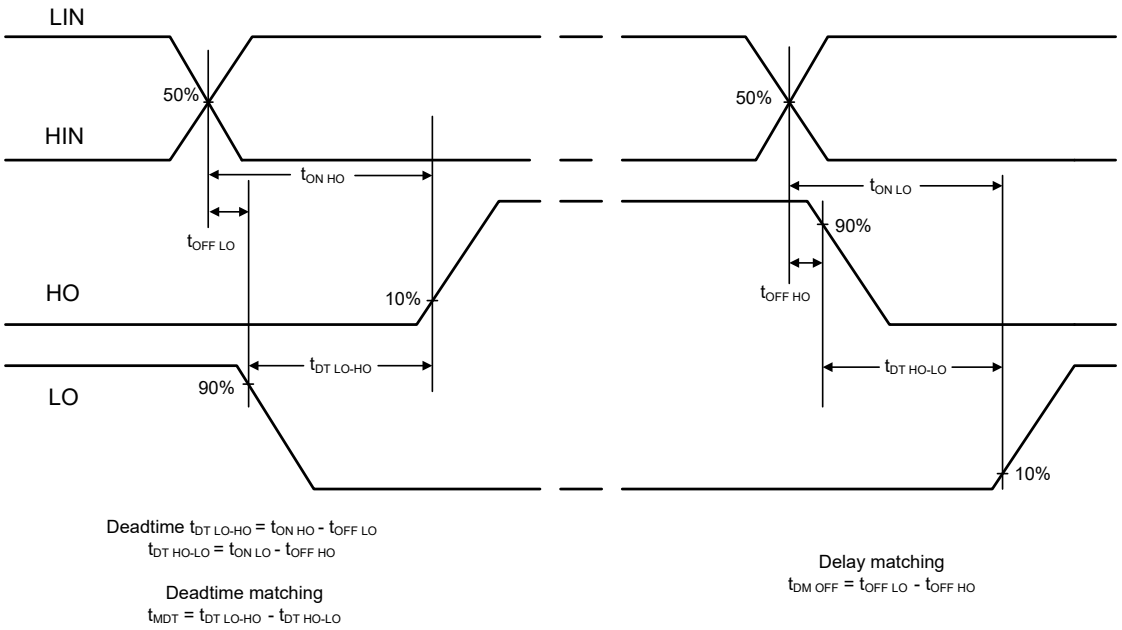
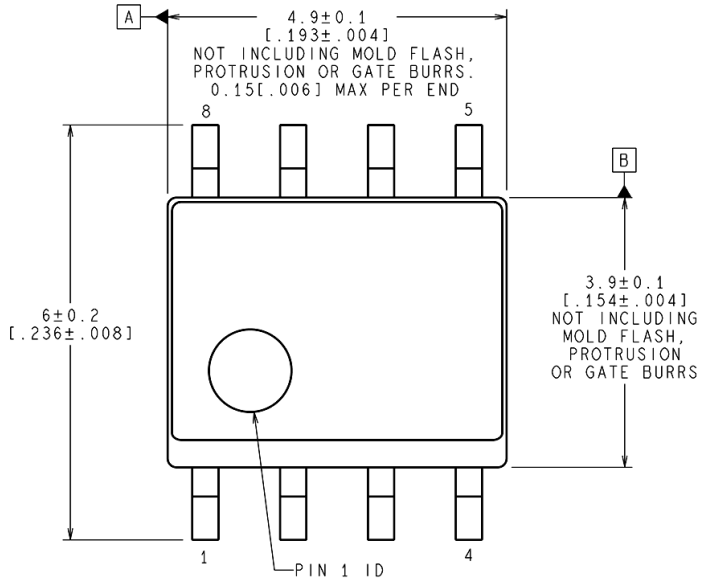
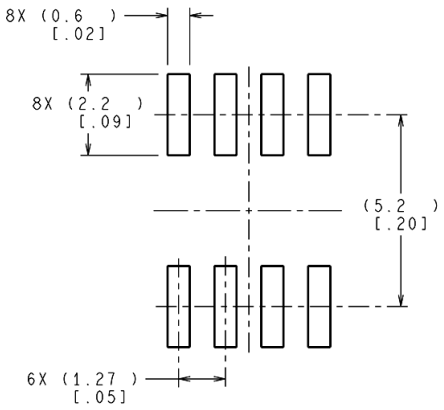


Figure 2. Switching Time Waveform Definition

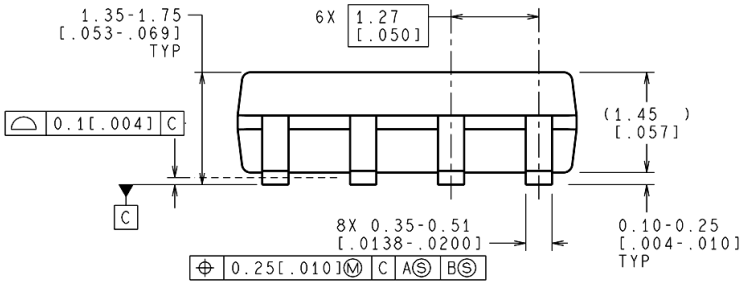
Package Dimensions (SOIC-8N)

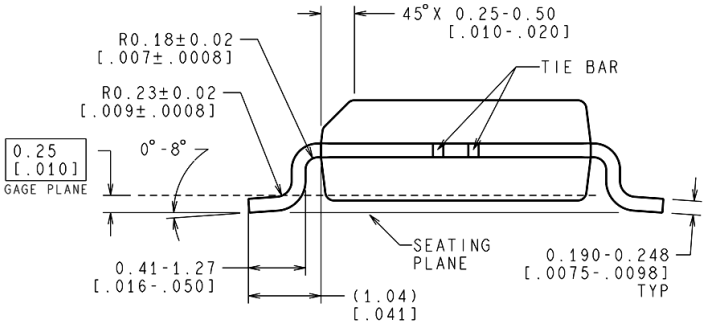
Please contact support@tfsemi.com for package availability.





RECOMMENDED LAND PATTERN





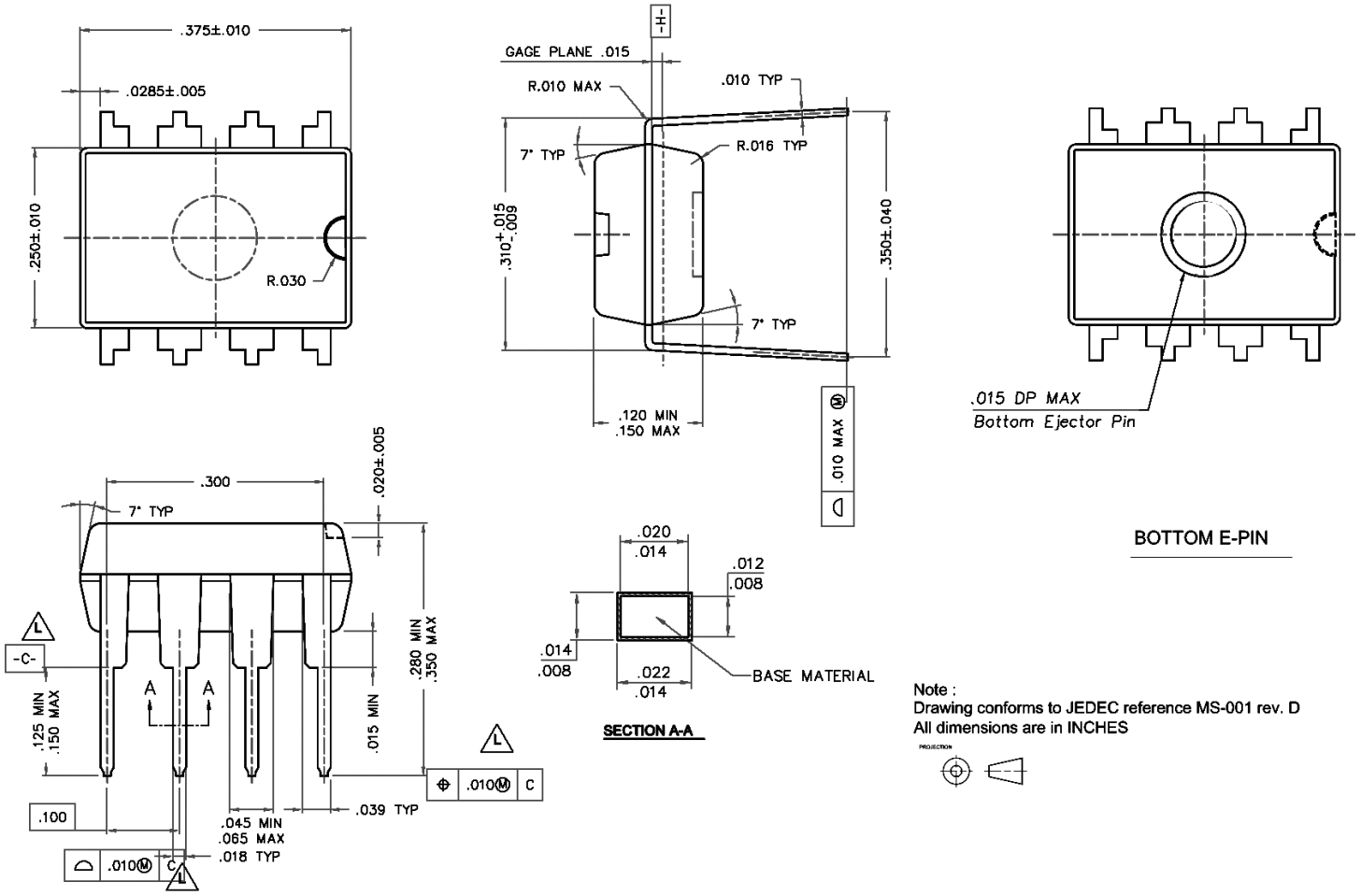
NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (PDIP-8)

Please contact support@tfsemi.com for package availability.



Revision History

Rev.	Change	Owner	Date
1.0	First release, AI datasheet	Keith Spaulding	3/3/2017
1.1	Add Note 5	Keith Spaulding	5/28/2019

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