

Features

- Core
 - ARM® Cortex®-M3 revision 2.0 running at up to 84 MHz
 - Memory Protection Unit (MPU)
 - Thumb®-2 instruction set
 - 24-bit SysTick Counter
 - Nested Vector Interrupt Controller
- Memories
 - From 256 to 512 Kbytes embedded Flash, 128-bit wide access, memory accelerator, dual bank
 - From 32 to 100 Kbytes embedded SRAM with dual banks
 - 16 Kbytes ROM with embedded bootloader routines (UART, USB) and IAP routines
 - Static Memory Controller (SMC): SRAM, NOR, NAND support. NAND Flash controller with 4-kbyte RAM buffer and ECC
- System
 - Embedded voltage regulator for single supply operation
 - POR, BOD and Watchdog for safe reset
 - Quartz or ceramic resonator oscillators: 3 to 20 MHz main and optional low power 32.768 kHz for RTC or device clock.
 - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz Default Frequency for fast device startup
 - Slow Clock Internal RC oscillator as permanent clock for device clock in low power mode
 - One PLL for device clock and one dedicated PLL for USB 2.0 High Speed Mini Host/Device
 - Temperature Sensor
 - Up to 17 peripheral DMA (PDC) channels and 6-channel central DMA plus dedicated DMA for High-Speed USB Mini Host/Device and Ethernet MAC
- Low Power Modes
 - Sleep and Backup modes, down to 2.5 µA in Backup mode.
 - Backup domain: VDDBU pin, RTC, eight 32-bit backup registers
 - Ultra Low-power RTC
- Peripherals
 - USB 2.0 Device/Mini Host: 480 Mbps, 4-kbyte FIFO, up to 10 bidirectional Endpoints, dedicated DMA
 - Up to 4 USARTs (ISO7816, IrDA®, Flow Control, SPI, Manchester and LIN support) and one UART
 - 2 TWI (I2C compatible), up to 6 SPIs, 1 SSC (I2S), 1 HSMCI (SDIO/SD/MMC) with up to 2 slots
 - 9-Channel 32-bit Timer/Counter (TC) for capture, compare and PWM mode, Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
 - Up to 8-channel 16-bit PWM (PWMC) with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
 - 32-bit Real Time Timer (RTT) and RTC with calendar and alarm features
 - 16-channel 12-bit 1Msps ADC with differential input mode and programmable gain stage
 - One 2-channel 12-bit 1 Msps DAC
 - One Ethernet MAC 10/100 (EMAC) with dedicated DMA
 - Two CAN Controller with eight Mailboxes
 - One True Random Number Generator (TRNG)
 - Write Protected Registers
- I/O
 - Up to 103 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
 - Up to Six 32-bit Parallel Input/Outputs (PIO)
- Packages
 - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm
 - 100-ball LFBGA, 9 x 9 mm, pitch 0.8 mm
 - 144-lead LQFP, 20 x 20 mm, pitch 0.5 mm
 - 144-ball LFBGA, 10 x 10 mm, pitch 0.8 mm



AT91SAM ARM-based Flash MCU

SAM3X SAM3A Series

Summary

11057BS-ATARM-13-Jul-12



1. SAM3X/A Description

Atmel's SAM3X/A series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 84 MHz and features up to 512 Kbytes of Flash and up to 100 Kbytes of SRAM. The peripheral set includes a High Speed USB Host and Device port with embedded transceiver, an Ethernet MAC, 2x CANs, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface with NAND Flash controller, 5x UARTs, 2x TWIs, 4x SPIs, as well as 1 PWM timer, 9x general-purpose 32-bit timers, an RTC, a 12-bit ADC and a 12-bit DAC.

The SAM3X/A series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders.

The SAM3X/A architecture is specifically designed to sustain high speed data transfers. It includes a multi-layer bus matrix as well as multiple SRAM banks, PDC and DMA channels that enable it to run tasks in parallel and maximize data throughput.

It operates from 1.62V to 3.6V and is available in 100- and 144-pin QFP and LFBGA packages.

The SAM3X/A devices are particularly well suited for networking applications: industrial and home/building automation, gateways.

1.1 Configuration Summary

The SAM3X/A series devices differ in memory sizes, package and features list. [Table 1-1](#) below summarizes the configurations.

Table 1-1. Configuration Summary

| Feature | SAM3X8E | SAM3X8C | SAM3X4E | SAM3X4C | SAM3A8C | SAM3A4C |
|-----------------------------|---|-----------------------|---|-----------------------|-----------------------|-----------------------|
| Flash | 2 x 256 Kbytes | 2 x 256 Kbytes | 2 x 128 Kbytes | 2 x 128 Kbytes | 2 x 256 Kbytes | 2 x 128 Kbytes |
| SRAM | 64 + 32 Kbytes | 64 + 32 Kbytes | 32 + 32 Kbytes | 32 + 32 Kbytes | 64 + 32 Kbytes | 32 + 32 Kbytes |
| Nand Flash Controller (NFC) | Yes | - | Yes | - | - | - |
| NFC SRAM ⁽¹⁾ | 4K bytes | - | 4K bytes | - | - | - |
| Package | LQFP144 LFBGA144 | LQFP100 LFBGA100 | LQFP144 LFBGA144 | LQFP100 LFBGA100 | LQFP100 LFBGA100 | LQFP100 LFBGA100 |
| Number of PIOs | 103 | 63 | 103 | 63 | 63 | 63 |
| SHDN Pin | Yes | No | Yes | No | No | No |
| EMAC | MII/RMII | RMII | MII/RMII | RMII | - | - |
| External Bus Interface | 16-bit data, 8 chip selects, 23-bit address | - | 16-bit data, 8 chip selects, 23-bit address | - | - | - |
| Central DMA | 6 | 4 | 6 | 4 | 4 | 4 |
| 12-bit ADC | 16 ch. ⁽²⁾ | 16 ch. ⁽²⁾ | 16 ch. ⁽²⁾ | 16 ch. ⁽²⁾ | 16 ch. ⁽²⁾ | 16 ch. ⁽²⁾ |
| 12-bit DAC | 2 ch. | 2 ch. | 2 ch. | 2 ch. | 2 ch. | 2 ch. |
| 32-bit Timer | 9 ⁽⁵⁾ | 9 ⁽⁶⁾ | 9 ⁽⁵⁾ | 9 ⁽⁶⁾ | 9 ⁽⁵⁾ | 9 ⁽⁵⁾ |
| PDC Channels | 17 | 15 | 17 | 15 | 15 | 15 |
| USART/ UART | 3/2 ⁽⁷⁾ | 3/1 | 3/2 ⁽⁷⁾ | 3/1 | 3/1 | 3/1 |
| SPI ⁽³⁾ | 1/4 + 3 | 1/4 + 3 | 1/4 + 3 | 1/4 + 3 | 1/4 + 3 | 1/4 + 3 |
| HSMCI | 1 slot 8 bits | 1 slot 4 bits | 1 slot 8 bits | 1 slot 4 bits | 1 slot 4 bits | 1 slot 4 bits |

- Notes:
1. 4 Kbytes RAM buffer of the NAND Flash Controller (NFC) which can be used by the core if not used by the NFC
 2. One channel is reserved for internal temperature sensor
 3. 2 / 8 + 4 = Number of SPI Controllers / Number of Chip Selects + Number of USART with SPI Mode
 4. 9 TC channels are accessible through PIO
 5. 6 TC channels are accessible through PIO
 6. 3 TC channels are accessible through PIO
 7. USART3 in UART mode (RXD3 and TXD3 available)

2. SAM3X/A Block Diagram

Figure 2-1. SAM3A4/8C (100 pins) Block Diagram

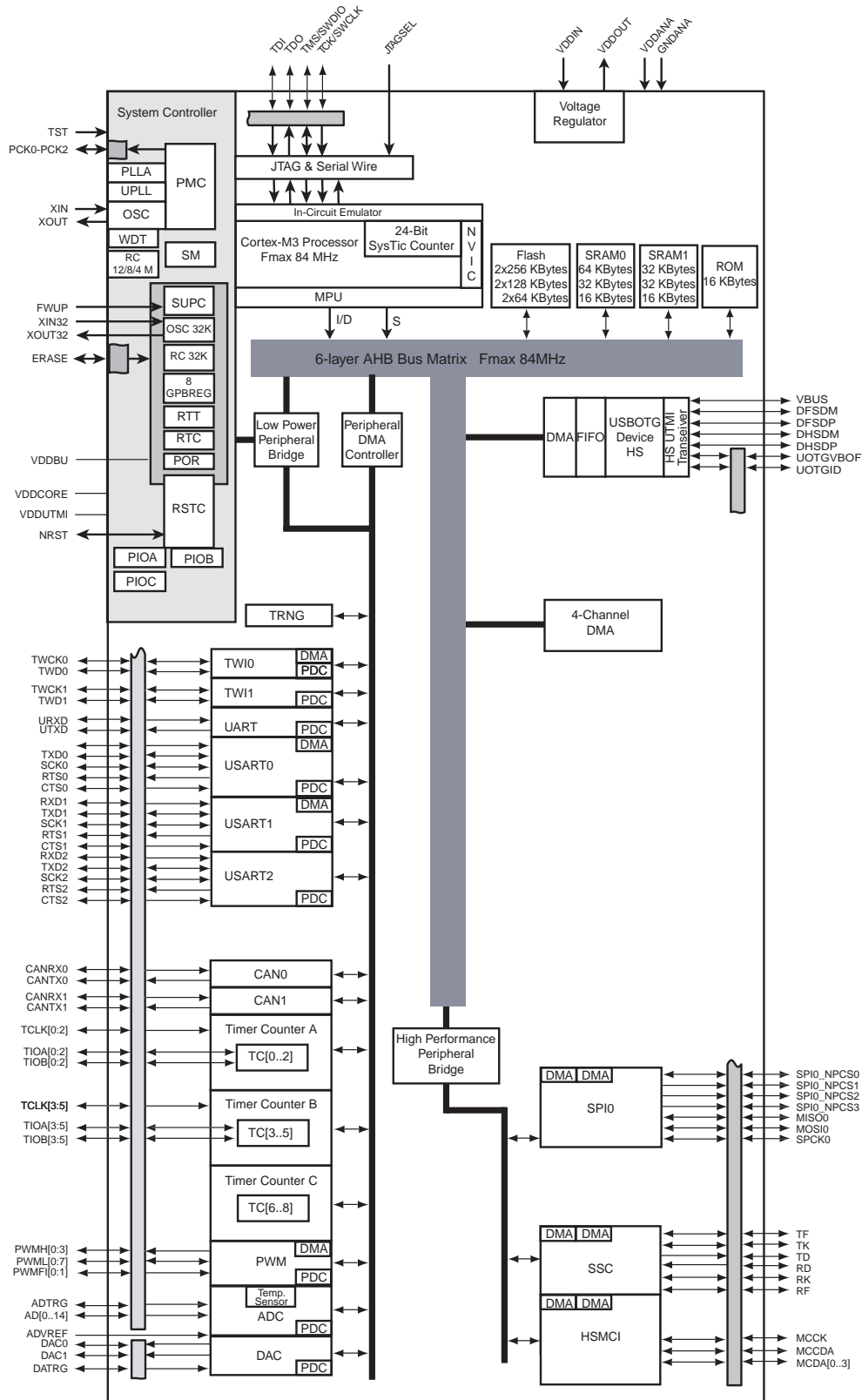


Figure 2-2. SAM3X4/8C (100 pins) Block Diagram

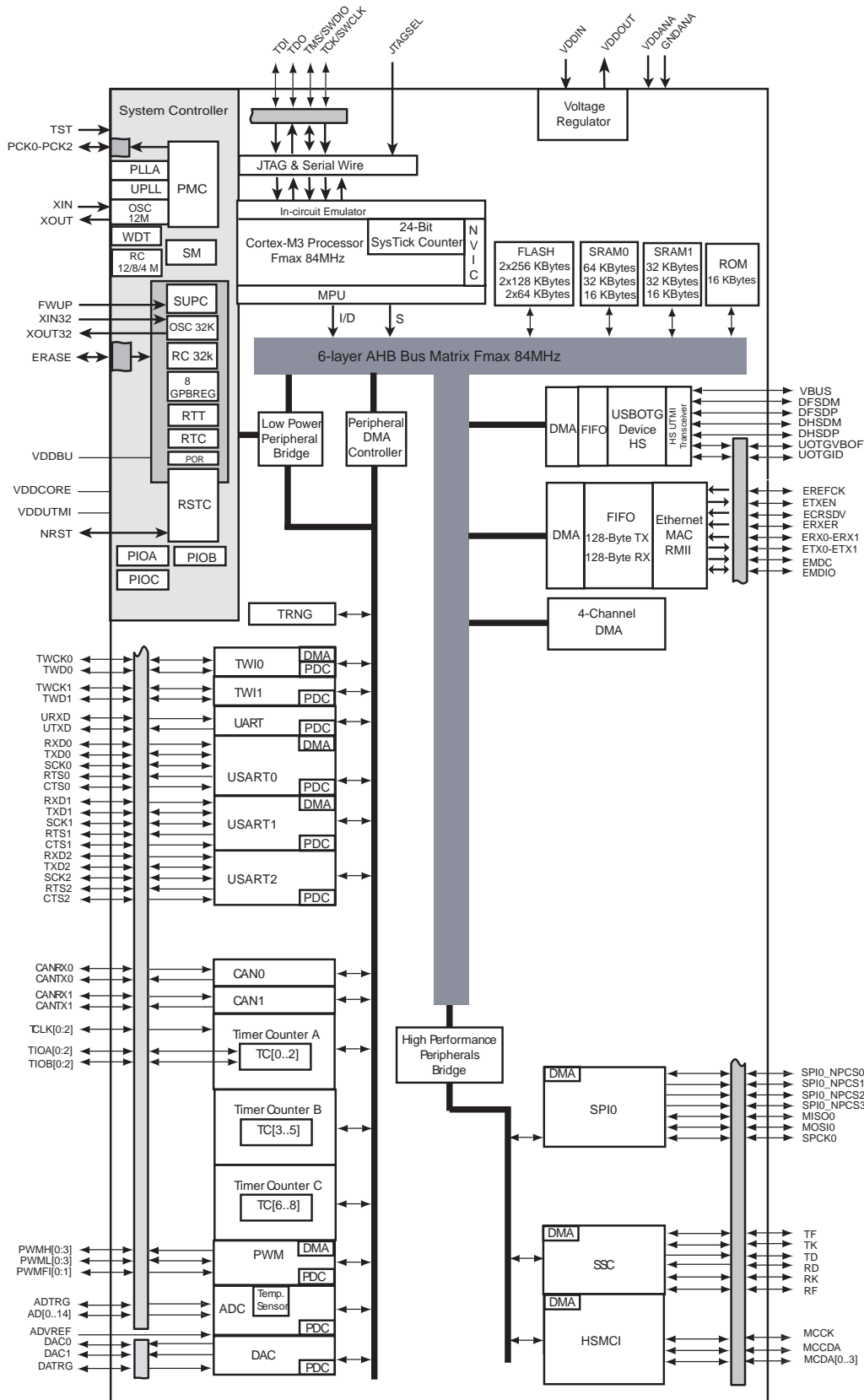
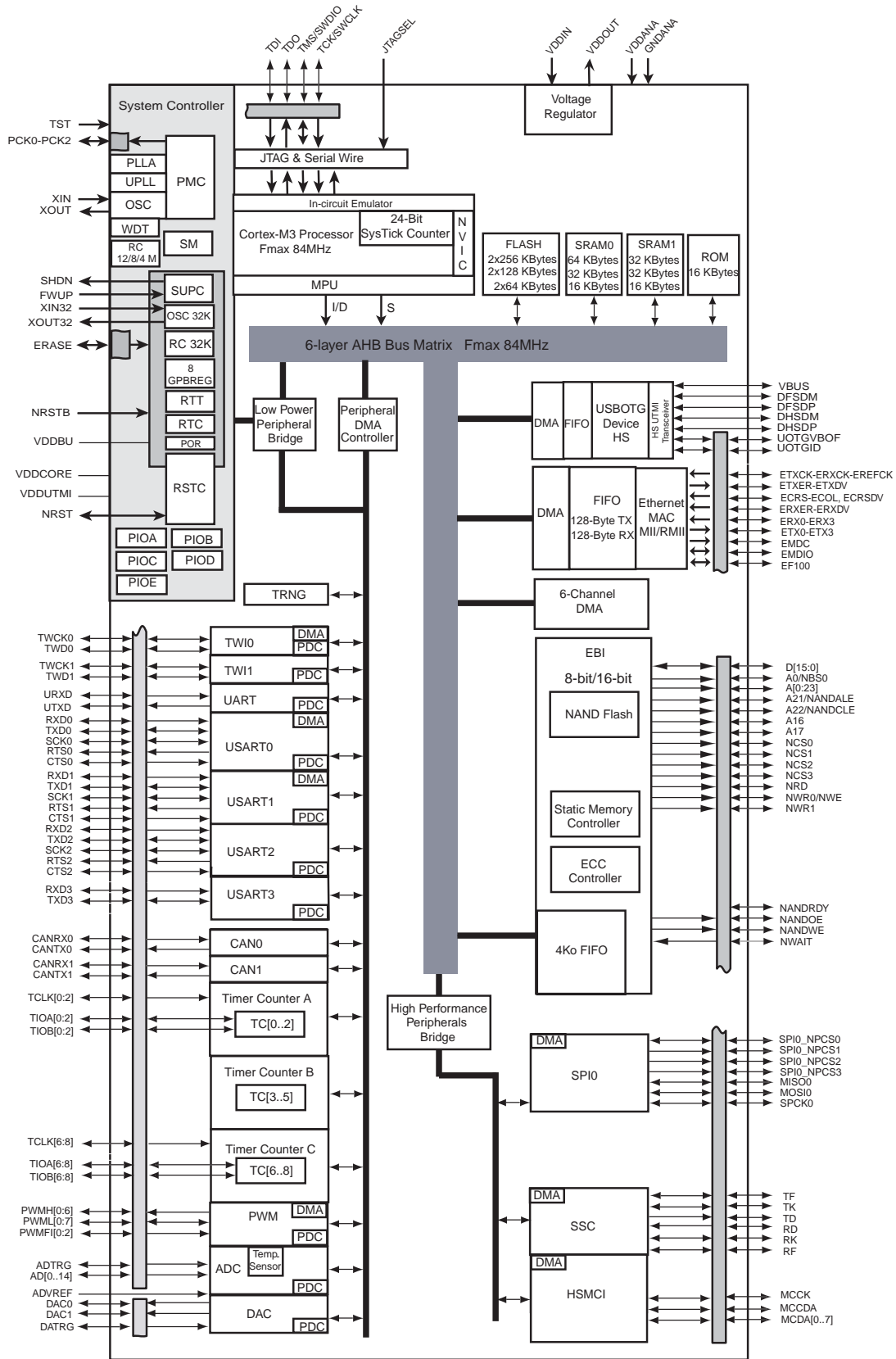


Figure 2-3. SAM3X4/8E (144 pins) Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

| Signal Name | Function | Type | Active Level | Voltage Reference | Comments |
|-------------------------------------|---|--------|--------------|-------------------|--|
| Power Supplies | | | | | |
| VDDIO | Peripherals I/O Lines Power Supply | Power | | | 1.62V to 3.6V |
| VDDUTMI | USB UTMI+ Interface Power Supply | Power | | | 3.0V to 3.6V |
| VDDOUT | Voltage Regulator Output | Power | | | |
| VDDIN | Voltage Regulator, ADC and DAC Power Supply | Power | | | |
| GNDUTMI | USB UTMI+ Interface Ground | Ground | | | |
| VDDBU | Backup I/O Lines Power Supply | Power | | | 1.62V to 3.6V |
| GNDBU | Backup Ground | Ground | | | |
| VDDPLL | PLL A, UPLL and Oscillator Power Supply | Power | | | 1.62 V to 1.95V |
| GNDPLL | PLL A, UPLL and Oscillator Ground | Ground | | | |
| VDDANA | ADC and DAC Analog Power Supply | Power | | | 2.0V to 3.6V |
| GNDANA | ADC and DAC Analog Ground | Ground | | | |
| VDDCORE | Core Chip Power Supply | Power | | | 1.62V to 1.95V |
| GND | Ground | Ground | | | |
| Clocks, Oscillators and PLLs | | | | | |
| XIN | Main Oscillator Input | Input | | VDDPLL | |
| XOUT | Main Oscillator Output | Output | | | |
| XIN32 | Slow Clock Oscillator Input | Input | | VDDBU | |
| XOUT32 | Slow Clock Oscillator Output | Output | | | |
| VBG | Bias Voltage Reference | Analog | | | |
| PCK0 - PCK2 | Programmable Clock Output | Output | | | |
| Shutdown, Wakeup Logic | | | | | |
| SHDN | Shut-Down Control | Output | | VDDBU | 0: The device is in backup mode 1: The device is running (not in backup mode) |
| FWUP | Force Wake-up Input | Input | | VDDBU | Needs external Pull-up |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage Reference | Comments |
|---|---|-------------|--------------|-------------------|---|
| ICE and JTAG | | | | | |
| TCK/SWCLK | Test Clock/Serial Wire Clock | Input | | VDDIO | Reset State: - SWJ-DP Mode - Internal pull-up disabled ⁽¹⁾ |
| TDI | Test Data In | Input | | | |
| TDO/TRACESWO | Test Data Out / Trace Asynchronous Data Out | Output | | | |
| TMS/SWDIO | Test Mode Select /Serial Wire Input/Output | Input / I/O | | | |
| JTAGSEL | JTAG Selection | Input | High | VDDBU | Permanent Internal pull-down |
| Flash Memory | | | | | |
| ERASE | Flash and NVM Configuration Bits Erase Command | Input | High | VDDIO | Pull-down resistor |
| Reset/Test | | | | | |
| NRST | Microcontroller Reset | I/O | Low | VDDIO | Pull-up resistor |
| NRSTB | Asynchronous Microcontroller Reset | Input | Low | VDDBU | Pull-up resistor |
| TST | Test Mode Select | Input | | VDDBU | Pull-down resistor |
| Universal Asynchronous Receiver Transceiver - UART | | | | | |
| URXD | UART Receive Data | Input | | | |
| UTXD | UART Transmit Data | Output | | | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage Reference | Comments |
|--|--------------------------|--------|--------------|-------------------|---|
| PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE | | | | | |
| PA0 - PA31 | Parallel IO Controller A | I/O | | VDDIO | <ul style="list-style-type: none"> •Schmitt Trigger⁽³⁾ Reset State: •PIO Input •Internal pull-up enabled |
| PB0 - PB31 | Parallel IO Controller B | I/O | | | <ul style="list-style-type: none"> •Schmitt Trigger⁽⁴⁾ Reset State: •PIO Input •Internal pull-up enabled |
| PC0 - PC30 | Parallel IO Controller C | I/O | | | <ul style="list-style-type: none"> •Schmitt Trigger⁽⁵⁾ Reset State: •PIO Input •Internal pull-up enabled |
| PD0 - PD30 | Parallel IO Controller D | I/O | | | <ul style="list-style-type: none"> •Schmitt Trigger⁽⁶⁾ Reset State: •PIO Input •Internal pull-up enabled |
| PE0 - PE31 | Parallel IO Controller E | I/O | | | <ul style="list-style-type: none"> •Schmitt Trigger⁽⁷⁾ Reset State: •PIO Input •Internal pull-up enabled |
| PF0 - PF6 | Parallel IO Controller F | I/O | | | <ul style="list-style-type: none"> •Schmitt Trigger⁽⁷⁾ Reset State: •PIO Input •Internal pull-up enabled |
| External Memory Bus | | | | | |
| D0 - D15 | Data Bus | I/O | | | Pulled-up input at reset |
| A0 - A23 | Address Bus | Output | | | 0 at reset |
| Static Memory Controller - SMC | | | | | |
| NCS0 - NCS7 | Chip Select Lines | Output | Low | | |
| NWR0 - NWR1 | Write Signal | Output | Low | | |
| NRD | Read Signal | Output | Low | | |
| NWE | Write Enable | Output | Low | | |
| NBS0 - NBS1 | Byte Mask Signal | Output | Low | | |
| NWAIT | External Wait Signal | Input | Low | | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage Reference | Comments |
|---|--------------------------------|--------|--------------|--------------------------|----------|
| NAND Flash Controller-NFC | | | | | |
| NANDOE | NAND Flash Output Enable | Output | Low | | |
| NANDWE | NAND Flash Write Enable | Output | Low | | |
| NANDRDY | NAND Ready | Input | | | |
| NANDCLE | NAND Flash Command Line Enable | Output | Low | | |
| NANDALE | NAND Flash Address Line Enable | Output | Low | | |
| High Speed Multimedia Card Interface HSMCI | | | | | |
| MCKK | Multimedia Card Clock | I/O | | | |
| MCCDA | Multimedia Card Slot A Command | I/O | | | |
| MCDA0 - MCDA7 | Multimedia Card Slot A Data | I/O | | | |
| MCCDB | Multimedia Card Slot B Command | I/O | | | |
| MCDB0 - MCDB3 | Multimedia Card Slot A Data | I/O | | | |
| Universal Synchronous Asynchronous Receiver Transmitter USARTx | | | | | |
| SCKx | USARTx Serial Clock | I/O | | | |
| TXDx | USARTx Transmit Data | I/O | | | |
| RXDx | USARTx Receive Data | Input | | | |
| RTSx | USARTx Request To Send | Output | | | |
| CTSx | USARTx Clear To Send | Input | | | |
| Ethernet MAC 10/100 - EMAC | | | | | |
| EREFCK | Reference Clock | Input | | RMII only | |
| ETXCK | Transmit Clock | Input | | MII only | |
| ERXCK | Receive Clock | Input | | MII only | |
| ETXEN | Transmit Enable | Output | | | |
| ETX0 - ETX3 | Transmit Data | Output | | ETX0 - ETX1 only in RMII | |
| ETXER | Transmit Coding Error | Output | | MII only | |
| ERXDV | Receive Data Valid | Input | | MII only | |
| ECRSDV | Carrier Sense and Data Valid | Input | | RMII only | |
| ERX0 - ERX3 | Receive Data | Input | | ERX0 - ERX1 only in RMII | |
| ERXER | Receive Error | Input | | | |
| ECRS | Carrier Sense | Input | | MII only | |
| ECOL | Collision Detected | Input | | MII only | |
| EMDC | Management Data Clock | Output | | | |
| EMDIO | Management Data Input/Output | I/O | | | |
| CAN Controller - CANx | | | | | |

Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage Reference | Comments |
|--|--|--------|--------------|-------------------|---|
| CANRXx | CAN Input | Input | | | |
| CANTXx | CAN Output | Output | | | |
| Synchronous Serial Controller - SSC | | | | | |
| TD | SSC Transmit Data | Output | | | |
| RD | SSC Receive Data | Input | | | |
| TK | SSC Transmit Clock | I/O | | | |
| RK | SSC Receive Clock | I/O | | | |
| TF | SSC Transmit Frame Sync | I/O | | | |
| RF | SSC Receive Frame Sync | I/O | | | |
| Timer/Counter - TC | | | | | |
| TCLKx | TC Channel x External Clock Input | Input | | | |
| TIOAx | TC Channel x I/O Line A | I/O | | | |
| TIOBx | TC Channel x I/O Line B | I/O | | | |
| Pulse Width Modulation Controller- PWMC | | | | | |
| PWMHx | PWM Waveform Output High for channel x | Output | | | |
| PWMLx | PWM Waveform Output Low for channel x, | Output | | | only output in complementary mode when dead time insertion is enabled |
| PWMFIx | PWM Fault Input for channel x | Input | | | |
| Serial Peripheral Interface - SPIx | | | | | |
| MISOx | Master In Slave Out | I/O | | | |
| MOSIx | Master Out Slave In | I/O | | | |
| SPCKx | SPI Serial Clock | I/O | | | |
| SPIx_NPCS0 | SPI Peripheral Chip Select 0 | I/O | Low | | |
| SPIx_NPCS1 - SPIx_NPCS3 | SPI Peripheral Chip Select | Output | Low | | |
| Two-Wire Interface- TWIx | | | | | |
| TWDx | TWIx Two-wire Serial Data | I/O | | | |
| TWCKx | TWIx Two-wire Serial Clock | I/O | | | |
| Analog-to-Digital Converter - ADC | | | | | |
| AD0 - AD14 | Analog Inputs | Analog | | | |
| ADTRG | ADC Trigger | Input | | | |
| ADVREF | ADC and DAC Reference | Analog | | | |
| Digital-to-Analog Converter - DAC | | | | | |
| DAC0 | DAC channel 0 analog output | Analog | | | |
| DAC1 | DAC channel 1 analog output | Analog | | | |
| DATR | DAC Trigger | | | | |



Table 3-1. Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Voltage Reference | Comments |
|---|--|--------|--------------|-------------------|----------|
| Fast Flash Programming Interface | | | | | |
| PGMEN0-PGMEN2 | Programming Enabling | Input | | VDDIO | |
| PGMM0-PGMM3 | Programming Mode | Input | | VDDIO | |
| PGMD0-PGMD15 | Programming Data | I/O | | VDDIO | |
| PGMRDY | Programming Ready | Output | High | VDDIO | |
| PGMNVALID | Data Direction | Output | Low | VDDIO | |
| PGMNOE | Programming Read | Input | Low | VDDIO | |
| PGMCK | Programming Clock | Input | | VDDIO | |
| PGMNCMD | Programming Command | Input | Low | VDDIO | |
| USB Mini Host/Device High Speed Device | | | | | |
| VBUS | USB Bus Power Measurement Port | Analog | | | |
| DFSDM | USB Full Speed Data - | Analog | | VDDUTMI | |
| DFSDP | USB Full Speed Data + | Analog | | VDDUTMI | |
| DHSDM | USB High Speed Data - | Analog | | VDDUTMI | |
| DHSDP | USB High Speed Data + | Analog | | VDDUTMI | |
| UOTGVBOF | USB VBus On/Off: Bus Power Control Port | | | VDDIO | |
| UOTGID | USB Identification: Mini Connector Identification Port | | | VDDIO | |

- Notes:
1. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.
 2. PIOA: Schmitt Trigger on all, except PA0, PA9, PA26, PA29, PA30, PA31
 3. PIOB: Schmitt Trigger on all, except PB14 and PB22
 4. PIOC: Schmitt Trigger on all, except PC2 to PC9, PC15 to PC24
 5. PIOD: Schmitt Trigger on all, except PD10 to PD30
 6. PIOE: Schmitt Trigger on all, except PE0 to PE4, PE15, PE17, PE19, PE21, PE23, PE25, PE29
 7. PIOF: Schmitt Trigger on all PIOs

3.1 Design Considerations

In order to facilitate schematic capture when using a SAM3X/A design, Atmel provides a “Schematics Checklist” Application Note. See <http://www.atmel.com/products/AT91/>

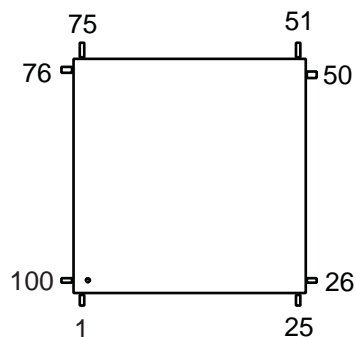
4. Package and Pinout

4.1 SAM3A4/8C and SAM3X4/8C Package and Pinout

The SAM3A4/8C and SAM3X4/8C are available in 100-lead LQFP and 100-ball LFBGA packages.

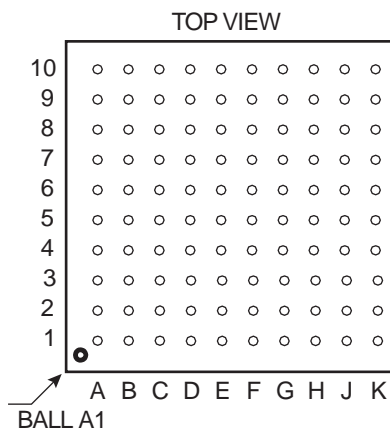
4.1.1 100-lead LQFP Package Outline

Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball LFBGA Package Outline

Figure 4-2. Orientation of the 100-ball LFBGA Package



4.1.3 100-lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3A4/8C and SAM3X4/8C Pinout

| | | | | | | | |
|----|---------|----|---------|----|---------|-----|---------|
| 1 | PB26 | 26 | DHSDP | 51 | VDDANA | 76 | PA26 |
| 2 | PA9 | 27 | DHSDM | 52 | GNDANA | 77 | PA27 |
| 3 | PA10 | 28 | VBUS | 53 | ADVREF | 78 | PA28 |
| 4 | PA11 | 29 | VBG | 54 | PB15 | 79 | PA29 |
| 5 | PA12 | 30 | VDDUTMI | 55 | PB16 | 80 | PB0 |
| 6 | PA13 | 31 | DFSDP | 56 | PA16 | 81 | PB1 |
| 7 | PA14 | 32 | DFSDM | 57 | PA24 | 82 | PB2 |
| 8 | PA15 | 33 | GNDUTMI | 58 | PA23 | 83 | PB3 |
| 9 | PA17 | 34 | VDDCORE | 59 | PA22 | 84 | PB4 |
| 10 | VDDCORE | 35 | JTAGSEL | 60 | PA6 | 85 | PB5 |
| 11 | VDDIO | 36 | XIN32 | 61 | PA4 | 86 | PB6 |
| 12 | GND | 37 | XOUT32 | 62 | PA3 | 87 | PB7 |
| 13 | PA0 | 38 | TST | 63 | PA2 | 88 | PB8 |
| 14 | PA1 | 39 | VDDBU | 64 | PB12 | 89 | VDDCORE |
| 15 | PA5 | 40 | FWUP | 65 | PB13 | 90 | VDDIO |
| 16 | PA7 | 41 | GND | 66 | PB17 | 91 | GND |
| 17 | PA8 | 42 | VDDOUT | 67 | PB18 | 92 | PB9 |
| 18 | PB28 | 43 | VDDIN | 68 | PB19 | 93 | PB10 |
| 19 | PB29 | 44 | GND | 69 | PB20 | 94 | PB11 |
| 20 | PB30 | 45 | VDDCORE | 70 | PB21 | 95 | PC0 |
| 21 | PB31 | 46 | PB27 | 71 | VDDCORE | 96 | PB14 |
| 22 | GNDPLL | 47 | NRST | 72 | VDDIO | 97 | PB22 |
| 23 | VDDPLL | 48 | PA18 | 73 | GND | 98 | PB23 |
| 24 | XOUT | 49 | PA19 | 74 | PA21 | 99 | PB24 |
| 25 | XIN | 50 | PA20 | 75 | PA25 | 100 | PB25 |

4.1.4 100-ball LFBGA Pinout

Table 4-2. 100-ball LFBGA SAM3X4/8E Package and Pinout

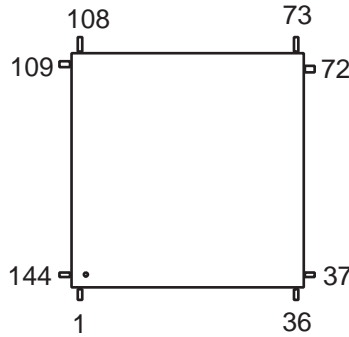
| | | | | | | | |
|-----|------|-----|---------|-----|---------|-----|---------|
| A1 | PB26 | C6 | PB11 | F1 | VDDPLL | H6 | NRST |
| A2 | PB24 | C7 | PB8 | F2 | GNDPLL | H7 | PA19 |
| A3 | PB22 | C8 | PB4 | F3 | PB30 | H8 | PA4 |
| A4 | PB14 | C9 | PB0 | F4 | PB29 | H9 | PA6 |
| A5 | PC0 | C10 | PA25 | F5 | GND | H10 | PA22 |
| A6 | PB9 | D1 | PA5 | F6 | GND | J1 | VBUS |
| A7 | PB6 | D2 | PA0 | F7 | VDDIO | J2 | DHSDP |
| A8 | PB2 | D3 | PA1 | F8 | PB13 | J3 | DHSMD |
| A9 | PA28 | D4 | VDDCORE | F9 | PB17 | J4 | JTAGSEL |
| A10 | PA26 | D5 | VDDIO | F10 | PB18 | J5 | XIN32 |
| B1 | PA11 | D6 | VDDCORE | G1 | XOUT | J6 | VDDIN |
| B2 | PB25 | D7 | VDDCORE | G2 | VDDUTMI | J7 | PA23 |
| B3 | PB23 | D8 | PB5 | G3 | PB31 | J8 | PA24 |
| B4 | PA10 | D9 | PB1 | G4 | GNDDBU | J9 | PB16 |
| B5 | PA9 | D10 | PA21 | G5 | PB27 | J10 | PA16 |
| B6 | PB10 | E1 | PB28 | G6 | PA18 | K1 | VBG |
| B7 | PB7 | E2 | PA7 | G7 | PA20 | K2 | DFSDP |
| B8 | PB3 | E3 | PA8 | G8 | PA3 | K3 | DFSDM |
| B9 | PA29 | E4 | VDDCORE | G9 | PA2 | K4 | VDDCORE |
| B10 | PA27 | E5 | GND | G10 | PB12 | K5 | XOUT32 |
| C1 | PA12 | E6 | GND | H1 | XIN | K6 | VDDOUT |
| C2 | PA14 | E7 | VDDIO | H2 | GNDUTMI | K7 | VDDANA |
| C3 | PA13 | E8 | PB19 | H3 | TST | K8 | GNDANA |
| C4 | PA17 | E9 | PB20 | H4 | VDDDBU | K9 | ADVREF |
| C5 | PA15 | E10 | PB21 | H5 | WAKEUP | K10 | PB15 |

4.2 SAM3X4/8E Package and Pinout

The SAM3X4/8E is available in 144-lead LQFP and 144-ball LFBGA packages.

4.2.1 144-lead LQFP Package Outline

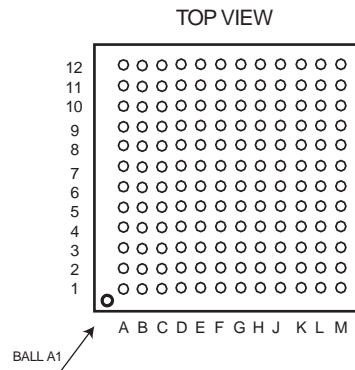
Figure 4-3. Orientation of the 144-lead LQFP Package



4.2.2 144-ball LFBGA Package Outline

The 144-Ball LFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 10 x 10 x 1.4 mm.

Figure 4-4. Orientation of the 144-ball LFBGA Package



4.2.3 144-lead LQFP Pinout

Table 4-3. 144-lead LQFP SAM3X4/8E Pinout

| | | | | | | | |
|----|---------|----|---------|-----|---------|-----|---------|
| 1 | PB26 | 37 | DHSDP | 73 | VDDANA | 109 | PA26 |
| 2 | PA9 | 38 | DHSDM | 74 | GNDANA | 110 | PA27 |
| 3 | PA10 | 39 | VBUS | 75 | ADVREF | 111 | PA28 |
| 4 | PA11 | 40 | VBG | 76 | PB15 | 112 | PA29 |
| 5 | PA12 | 41 | VDDUTMI | 77 | PB16 | 113 | PB0 |
| 6 | PA13 | 42 | DFSDP | 78 | PA16 | 114 | PB1 |
| 7 | PA14 | 43 | DFSDM | 79 | PA24 | 115 | PB2 |
| 8 | PA15 | 44 | GNDUTMI | 80 | PA23 | 116 | PC4 |
| 9 | PA17 | 45 | VDDCORE | 81 | PA22 | 117 | PC10 |
| 10 | VDDCORE | 46 | JTAGSEL | 82 | PA6 | 118 | PB3 |
| 11 | VDDIO | 47 | NRSTB | 83 | PA4 | 119 | PB4 |
| 12 | GND | 48 | XIN32 | 84 | PA3 | 120 | PB5 |
| 13 | PD0 | 49 | XOUT32 | 85 | PA2 | 121 | PB6 |
| 14 | PD1 | 50 | SHDN | 86 | PB12 | 122 | PB7 |
| 15 | PD2 | 51 | TST | 87 | PB13 | 123 | PB8 |
| 16 | PD3 | 52 | VDDBU | 88 | PB17 | 124 | VDDCORE |
| 17 | PD4 | 53 | FWUP | 89 | PB18 | 125 | VDDIO |
| 18 | PD5 | 54 | GNDBU | 90 | PB19 | 126 | GND |
| 19 | PD6 | 55 | PC1 | 91 | PB20 | 127 | PB9 |
| 20 | PD7 | 56 | VDDOUT | 92 | PB21 | 128 | PB10 |
| 21 | PD8 | 57 | VDDIN | 93 | PC11 | 129 | PB11 |
| 22 | PD9 | 58 | GND | 94 | PC12 | 130 | PC0 |
| 23 | PA0 | 59 | PC2 | 95 | PC13 | 131 | PC20 |
| 24 | PA1 | 60 | PC3 | 96 | PC14 | 132 | PC21 |
| 25 | PA5 | 61 | VDDCORE | 97 | PC15 | 133 | PC22 |
| 26 | PA7 | 62 | VDDIO | 98 | PC16 | 134 | PC23 |
| 27 | PA8 | 63 | PC5 | 99 | PC17 | 135 | PC24 |
| 28 | PB28 | 64 | PC6 | 100 | PC18 | 136 | PC25 |
| 29 | PB29 | 65 | PC7 | 101 | PC19 | 137 | PC26 |
| 30 | PB30 | 66 | PC8 | 102 | PC29 | 138 | PC27 |
| 31 | PB31 | 67 | PC9 | 103 | PC30 | 139 | PC28 |
| 32 | PD10 | 68 | PB27 | 104 | VDDCORE | 140 | PB14 |
| 33 | GNDPLL | 69 | NRST | 105 | VDDIO | 141 | PB22 |
| 34 | VDDPLL | 70 | PA18 | 106 | GND | 142 | PB23 |
| 35 | XOUT | 71 | PA19 | 107 | PA21 | 143 | PB24 |
| 36 | XIN | 72 | PA20 | 108 | PA25 | 144 | PB25 |

4.2.4 144-ball LFBGA Pinout

Table 4-4. 144-ball LFBGA SAM3X4/8E Pinout

| | | | | | | | |
|-----|------|-----|---------|-----|---------|-----|---------|
| A1 | PA9 | D1 | PA17 | G1 | PA5 | K1 | VDDCORE |
| A2 | PB23 | D2 | PD0 | G2 | PA7 | K2 | GNDUTMI |
| A3 | PB14 | D3 | PA11 | G3 | PA8 | K3 | VDDPLL |
| A4 | PC26 | D4 | PA15 | G4 | PA1 | K4 | NRSTB |
| A5 | PC24 | D5 | PA14 | G5 | GND | K5 | SHDN |
| A6 | PC20 | D6 | PC27 | G6 | GND | K6 | PC3 |
| A7 | PB10 | D7 | PC25 | G7 | GND | K7 | PC6 |
| A8 | PB6 | D8 | VDDIO | G8 | PC16 | K8 | PC7 |
| A9 | PB4 | D9 | PB5 | G9 | PC15 | K9 | PA18 |
| A10 | PC4 | D10 | PB0 | G10 | PC13 | K10 | PA23 |
| A11 | PA28 | D11 | PC30 | G11 | PB13 | K11 | PA16 |
| A12 | PA27 | D12 | PC19 | G12 | PB18 | K12 | PA24 |
| B1 | PA10 | E1 | PD1 | H1 | XOUT | L1 | DHSDP |
| B2 | PB26 | E2 | PD2 | H2 | PB30 | L2 | DHS DM |
| B3 | PB24 | E3 | PD3 | H3 | PB28 | L3 | VDDUTMI |
| B4 | PC28 | E4 | PD4 | H4 | PB29 | L4 | JTAGSEL |
| B5 | PC23 | E5 | PD5 | H5 | VDDBU | L5 | GNDBU |
| B6 | PC0 | E6 | VDDCORE | H6 | VDDCORE | L6 | PC1 |
| B7 | PB9 | E7 | VDDCORE | H7 | VDDIO | L7 | PC2 |
| B8 | PB8 | E8 | VDDCORE | H8 | PC12 | L8 | PC5 |
| B9 | PB3 | E9 | PB1 | H9 | PC11 | L9 | PC9 |
| B10 | PB2 | E10 | PC18 | H10 | PA3 | L10 | PA20 |
| B11 | PA26 | E11 | PB19 | H11 | PB12 | L11 | VDDANA |
| B12 | PA25 | E12 | PB21 | H12 | PA2 | L12 | PB16 |
| C1 | PA13 | F1 | PD8 | J1 | XIN | M1 | DFSDP |
| C2 | PA12 | F2 | PD6 | J2 | GNDPLL | M2 | DFSDM |
| C3 | PB25 | F3 | PD9 | J3 | PD10 | M3 | VBG |
| C4 | PB22 | F4 | PA0 | J4 | PB31 | M4 | VBUS |
| C5 | PC22 | F5 | PD7 | J5 | TST | M5 | XIN32 |
| C6 | PC21 | F6 | GND | J6 | FWUP | M6 | XOUT32 |
| C7 | PB11 | F7 | GND | J7 | PB27 | M7 | VDDOUT |
| C8 | PB7 | F8 | VDDIO | J8 | NRST | M8 | VDDIN |
| C9 | PC10 | F9 | PC17 | J9 | PA19 | M9 | PC8 |
| C10 | PA29 | F10 | PC14 | J10 | PA22 | M10 | GNDANA |
| C11 | PA21 | F11 | PB20 | J11 | PA4 | M11 | ADVREF |
| C12 | PC29 | F12 | PB17 | J12 | PA6 | M12 | PB15 |

5. Power Considerations

5.1 Power Supplies

The SAM3X/A series product has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals; voltage ranges from 1.62V to 1.95V.
- VDDIO pins: Power the Peripherals I/O lines; voltage ranges from 1.62V to 3.6V.
- VDDIN pin: Powers the Voltage regulator
- VDDOUT pin: It is the output of the voltage regulator.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.62V to 3.6V. VDDBU must be supplied before or at the same time than VDDIO and VDDCORE.
- VDDPLL pin: Powers the PLL A, UPLL and 3-20 MHz Oscillator; voltage ranges from 1.62V to 1.95V.
- VDDUTMI pin: Powers the UTMI+ interface; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDANA pin: Powers the ADC and DAC cells; voltage ranges from 2.0V to 3.6V.

Ground pins GND are common to VDDCORE and VDDIO pins power supplies.

Separated ground pins are provided for VDDBU, VDDPLL, VDDUTMI and VDDANA. These ground pins are respectively GNDBU, GNDPLL, GNDUTMI and GNDANA.

5.2 Voltage Regulator

The SAM3X/A series embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3X/A series but can be used to supply other parts in the application. It features two different operating modes:

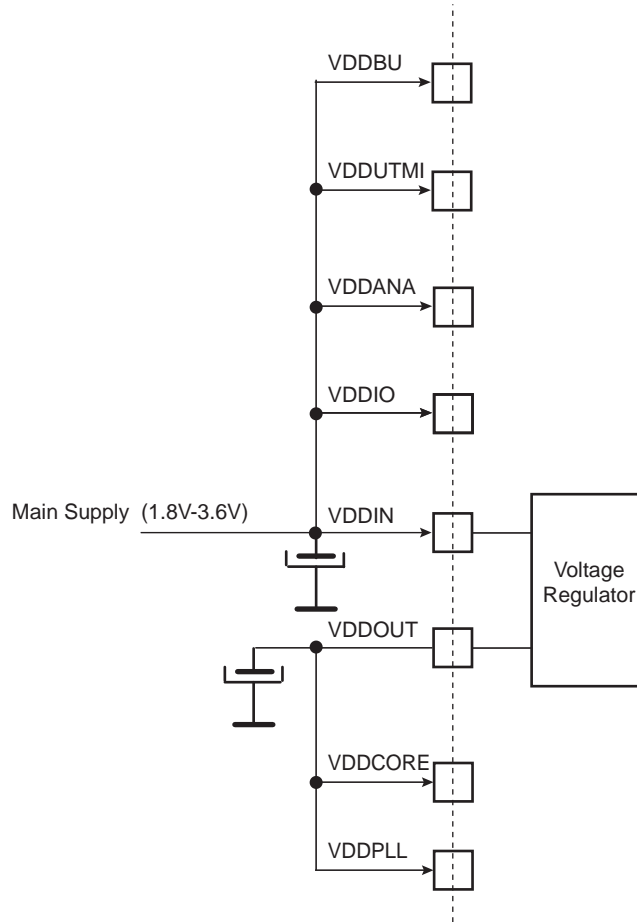
- In Normal mode, the voltage regulator consumes less than 700 μ A static current and draws 150 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode or when the output current is low, quiescent current is only 7 μ A.
- In Shutdown mode, the voltage regulator consumes less than 1 μ A while its output is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is inferior to 400 μ s.

For adequate input and output power supply decoupling/bypassing, refer to “Voltage Regulator” in the “Electrical Characteristics” section of the product datasheet.

5.3 Typical Powering Schematics

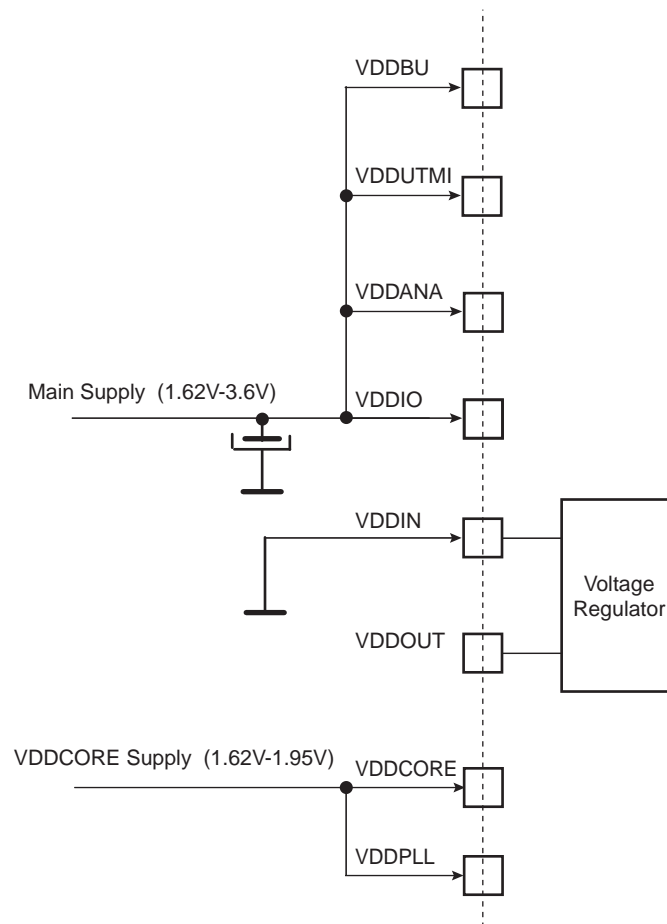
The SAM3X/A series supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

Figure 5-1. Single Supply



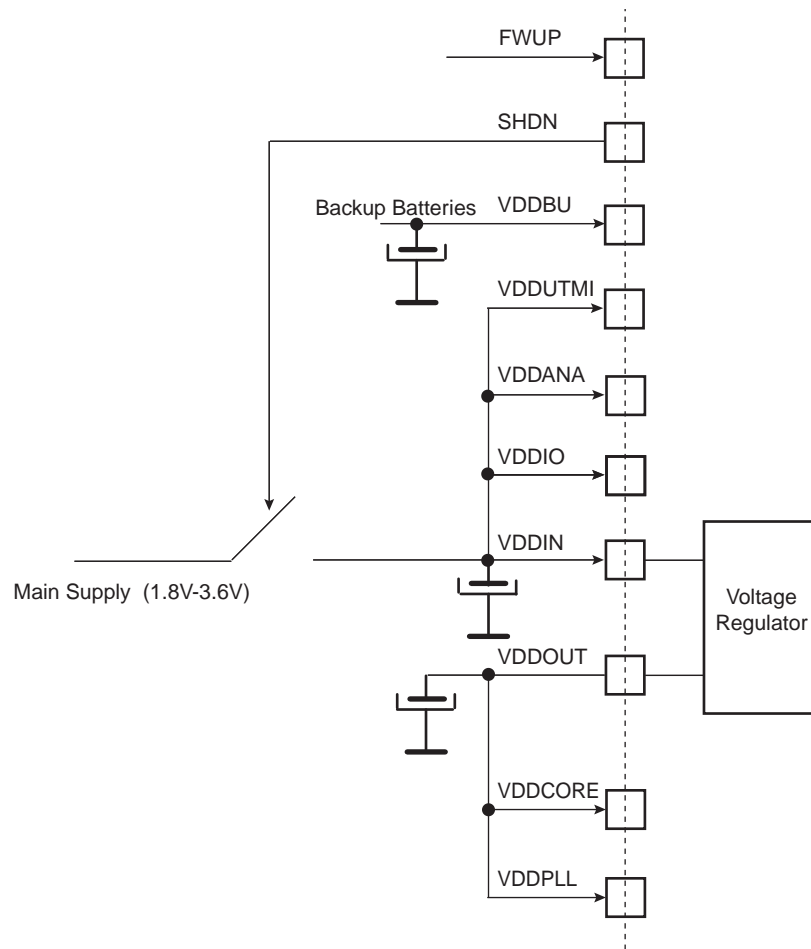
Note: Restrictions
 For USB, VDDUTMI needs to be greater than 3.0V.
 For ADC, VDDANA needs to be greater than 2.0V.
 For DAC, VDDANA needs to be greater than 2.4V.

Figure 5-2. Core Externally Supplied



Note: Restrictions
 For USB, VDDUTMI needs to be greater than 3.0V.
 For ADC, VDDANA needs to be greater than 2.0V.
 For DAC, VDDANA needs to be greater than 2.4V.

Note: Backup Batteries Used



- Note:
1. Restrictions
 - For USB, VDDUTMI needs to be greater than 3.0V.
 - For ADC, VDDANA needs to be greater than 2.0V.
 - For DAC, VDDANA needs to be greater than 2.4V.
 2. VDDUTMI and VDDANA cannot be left unpowered.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low Power Modes

The various low power modes of the SAM3X/A series are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (< 0.5ms).

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz Oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup Mode is based on the Cortex-M3 deep-sleep mode with the voltage regulator disabled.

The SAM3X/A series can be awakened from this mode through the Force Wake-up pin (FWUP), and Wake-up input pins WKUP0 to WKUP15, Supply Monitor, RTT or RTC wake-up event. Current Consumption is 2.5 μ A typical on VDDBU.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the Power management description in the “ARM Cortex M3 Processor” section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- FWUP pin (low level, configurable debouncing)
- WKUPEN0-15 pins (level transition, configurable debouncing)
- SM alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 μ s.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WKUP0-15 as fast startup wake-up pins (refer to [Section 5.7 “Fast Start-Up”](#)). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Current Consumption in Wait mode is typically 23 μ A for total current consumption if the internal voltage regulator is used or 15 μ A if an external regulator is used.

Entering Wait Mode:

- Select the 4/8/12 MHz Fast RC Oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.



The processor can be awakened from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake-up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

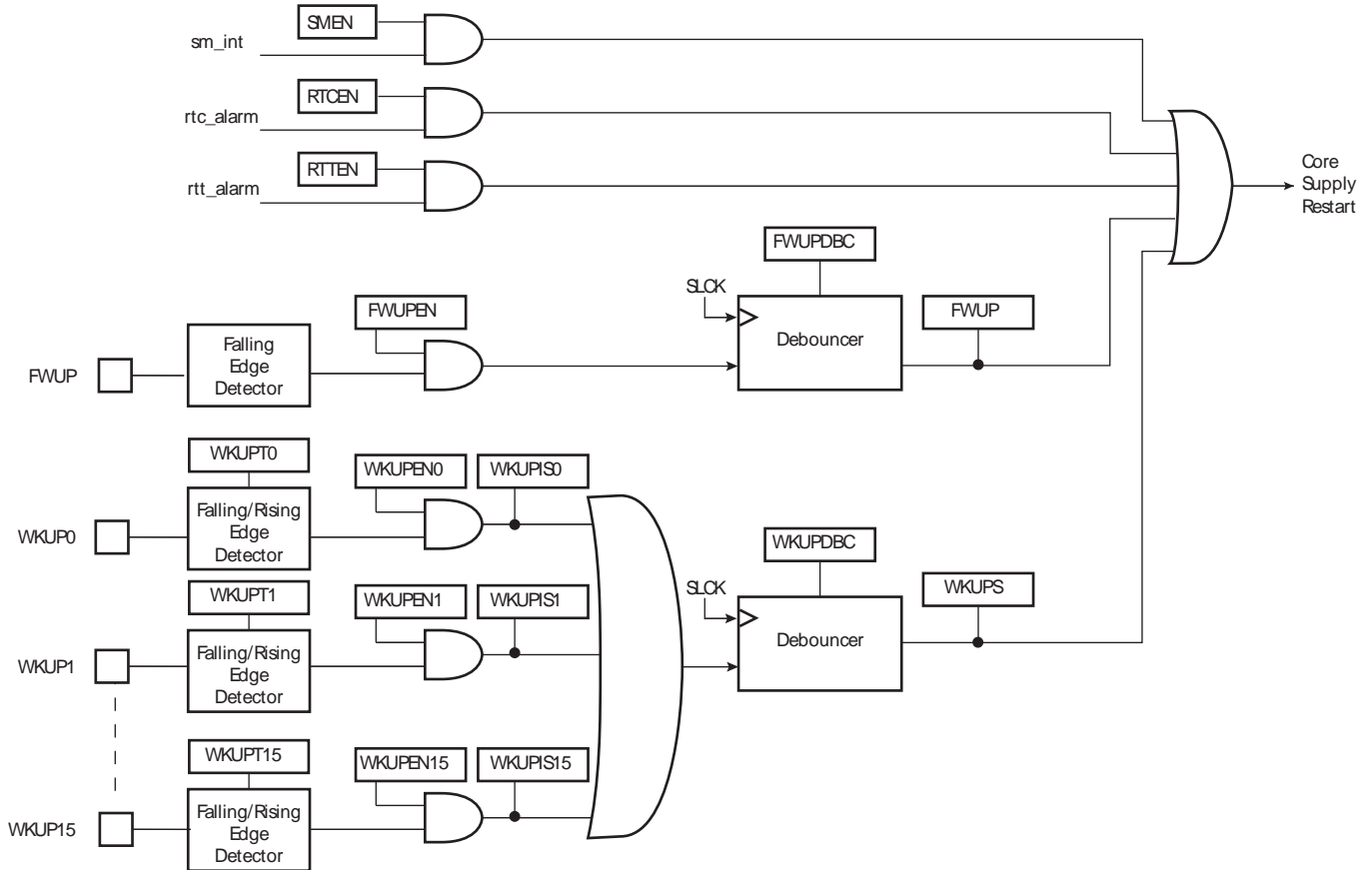
| Mode | VDDBU Region ⁽¹⁾ | Regulator | Core Memory Peripherals | Mode Entry | Potential Wake-up Sources | Core at Wake-up | PIO State while in Low Power Mode | PIO State at Wake-up | Consumption ^{(2) (3)} | Wake-up Time ⁽⁴⁾ |
|-------------|-----------------------------|----------------|---|--|---|-----------------|-----------------------------------|---|--|-----------------------------|
| Backup Mode | ON | OFF SHDN =0 | OFF (Not powered) | WFE +SLEEPDEEP bit = 1 | FWUP pin WKUP0-15 pins BOD alarm RTC alarm RTT alarm | Reset | Previous state saved | PIOA & PIOB & PIOC & PIOD & PIOE & PIOF Inputs with pull-ups | 2.5 μ A typ ⁽⁵⁾ | < 0.5 ms |
| Wait Mode | ON | ON SHDN =1 | Powered (Not clocked) | WFE +SLEEPDEEP bit = 0 +LPM bit = 1 | Any Event from: Fast startup through WKUP0-15 pins RTC alarm RTT alarm USB wake-up | Clocked back | Previous state saved | Unchanged | 18.4 μ A/26.6 μ A ⁽⁶⁾ | < 10 μ s |
| Sleep Mode | ON | ON SHDN =1 | Powered ⁽⁷⁾ (Not clocked) | WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0 | Entry mode = WFI Interrupt Only; Entry mode = WFE Any Enabled Interrupt and/or Any Event from Fast start-up through WKUP0-15 pins RTC alarm RTT alarm USB wake-up | Clocked back | Previous state saved | Unchanged ⁽⁷⁾ | ⁽⁷⁾ | ⁽⁷⁾ |

- Notes:
1. SUPC, 32 kHz Oscillator, RTC, RTT, Backup Registers, POR
 2. The external loads on PIOs are not taken into account in the calculation.
 3. BOD current consumption is not included.
 4. When considering the wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake-up until the first instruction is fetched
 5. Current consumption on VDDBU.
 6. 18.4 μ A on VDDCORE, 26.6 μ A for total current consumption (using internal voltage regulator).
 7. Depends on MCK frequency. In this mode, the core is supplied and not clocked but some peripherals can be clocked.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply.

Figure 5-3. Wake-up Source

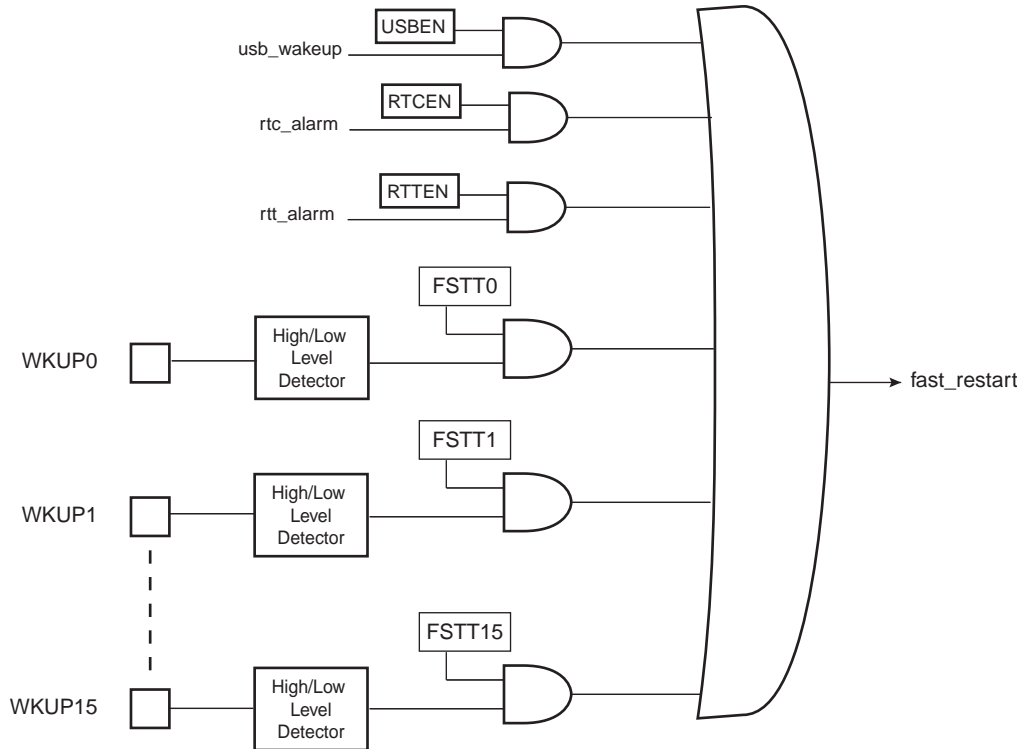


5.7 Fast Start-Up

The SAM3X/A series allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs.

The fast restart circuitry, as shown in [Figure 5-4](#), is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4/8/12 MHz fast RC oscillator, switches the master clock on this 4/8/12 MHz clock and reenables the processor clock.

Figure 5-4. Fast Start-Up Sources



6. Input/Output Lines

The SAM3X/A has different kinds of input/output (I/O) lines, such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functions thanks to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

With a few exceptions, the I/Os have input schmitt triggers. Refer to the footnotes associated with PIOA to PIOF on [page 14](#), at the end of [Table 3-1, “Signal Description List”](#).

6.1 General Purpose I/O Lines (GPIO)

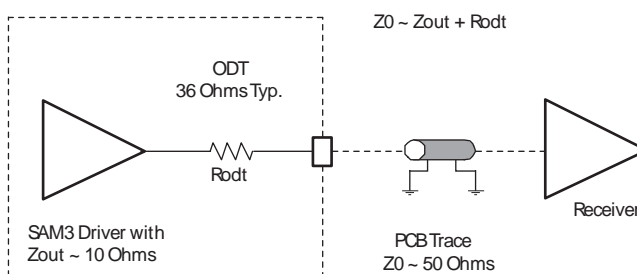
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up, input schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the “PIO Controller” section of the product datasheet.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3X/A embeds high speed pads able to handle up to 65 MHz for HSMCI and SPI clock lines and 45 MHz on other lines. See product AC Characteristics for more details. Typical pull-up value is 100 k Ω for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see [Figure 6-1](#) below). ODT consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3) and the PCB track impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion, ODT helps reducing signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset, flash erase and JTAG to name but a few. Described below are the SAM3X/A system I/O lines shared with PIO lines.

These pins are software configurable as general purpose I/O or system pins. At startup, the default function of these pins is always used.

Table 6-1. System I/O Configuration Pin List

| SYSTEM_IO Bit Number | Peripheral | Default Function After Reset | Other Function | Constraints for Normal Start | Configuration |
|----------------------|------------|------------------------------|----------------|-----------------------------------|--|
| 12 | - | ERASE | PC0 | Low Level at startup ⁰ | In Matrix User Interface Registers (Refer to “System IO Configuration Register” in the “Bus Matrix” section of the product datasheet.) |
| | A | TCK/SWCLK | PB28 | - | In PIO Controller |
| | A | TDI | PB29 | - | |
| | A | TDO/TRACESWO | PB30 | - | |
| | A | TMS/SWDIO | PB31 | - | |

Note: 1. If PC0 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PC0 into PIO mode.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to [Table 3-1](#).

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the “Debug and Test” section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users with more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the “Debug and Test” section of the product datasheet.

All JTAG signals are supplied with VDDIO except JTAGSEL, supplied by VDDBU.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3X/A series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the “Fast Flash Programming Interface” section. For more information on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components, or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length.

The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 k Ω .

6.5 NRSTB Pin

The NRSTB pin is input only and enables asynchronous reset of the SAM3X/A series when asserted low. The NRSTB pin integrates a permanent pull-up resistor of about 15 k Ω . This allows connection of a simple push button on the NRSTB pin as a system-user reset. In all modes, this pin will reset the chip including the Backup region (RTC, RTT and Supply Controller). It reacts as the Power-on reset. It can be used as an external system reset source. In harsh environments, it is recommended to add an external capacitor (10 nF) between NRSTB and VDDBU. (For filtering values, refer to “I/O characteristics” in the “Electrical Characteristics” section of the product datasheet)

It embeds an anti-glitch filter.

6.6 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 k Ω to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, the startup level of this pin must be low to prevent unwanted erasing. Please refer to [Section 11.2 “Peripheral Signal Multiplexing on I/O Lines”](#). Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB Bridge

The SAM3X/A series product embeds two separate APB/AHB bridges:

- a low speed bridge
- a high speed bridge

This architecture enables a concurrent access on both bridges.

SPI, SSC and HSMCI peripherals are on the high-speed bridge connected to DMAC with the internal FIFO for Channel buffering.

UART, ADC, TWI0-1, USART0-3, PWM, DAC and CAN peripherals are on the low-speed bridge and have dedicated channels for the Peripheral DMA Channels (PDC). Please note that USART0-1 can be used with the DMA as well.

The peripherals on the high speed bridge are clocked by MCK. On the low-speed bridge, CAN controllers can be clocked at MCK divided by 2 or 4. Refer to the Power Management Controller (PMC) section of the Full datasheet for further details.

7.3 Matrix Masters

The Bus Matrix of the SAM3X/A series product manages 5 (SAM3A) or 6 (SAM3X) masters, which means that each master can perform an access, concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

| | |
|----------|---------------------------------|
| Master 0 | Cortex-M3 Instruction/Data |
| Master 1 | Cortex-M3 System |
| Master 2 | Peripheral DMA Controller (PDC) |
| Master 3 | USB OTG High Speed DMA |
| Master 4 | DMA Controller |
| Master 5 | Ethernet MAC (SAM3X) |

7.4 Matrix Slaves

The Bus Matrix of the SAM3X/A series product manages 9 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

| | |
|---------|------------------------------------|
| Slave 0 | Internal SRAM0 |
| Slave 1 | Internal SRAM1 |
| Slave 2 | Internal ROM |
| Slave 3 | Internal Flash |
| Slave 4 | USB High Speed Dual Port RAM (DPR) |
| Slave 5 | NAND Flash Controller RAM |
| Slave 6 | External Bus Interface |
| Slave 7 | Low Speed Peripheral Bridge |
| Slave 8 | High Speed Peripheral Bridge |

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the USB High Speed DMA to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown as “-” in the following table.

Table 7-3. SAM3X/A Series Master to Slave Access

| Masters | | 0 | 1 | 2 | 3 | 4 | 5 |
|---------|------------------------------|-------------------|-----------------|-----|--------------------|----------------|----------|
| Slaves | | Cortex-M3 I/D Bus | Cortex-M3 S Bus | PDC | USB High Speed DMA | DMA Controller | EMAC DMA |
| 0 | Internal SRAM0 | - | X | X | X | X | X |
| 1 | Internal SRAM1 | - | X | X | X | X | X |
| 2 | Internal ROM | X | - | X | X | X | X |
| 3 | Internal Flash | X | - | - | - | - | - |
| 4 | USB High Speed Dual Port RAM | - | X | - | - | X | - |
| 5 | Nand Flash Controller RAM | - | X | X | X | X | X |
| 6 | External Bus Interface | - | X | X | X | X | X |
| 7 | Low Speed Peripheral Bridge | - | X | X | - | X | - |
| 8 | High Speed Peripheral Bridge | - | X | - | - | X | - |

7.6 DMA Controller

- Acting as one Matrix Master
- Embeds 4 (SAM3A and 100-pin SAM3X) or 6 (144-pin SAM3X) channels

Table 7-4. DMA Channels

| DMA Channel Size | SAM3A 100-pin SAM3X | 144-pin SAM3X |
|-------------------------------------|----------------------------|-------------------------------|
| 8 bytes FIFO for Channel Buffering | 3 (Channels 0, 1 and 2) | 4 (Channels 0, 1, 2 and 4) |
| 32 bytes FIFO for Channel Buffering | 1 (Channel 3) | 2 (Channels 3 and 5) |

- Linked List support with Status Write Back operation at End of Transfer
- Word, HalfWord, Byte transfer support.
- Handles high speed transfer of SPI0-1, USART0-1, SSC and HSMCI (peripheral to memory, memory to peripheral)
- Memory to memory transfer
- Can be triggered by PWM and T/C which enables to generates waveform though the External Bus Interface

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals below. The hardware interface numbers are also given in [Table 7-5](#).

Table 7-5. DMA Controller

| Instance Name | Channel T/R | DMA Channel HW Interface Number |
|---------------|------------------|---------------------------------|
| HSMCI | Transmit/Receive | 0 |
| SPI0 | Transmit | 1 |
| SPI0 | Receive | 2 |
| SSC | Transmit | 3 |
| SSC | Receive | 4 |
| SPI1 | Transmit | 5 |
| SPI1 | Receive | 6 |
| TWI0 | Transmit | 7 |
| TWI0 | Receive | 8 |
| - | - | - |
| - | - | - |
| USART0 | Transmit | 11 |
| USART0 | Receive | 12 |
| USART1 | Transmit | 13 |
| USART1 | Receive | 14 |
| PWM | Transmit | 15 |

7.7 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-6. Peripheral DMA Controller

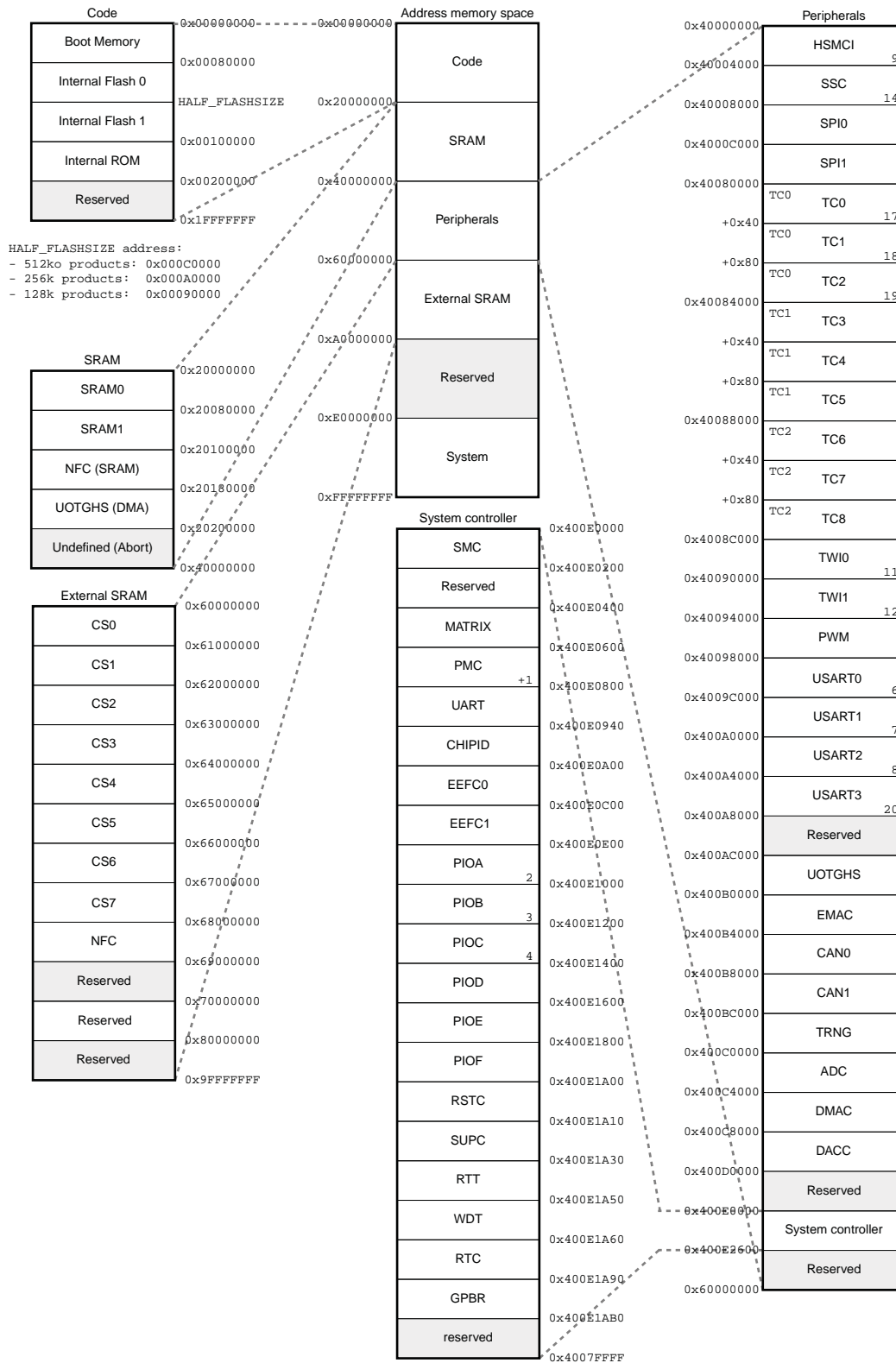
| Instance Name | Channel T/R | 144 Pins | 100 Pins |
|---------------|-------------|----------|----------|
| DAC | Transmit | X | X |
| PWM | Transmit | X | X |
| TWI1 | Transmit | X | X |
| TWI0 | Transmit | X | X |
| USART3 | Transmit | X | X |
| USART2 | Transmit | X | X |
| USART1 | Transmit | X | X |
| USART0 | Transmit | X | X |
| UART | Transmit | X | X |
| ADC | Receive | X | X |
| TWI1 | Receive | X | X |
| TWI0 | Receive | X | X |
| USART3 | Receive | X | N/A |
| USART2 | Receive | X | X |
| USART1 | Receive | X | X |
| USART0 | Receive | X | X |
| UART | Receive | X | X |

7.8 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing break points and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watch points, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE® 1149.1 JTAG Boundary-scan on all digital pins

8. Product Mapping

Figure 8-1. SAM3X/A Product Mapping



9. Memories

9.1 Embedded Memories

9.1.1 Internal SRAM

- The 100-pin SAM3A/X8 product embeds a total of 96 Kbytes high-speed SRAM (64 Kbytes SRAM0 and 32 Kbytes SRAM1).
- The 100-pin SAM3A/X4 product embeds a total of 64 Kbytes high-speed SRAM (32 Kbytes SRAM0, 32 Kbytes SRAM1).
- The 100-pin SAM3A/4 product embeds a total of 36 Kbytes high-speed SRAM (16 Kbytes SRAM0 and 16 Kbytes SRAM1).

The SRAM0 is accessible over System Cortex-M3 bus at address 0x2000 0000 and SRAM1 at address 0x2008 0000. The user can see the SRAM as contiguous thanks to mirror effect, giving 0x2007 0000 - 0x2008 7FFF for SAM3X/A8, 0x2007 8000 - 0x2008 7FFF for SAM3X/A4 and 0x2007 C000 - 0x2008 3FFF for SAM3X/A2.

The SRAM0 and SRAM1 are in the bit band region. The bit band alias region is mapped from 0x2200 0000 to 0x23FF FFFF.

The NAND Flash Controller embeds 4224 bytes of internal SRAM. If the NAND Flash controller is not used, these 4224 Kbytes of SRAM can be used as general purpose. It can be seen at address 0x2010 0000.

9.1.2 Internal ROM

The SAM3X/A series product embeds an Internal ROM, which contains the SAM-BA and FFPI program.

At any time, the ROM is mapped at address 0x0018 0000.

9.1.3 Embedded Flash

9.1.3.1 Flash Overview

- The Flash of the ATSAM3A/X8 is organized in two banks of 1024 pages (dual plane) of 256 bytes.
- The Flash of the ATSAM3A/X4 is organized in two banks of 512 pages (dual plane) of 256 bytes.

The Flash contains a 128-byte write buffer, accessible through a 32-bit interface.

9.1.3.2 Flash Power Supply

The Flash is supplied by VDDCORE.

9.1.3.3 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block with the 32-bit internal bus. Its 128-bit wide memory interface increases performance.

The user can choose between high performance or lower current consumption by selecting either 128-bit or 64-bit access. It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

9.1.3.4 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Number of Lock Bits

| Product | Number of Lock Bits | Lock Region Size |
|------------|---------------------|----------------------|
| ATSAM3X/A8 | 32 | 16 kbytes (64 pages) |
| ATSAM3X/A4 | 16 | 16 kbytes (64 pages) |

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The "Set Lock Bit" command enables the protection. The "Clear Lock Bit" command unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.5 Security Bit Feature

The SAM3X/A series features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled through the "Set General Purpose NVM Bit 0" command of the EEFC0 User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.6 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.7 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.8 Fast Flash Programming Interface

The Fast Flash Programming Interface allows device programming through multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST, PA0, PA1 are set to high, PA2 and PA3 are set to low and NRST is toggled from 0 to 1.

The table below shows the signal assignment of the PIO lines in FFPI mode

Table 9-2. FFPI PIO Assignment

| FFPI Signal | PIO Used |
|-------------|----------|
| PGMNCMD | PA0 |
| PGMRDY | PA1 |
| PGMNOE | PA2 |
| PGMNVALID | PA3 |
| PGMM[0] | PA4 |
| PGMM[1] | PA5 |
| PGMM[2] | PA6 |
| PGMM[3] | PA7 |
| PGMD[0] | PA8 |
| PGMD[1] | PA9 |
| PGMD[2] | PA10 |
| PGMD[3] | PA11 |
| PGMD[4] | PA12 |
| PGMD[5] | PA13 |
| PGMD[6] | PA14 |
| PGMD[7] | PA15 |
| PGMD[8] | PA16 |
| PGMD[9] | PA17 |
| PGMD[10] | PA18 |
| PGMD[11] | PA19 |
| PGMD[12] | PA20 |
| PGMD[13] | PA21 |
| PGMD[14] | PA22 |
| PGMD[15] | PA23 |

9.1.3.9 SAM-BA[®] Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

9.1.3.10 GPNVM Bits

The SAM3X/A series features three GPNVM bits that can be cleared or set respectively through the "Clear GPNVM Bit" and "Set GPNVM Bit" commands of the EEFC0 User Interface.

Table 9-3. General Purpose Non-volatile Memory Bits

| GPNVMBit[#] | Function |
|-------------|--------------------------------------|
| 0 | Security bit |
| 1 | Boot mode selection |
| 2 | Flash selection (Flash 0 or Flash 1) |

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general-purpose NVM (GPNVM1) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the "Clear General-purpose NVM Bit" and "Set General-purpose NVM Bit" commands of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears GPNVM Bit 1 and thus selects the boot from the ROM by default.

GPNVM2 enables to select if Flash 0 or Flash 1 is used for the boot.

Setting GPNVM bit 2 selects the boot from Flash 1, clearing it selects the boot from Flash 0.

9.2 External Memories

The 144-pin SAM3X features one External Memory Bus to offer interface to a wide range of external memories and to any parallel peripheral.

9.2.1 External Memory Bus

- Integrates Four External Memory Controllers:
 - Static Memory Controller
 - NAND Flash Controller
 - SLC NAND Flash ECC Controller
- Up to 24-bit Address Bus (up to 16 MBytes linear per chip select)
- Up to 8 chip selects, Configurable Assignment

9.2.2 Static Memory Controller

- 8- or 16-bit Data Bus
- Multiple Access Modes supported
 - Byte Write or Byte Select Lines
 - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
 - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
 - Programmable Wait State Generation
 - External Wait Request
 - Programmable Data Float Time
- Slow Clock mode supported

9.2.3 NAND Flash Controller

- Handles automatic Read/write transfer through 4224 bytes SRAM buffer
- DMA support
- Supports SLC NAND Flash technology
- Programmable timing on a per chip select basis
- Programmable Flash Data width 8-bit or 16-bit

9.2.4 NAND Flash Error Corrected Code Controller

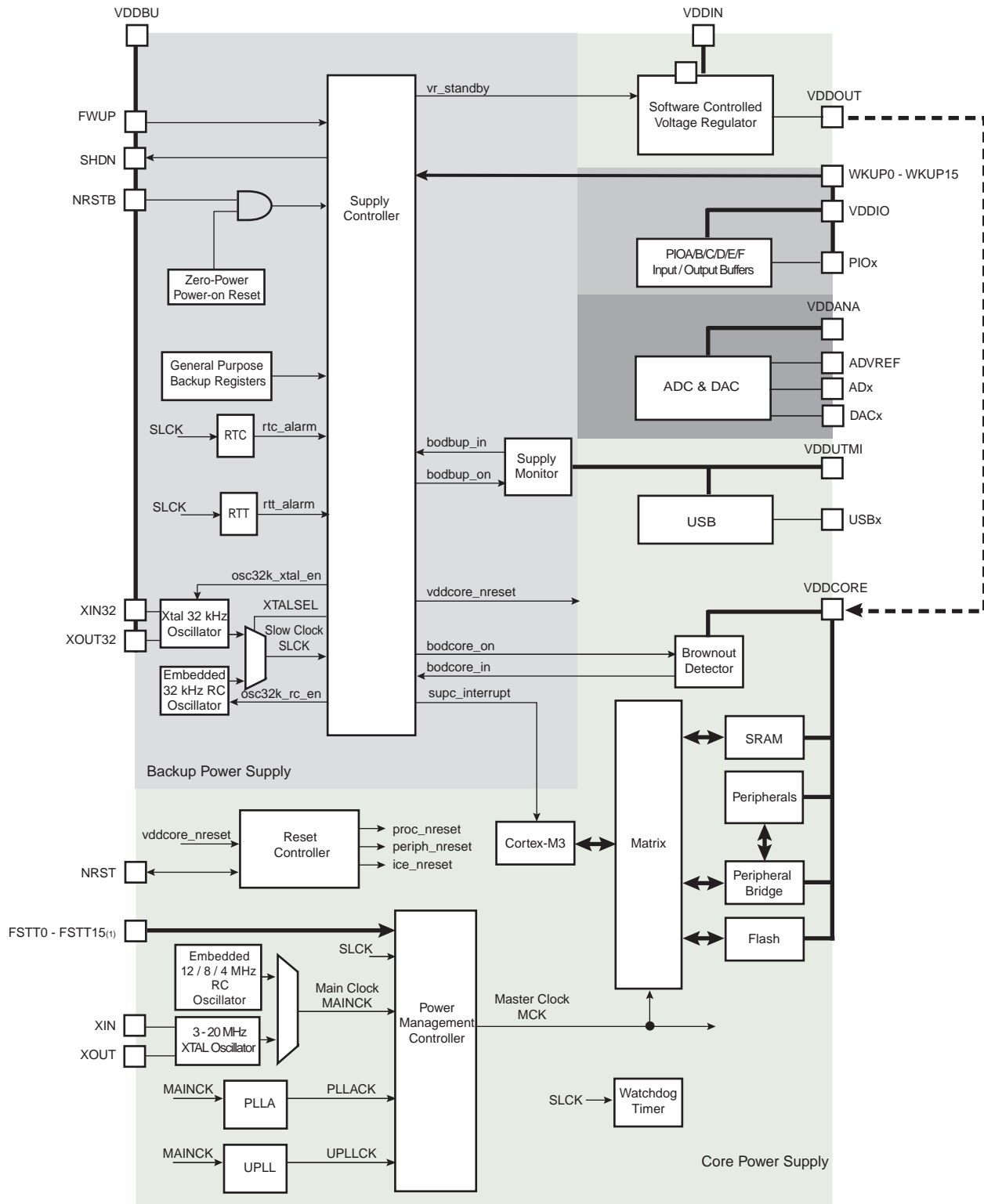
- Integrated in the NAND Flash Controller
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
 - ECC value available in a register
- Automatic Hamming Code Calculation while reading
 - Error Report, including error flag, correctable error flag and word address being detected erroneous
 - Support 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system such as power, resets, clocks, time, interrupts, watchdog, etc...

The System Controller User Interface also embeds the registers allowing to configure the Matrix.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

10.1 System Controller and Peripherals Mapping

Please refer to [Figure 8-1 on page 37](#).

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3X/A embeds three features to monitor, warn and/or reset the chip:

- Power-on-Reset on VDDBU
- Brownout Detector on VDDCORE
- Supply Monitor on VDDUTMI

10.2.1 Power-on-Reset on VDDBU

The Power-on-Reset monitors VDDBU. It is always activated and monitors voltage at start up but also during power down. If VDDBU goes below the threshold voltage, the entire chip is reset. For more information, refer to the “Electrical Characteristics” section of the product datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the “Supply Controller” and “Electrical Characteristics” sections of the product datasheet.

10.2.3 Supply Monitor on VDDUTMI

The Supply Monitor monitors VDDUTMI. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the “SUPC” and “Electrical Characteristics” sections of the product datasheet.

10.3 Reset Controller

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

10.4 Supply Controller

The Supply Controller controls the power supplies of each section of the processor and peripherals (via Voltage regulator control).

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell. The zero-power power-on reset allows the Supply Controller to start properly.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by enabling the Voltage Regulator, then it generates the proper reset signals to the core power supply.

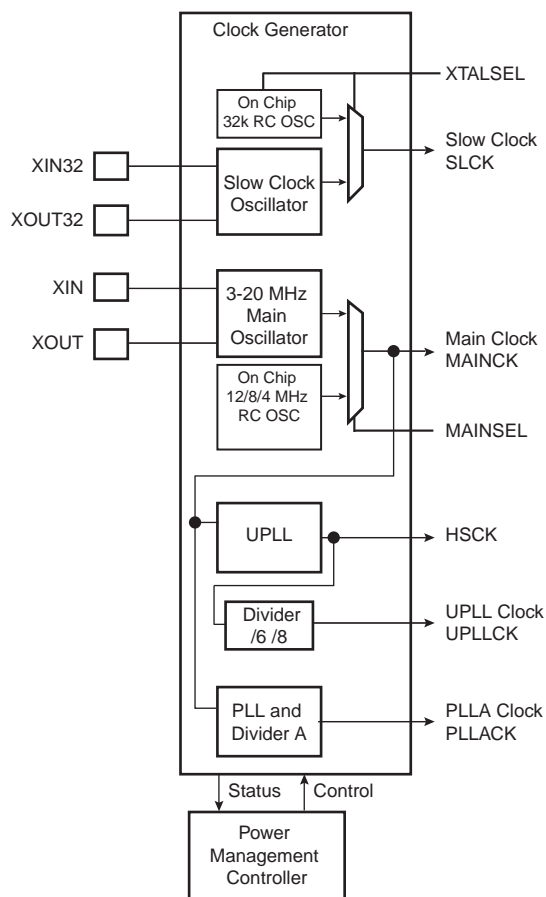
It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32,768 Hz Slow Clock Oscillator with bypass mode
- One Low Power RC Oscillator
- One 3 to 20 MHz Crystal or Ceramic-based Oscillator, which can be bypassed
- One factory-programmed Fast RC Oscillator; 3 output frequencies can be selected: 4, 8 or 12 MHz. By default, 4 MHz is selected. 8 MHz and 12 MHz output are factory-calibrated.
- One 480 MHz UPLL providing a clock for the USB OTG High Speed Controller. Input frequency is 12 MHz (only).
- One 96 to 192 MHz programmable PLL (PLLA), capable to provide the clock MCK to the processor and to the peripherals. The input frequency of the PLL A is between 8 and 16 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

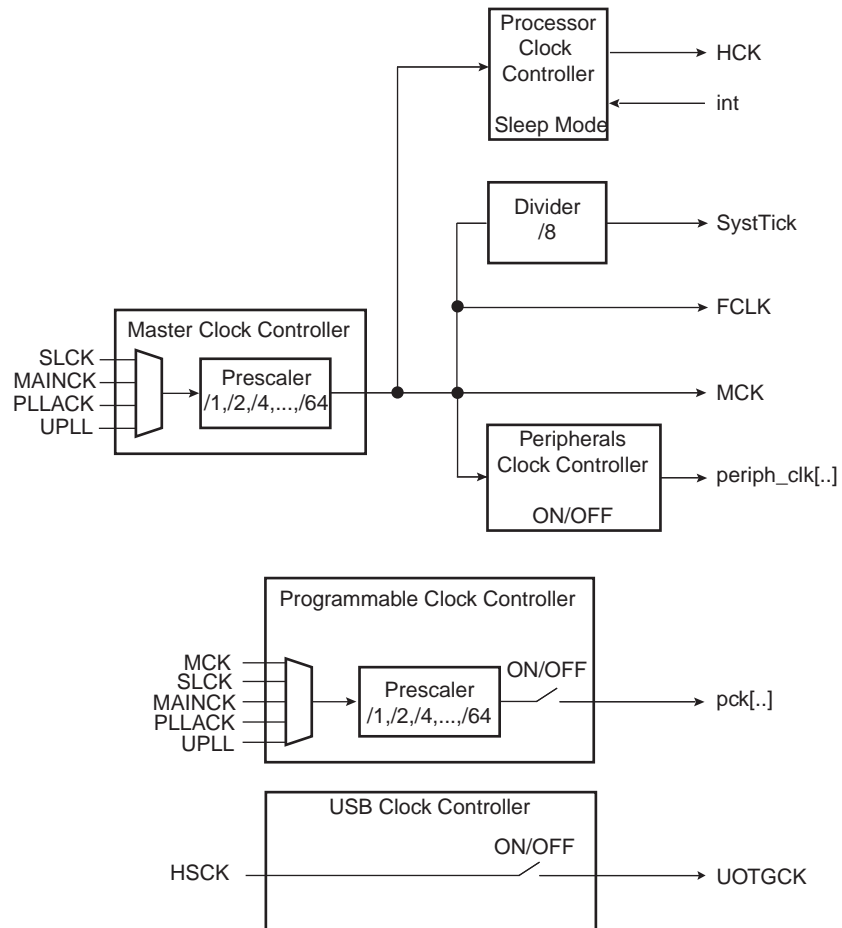
The Power Management Controller provides all the clock signals to the system. It provides:

- the Processor Clock HCLK
- the Free running processor clock FCLK
- the Cortex SysTick external clock
- the Master Clock MCK, in particular to the Matrix and the memory interfaces
- the USB OTG HS Clock UOTGCK
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the Fast RC Oscillator running at 4 MHz.

Figure 10-3. Power Management Controller Block Diagram



The SysTick calibration value is fixed at 10500, which allows the generation of a time base of 1 ms with SysTick clock to 10.5 MHz (max HCLK/8).

10.7 Watchdog Timer

- 16-bit key-protected once-only Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

10.8 SysTick Timer

- 24-bit down counter
- Self-reload capability
- Flexible system timer

10.9 Real Time Timer

- Real Time Timer, allowing backup of time with different accuracies
 - 32-bit Free-running back-up Counter
 - Integrates a 16-bit programmable prescaler running on slow clock
 - Alarm Register capable to generate a wake-up of the system

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General-Purpose Backup Registers

- Eight 32-bit general-purpose backup registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable interrupts
- Sixteen priority levels
- Dynamic reprioritization of interrupts
- Priority grouping
 - selection of preempting interrupt levels and non preempting interrupt levels.
- Support for tail-chaining and late arrival of interrupts.
 - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.
- .JTAG ID: 0x05B2B03F

Table 10-1. ATSAM3A/X Chip IDs Register

| Chip Name | CHIPID_CIDR | CHIPID_EXID |
|-------------------|-------------|-------------|
| ATSAM3X8H (Rev A) | 0x286E0A60 | 0x0 |
| ATSAM3X8E (Rev A) | 0x285E0A60 | 0x0 |
| ATSAM3X4E (Rev A) | 0x285B0960 | 0x0 |
| ATSAM3X8C (Rev A) | 0x284E0A60 | 0x0 |
| ATSAM3X4C (Rev A) | 0x284B0960 | 0x0 |
| ATSAM3A8C (Rev A) | 0x283E0A60 | 0x0 |
| ATSAM3A4C (Rev A) | 0x283B0960 | 0x0 |

10.14 UART

- Two-pin UART
 - Implemented features are 100% compatible with the standard Atmel USART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
 - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- Up to 6 PIO Controllers, PIOA, PIOB, PIOC, PIOD, PIOE and PIOF controlling a maximum of 167 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines

Table 10-2. PIO Lines per PIO according to Version

| Version | 100 pin SAM3X/A | 144 pin SAM3X |
|---------|-----------------|---------------|
| PIOA | 30 | |
| PIOB | 32 | |
| PIOC | 1 | 31 |
| PIOD | - | 10 |
| PIOE | - | - |
| PIOF | - | - |
| Total | 63 | 103 |

- Fully programmable through Set/Clear Registers
- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
 - Input change, rising edge, falling edge, low level and level interrupt
 - Debouncing and Glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3X/A series. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Note that some Peripherals are always clocked. Please refer to the table below.

Table 11-1. Peripheral Identifiers

| Instance ID | Instance Name | NVIC Interrupt | PMC Clock Control | Instance Description |
|-------------|---------------|----------------|-------------------|---|
| 0 | SUPC | X | | Supply Controller |
| 1 | RSTC | X | | Reset Controller |
| 2 | RTC | X | | Real Time Clock |
| 3 | RTT | X | | Real Time Timer |
| 4 | WDG | X | | Watchdog Timer |
| 5 | PMC | X | | Power Management Controller |
| 6 | EEFC0 | X | | Enhanced Flash Controller 0 |
| 7 | EEFC1 | X | | Enhanced Flash Controller 1 |
| 8 | UART | X | | Universal Asynchronous Receiver Transceiver |
| 9 | SMC | X | X | Static Memory Controller |
| 10 | | | | Reserved |
| 11 | PIOA | X | X | Parallel I/O Controller A, |
| 12 | PIOB | X | X | Parallel I/O Controller B |
| 13 | PIOC | X | X | Parallel I/O Controller C |
| 14 | PIOD | X | X | Parallel I/O Controller D |
| 15 | PIOE | X | X | Parallel I/O Controller E |
| 16 | PIOF | X | X | Parallel I/O Controller F |
| 17 | USART0 | X | X | USART 0 |
| 18 | USART1 | X | X | USART 1 |
| 19 | USART2 | X | X | USART 2 |
| 20 | USART3 | X | X | USART 3 |
| 21 | HSMCI | X | X | Multimedia Card Interface |
| 22 | TWI0 | X | X | Two-Wire Interface 0 |
| 23 | TWI1 | X | X | Two-Wire Interface 1 |
| 24 | SPI0 | X | X | Serial Peripheral Interface |
| 25 | SPI1 | X | X | Serial Peripheral Interface |
| 26 | SSC | X | X | Synchronous Serial Controller |
| 27 | TC0 | X | X | Timer Counter 0 |
| 28 | TC1 | X | X | Timer Counter 1 |
| 29 | TC2 | X | X | Timer Counter 2 |

Table 11-1. Peripheral Identifiers (Continued)

| Instance ID | Instance Name | NVIC Interrupt | PMC Clock Control | Instance Description |
|-------------|---------------|----------------|-------------------|-----------------------------------|
| 30 | TC3 | X | X | Timer Counter 3 |
| 31 | TC4 | X | X | Timer Counter 4 |
| 32 | TC5 | X | X | Timer Counter 5 |
| 33 | TC6 | X | X | Timer Counter 6 |
| 34 | TC7 | X | X | Timer Counter 7 |
| 35 | TC8 | X | X | Timer Counter 8 |
| 36 | PWM | X | X | Pulse Width Modulation Controller |
| 37 | ADC | X | X | ADC Controller |
| 38 | DACC | X | X | DAC Controller |
| 39 | DMAC | X | X | DMA Controller |
| 40 | UOTGHS | X | X | USB OTG High Speed |
| 41 | TRNG | X | X | True Random Number Generator |
| 42 | EMAC | X | X | Ethernet MAC |
| 43 | CAN0 | X | X | CAN Controller 0 |
| 44 | CAN1 | X | X | CAN Controller 1 |

11.2 Peripheral Signal Multiplexing on I/O Lines

The SAM3X/A series product features 3 PIO (SAM3A and 100-pin SAM3X) or 4 PIO (144-pin SAM3X) controllers, PIOA, PIOB, PIOC, PIOD, PIOE and PIOF, which multiplexes the I/O lines of the peripheral set.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral function, which are output only, might be duplicated within both tables.

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

| I/O Line | Peripheral A | Peripheral B | Extra Function | Comments |
|----------|--------------|--------------|----------------|----------|
| PA0 | CANTX0 | PWML3 | | |
| PA1 | CANRX0 | PCK0 | WKUP0 | |
| PA2 | TIOA1 | NANDRDY | AD0 | |
| PA3 | TIOB1 | PWMF11 | AD1/WKUP1 | |
| PA4 | TCLK1 | NWAIT | AD2 | |
| PA5 | TIOA2 | PWMF10 | WKUP2 | |
| PA6 | TIOB2 | NCS0 | AD3 | |
| PA7 | TCLK2 | NCS1 | WKUP3 | |
| PA8 | URXD | PWMH0 | WKUP4 | |
| PA9 | UTXD | PWMH3 | | |
| PA10 | RXD0 | DATRG | WKUP5 | |
| PA11 | TXD0 | ADTRG | WKUP6 | |
| PA12 | RXD1 | PWML1 | WKUP7 | |
| PA13 | TXD1 | PWMH2 | | |
| PA14 | RTS1 | TK | | |
| PA15 | CTS1 | TF | WKUP8 | |
| PA16 | SCK1 | TD | AD7 | |
| PA17 | TWD0 | SCK0 | | |
| PA18 | TWCK0 | A20 | WKUP9 | |
| PA19 | MCCK | PWMH1 | | |
| PA20 | MCCDA | PWML2 | | |
| PA21 | MCDA0 | PWML0 | | |
| PA22 | MCDA1 | TCLK3 | AD4 | |
| PA23 | MCDA2 | TCLK4 | AD5 | |
| PA24 | MCDA3 | PCK1 | AD6 | |
| PA25 | SPI0_MISO | A18 | | |
| PA26 | SPI0_MOSI | A19 | | |
| PA27 | SPI0_SPCK | A20 | WKUP10 | |
| PA28 | SPI0_NPCS0 | PCK2 | WKUP11 | |
| PA29 | SPI0_NPCS1 | NRD | | |
| PA30 | SPI0_NPCS2 | PCK1 | | |
| PA31 | SPI0_NPCS3 | PCK2 | | |

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

| I/O Line | Peripheral A | Peripheral B | Extra Function | Comments |
|----------|-----------------------------|----------------------|----------------|-----------------|
| PB0 | ETXCK/EREFCK ⁽¹⁾ | TIOA3 ⁽²⁾ | | See the Notes |
| PB1 | ETXEN ⁽¹⁾ | TIOB3 ⁽²⁾ | | See the Notes |
| PB2 | ETX0 ⁽¹⁾ | TIOA4 ⁽²⁾ | | See the Notes |
| PB3 | ETX1 ⁽¹⁾ | TIOB4 ⁽²⁾ | | See the Notes |
| PB4 | ECRSDV/ERXDV ⁽¹⁾ | TIOA5 ⁽²⁾ | | See the Notes |
| PB5 | ERX0 ⁽¹⁾ | TIOB5 ⁽²⁾ | | See the Notes |
| PB6 | ERX1 ⁽¹⁾ | PWML4 ⁽²⁾ | | See the Notes |
| PB7 | ERXER ⁽¹⁾ | PWML5 ⁽²⁾ | | See the Notes |
| PB8 | EMDC ⁽¹⁾ | PWML6 ⁽²⁾ | | See the Notes |
| PB9 | EMDIO ⁽¹⁾ | PWML7 ⁽²⁾ | | See the Notes |
| PB10 | UOTGVBOF | A18 | | |
| PB11 | UOTGID | A19 | | |
| PB12 | TWD1 | PWMH0 | AD8 | |
| PB13 | TWCK1 | PWMH1 | AD9 | |
| PB14 | CANTX1 | PWMH2 | | |
| PB15 | CANRX1 | PWMH3 | DAC0/WKUP12 | |
| PB16 | TCLK5 | PWML0 | DAC1 | |
| PB17 | RF | PWML1 | AD10 | |
| PB18 | RD | PWML2 | AD11 | |
| PB19 | RK | PWML3 | AD12 | |
| PB20 | TXD2 | SPI0_NPCS1 | AD13 | |
| PB21 | RXD2 | SPI0_NPCS2 | AD14/WKUP13 | |
| PB22 | RTS2 | PCK0 | | |
| PB23 | CTS2 | SPI0_NPCS3 | WKUP14 | |
| PB24 | SCK2 | NCS2 | | |
| PB25 | RTS0 | TIOA0 | | |
| PB26 | CTS0 | TCLK0 | WKUP15 | |
| PB27 | NCS3 | TIOB0 | | |
| PB28 | TCK/SWCLK | | | TCK after reset |
| PB29 | TDI | | | TDI after reset |
| PB30 | TDO/TRACESWO | | | TDO after reset |
| PB31 | TMS/SWDIO | | | TMS after reset |

Notes: 1. SAM3X only
2. SAM3A only

11.2.3 PIO Controller C Multiplexing

Table 11-4. Multiplexing on PIO Controller C (PIOC)

| I/O Line | Peripheral A | Peripheral B | Extra Function | Comments |
|----------|--------------|--------------|----------------|----------|
| PC0 | | | ERASE | |
| PC1 | | | | 144 pins |
| PC2 | D0 | PWML0 | | 144 pins |
| PC3 | D1 | PWMH0 | | 144 pins |
| PC4 | D2 | PWML1 | | 144 pins |
| PC5 | D3 | PWMH1 | | 144 pins |
| PC6 | D4 | PWML2 | | 144 pins |
| PC7 | D5 | PWMH2 | | 144 pins |
| PC8 | D6 | PWML3 | | 144 pins |
| PC9 | D7 | PWMH3 | | 144 pins |
| PC10 | D8 | ECS | | 144 pins |
| PC11 | D9 | ERX2 | | 144 pins |
| PC12 | D10 | ERX3 | | 144 pins |
| PC13 | D11 | ECOL | | 144 pins |
| PC14 | D12 | ERXCK | | 144 pins |
| PC15 | D13 | ETX2 | | 144 pins |
| PC16 | D14 | ETX3 | | 144 pins |
| PC17 | D15 | ETXER | | 144 pins |
| PC18 | NWR0/NWE | PWMH6 | | 144 pins |
| PC19 | NANDOE | PWMH5 | | 144 pins |
| PC20 | NANDWE | PWMH4 | | 144 pins |
| PC21 | A0/NBS0 | PWML4 | | 144 pins |
| PC22 | A1 | PWML5 | | 144 pins |
| PC23 | A2 | PWML6 | | 144 pins |
| PC24 | A3 | PWML7 | | 144 pins |
| PC25 | A4 | TIOA6 | | 144 pins |
| PC26 | A5 | TIOB6 | | 144 pins |
| PC27 | A6 | TCLK6 | | 144 pins |
| PC28 | A7 | TIOA7 | | 144 pins |
| PC29 | A8 | TIOB7 | | 144 pins |
| PC30 | A9 | TCLK7 | | 144 pins |

11.2.4 PIO Controller D Multiplexing

Table 11-5. Multiplexing on PIO Controller D (PIOD)

| I/O Line | Peripheral A | Peripheral B | Extra Function | Comments |
|----------|--------------|--------------|----------------|----------|
| PD0 | A10 | MCDA4 | | 144 pins |
| PD1 | A11 | MCDA5 | | 144 pins |
| PD2 | A12 | MCDA6 | | 144 pins |
| PD3 | A13 | MCDA7 | | 144 pins |
| PD4 | A14 | TXD3 | | 144 pins |
| PD5 | A15 | RXD3 | | 144 pins |
| PD6 | A16 | PWMFI2 | | 144 pins |
| PD7 | A17 | TIOA8 | | 144 pins |
| PD8 | A21/NANDALE | TIOB8 | | 144 pins |
| PD9 | A22/NANDCLE | TCLK8 | | 144 pins |
| PD10 | NWR1/NBS1 | | | 144 pins |
| PD11 | | | | |
| PD12 | | | | |
| PD13 | | | | |
| PD14 | | | | |
| PD15 | | | | |
| PD16 | | | | |
| PD17 | A5 | | | |
| PD18 | A6 | | | |
| PD19 | A7 | | | |
| PD20 | A8 | | | |
| PD21 | A9 | | | |
| PD22 | A10 | | | |
| PD23 | A11 | | | |
| PD24 | A12 | | | |
| PD25 | A13 | | | |
| PD26 | A14 | | | |
| PD27 | A15 | | | |
| PD28 | A16 | | | |
| PD29 | A17 | | | |
| PD30 | A18 | | | |

11.2.5 PIO Controller E Multiplexing

Table 11-6. Multiplexing on PIO Controller E (PIOE)

| I/O Line | Peripheral A | Peripheral B | Extra Function | Comments |
|----------|--------------|--------------|----------------|----------|
| PE0 | A19 | | | |
| PE1 | A20 | | | |
| PE2 | A21/NANDALE | | | |
| PE3 | A22/NANDCLE | | | |
| PE4 | A23 | | | |
| PE5 | NCS4 | | | |
| PE6 | NCS5 | | | |
| PE7 | | | | |
| PE8 | | | | |
| PE9 | TIOA3 | | | |
| PE10 | TIOB3 | | | |
| PE11 | TIOA4 | | | |
| PE12 | TIOB4 | | | |
| PE13 | TIOA5 | | | |
| PE14 | TIOB5 | | | |
| PE15 | PWMH0 | | | |
| PE16 | PWMH1 | SCK3 | | |
| PE17 | PWML2 | | | |
| PE18 | PWML0 | NCS6 | | |
| PE19 | PWML4 | | | |
| PE20 | PWMH4 | MCCDB | | |
| PE21 | PWML5 | | | |
| PE22 | PWMH5 | MCDB0 | | |
| PE23 | PWML6 | | | |
| PE24 | PWMH6 | MCDB1 | | |
| PE25 | PWML7 | | | |
| PE26 | PWMH7 | MCDB2 | | |
| PE27 | NCS7 | MCDB3 | | |
| PE28 | SPI1_MISO | | | |
| PE29 | SPI1_MOSI | | | |
| PE30 | SPI1_SPCK | | | |
| PE31 | SPI1_NPCS0 | | | |

11.2.6 PIO Controller F Multiplexing

Table 11-7. Multiplexing on PIO Controller F (PIOF)

| I/O Line | Peripheral A | Peripheral B | Extra Function | Comments |
|----------|--------------|--------------|----------------|----------|
| PF0 | SPI1_NPCS1 | | | |
| PF1 | SPI1_NPCS2 | | | |
| PF2 | SPI1_NPCS3 | | | |
| PF3 | PWMH3 | | | |
| PF4 | CTS3 | | | |
| PF5 | RTS3 | | | |

12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
 - Four chip selects with external decoder support allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays between consecutive transfers and between clock and data per chip select
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
- Very fast transfers supported
 - Transfers with baud rates up to MCK
 - The chip select line may be left active to speed up transfers on the same device
 - Four Character FIFO in Reception
- Connection to DMA Channel Capabilities Optimizes Data Transfers
 - One channel for the Receiver, One Channel for the Transmitter

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I²C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: up to 400 kbit/s
- General Call Supported in Slave Mode
- SMBUS Quick Command Supported in Master Mode
- Connection to Peripheral DMA Controller (PDC) for TWI0 and TWI1 and DMA Controller (DMAC) for TWI0 Channel Capabilities Optimizes Data Transfers in Master Mode Only

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes

- Support for two PDC channels with connection to receiver and transmitter
- Connection to Peripheral DMA Controller or DMA Controller (TWI0) Channel Capabilities Optimizes Data Transfers

12.4 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode, or 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB- or LSB-first
 - Optional break generation and detection
 - By 8 or by-16 over-sampling receiver frequency
 - Hardware handshaking RTS-CTS
 - Receiver time-out and transmitter timeguard
 - Optional Multi-drop Mode with address generation and detection
 - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- SPI Mode
 - Master or Slave
 - Serial Clock programmable Phase and Polarity
 - SPI Serial Clock (SCK) Frequency up to MCK/6
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- LIN Mode (USART0 only)
 - Compliant with LIN 1.3 and LIN 2.0 specifications
 - Master or Slave
 - Processing of frames with up to 256 data bytes
 - Response Data length can be configurable or defined automatically by the Identifier
 - Self synchronization in Slave node configuration
 - Automatic processing and verification of the “Synch Break” and the “Synch Field”
 - The “Synch Break” is detected even if it is partially superimposed with a data byte
 - Automatic Identifier parity calculation/sending and verification
 - Parity sending and verification can be disabled
 - Automatic Checksum calculation/sending and verification
 - Checksum sending and verification can be disabled
 - Support both “Classic” and “Enhanced” checksum types
 - Full LIN error checking and reporting
 - Frame Slot Mode: the Master allocates slots to the scheduled frames automatically

- Generation of the Wakeup signal
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo
- Interfaced with Peripheral DMA (PDC) Channels to Reduce Processor Overhead (All USARTs) and with the DMA Controller (DMAC) (USART0 and 1)

12.5 Serial Synchronous Controller (SSC)

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I²S, TDM Buses, Magnetic Card Reader,...)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal
- Interfaced with the DMA Controller (DMAC) to Reduce Processor Overhead

12.6 Timer Counter (TC)

- Three 32-bit Timer Counter Channels
- Wide range of functions including:
 - Frequency Measurement
 - Event Counting
 - Interval Measurement
 - Pulse Generation
 - Delay Timing
 - Pulse Width Modulation
 - Up/down Capabilities
- Each channel is user-configurable and can contain:
 - Three external clock inputs
 - Five internal clock inputs
 - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
 - Advanced line filtering
 - Position / revolution / speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.7 Pulse Width Modulation Controller (PWM)

- One Eight-channel (SAM3A and 144-pin SAM3X) or One Four-channel (100-pin SAM3X) 16-bit PWM Controller, 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
 - A Modulo n counter providing eleven clocks
 - Two independent Linear Dividers working on modulo n counter outputs
 - High Frequency Asynchronous clocking mode
- Independent channel programming
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Bufferization
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform
 - Independent Output Override for each channel
 - Independent complementary Outputs with 12-bit dead time generator for each channel
 - Independent Enable Disable Commands
 - Independent Clock Selection
 - Independent Period and Duty Cycle, with Double Bufferization
- Synchronous Channel mode
 - Synchronous Channels share the same counter
 - Mode to update the synchronous channels registers after a programmable number of periods
- Interfaced with Peripheral DMA (PDC) or with the DMA Controller (DMAC) Channels to Reduce Processor Overhead
- Two independent event lines which can send up to 4 triggers on ADC within a period
- Three programmable external (PWMPFix pins) and three internal (from ADC, PMC controller and Timer 0) Fault Inputs providing an asynchronous protection of outputs without MCU intervention
- Stepper motor control (2 Channels)

12.8 High Speed Multimedia Card Interface (HSMCI)

- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V2.0
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- Supports 2 Multiplexed Slot(s)

- Each Slot for either a High Speed MultiMediaCard Bus (Up to 30 Cards) or an SD Memory Card
- Support for Stream, Block and Multi-block Data Read and Write
- Supports Connection to DMA Controller (DMAC)
 - Minimizes Processor Intervention for Large Buffer Transfers
- Built in FIFO (from 16 to 256 bytes) with Large Memory Aperture Supporting Incremental Access
- Support for CE-ATA Completion Signal Disable Command
- Protection Against Unexpected Modification On-the-Fly of the Configuration Registers

12.9 USB On-The-Go High Speed Port (UOTGHS)

- USB2.0 Compliant, Low/Full/High-Speed (LS/FS/HS) and On-The-Go, 1.5Mb/s, 12Mb/s, 480Mb/s
- 10 Pipes/Endpoints
- 4K bytes of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints
- Up to 2 Memory Banks per Pipe/Endpoint (Not for Control Pipe/Endpoint)
- Flexible Pipe/Endpoint Configuration and Management with 6 Dedicated DMA Channels
- On-Chip UTMI transceiver including Pull-ups/Pull-downs
- On-Chip OTG pad including VBUS analog comparator

12.10 Analog-to-Digital Converter (ADC)

- 12-bit Resolution
- 1 MHz Conversion Rate
- 2.4 V to 3.6 V Wide Range Power Supply Operation
- Selectable Single Ended or Differential Input Voltage
- Programmable Gain and Offset per channel For Maximum Full Scale Input Range 0 - VDD
- Integrated Multiplexer Offering Up to 16 Independent Analog Inputs
- Individual Enable and Disable of Each Channel
- Hardware or Software Trigger
 - External Trigger Pin
 - Timer Counter Outputs (Corresponding TIOA Trigger)
 - Internal Trigger Counter
 - PWM Event Line
- Drive of PWM Fault Input
- PDC Support
- Possibility of ADC Timings Configuration
- Two Sleep Modes and Conversion Sequencer
 - Automatic Wakeup on Trigger and Back to Sleep Mode after Conversions of all Enabled Channels
 - Possibility of Customized Channel Sequence
- Standby Mode for Fast Wakeup Time Response
 - Power Down Capability

- Automatic Window Comparison of Converted Values
- Write Protect Registers

12.11 Digital-to-Analog Converter (DAC)

- 2 channels, 12-bit DAC
- Up to 1 mega-sample conversion rate in single channel mode
- Flexible conversion range
- Multiple trigger sources for each channel
- Built-in offset and gain calibration
- Possibility to drive output to ground
- Possibility to use as input to analog comparator or ADC (as an internal wire and without S/H stage)
- Two PDCA channels
- Power reduction mode

12.12 CAN Controller (CAN)

- Fully Compliant with CAN 2.0 Part A and 2.0 Part B
- Bit Rates up to 1Mbit/s
- 8 Object Oriented Mailboxes with the Following Properties:
 - CAN Specification 2.0 Part A or 2.0 Part B Programmable for Each Message
 - Object Configurable in Receive (with Overwrite or Not) or Transmit Modes
 - Independent 29-bit Identifier and Mask Defined for Each Mailbox
 - 32-bit Access to Data Registers for Each Mailbox Data Object
 - Uses a CAN_SIZE_COUNTER-bit Timestamp on Receive and Transmit Messages
 - Hardware Concatenation of ID Masked Bitfields To Speed Up Family ID Processing
- 16-bit Internal Timer for Timestamping and Network Synchronization
- Programmable Reception Buffer Length up to 8 Mailbox Objects
- Priority Management between Transmission Mailboxes
- Autobaud and Listening Mode
- Low Power Mode and Programmable Wake-up on Bus Activity or by the Application
- Data, Remote, Error and Overload Frame Handling

12.13 Ethernet MAC (EMAC)

- DMA Master on Receive and Transmit Channels
- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full- and half-duplex operation
- Statistics Counter Registers
- MII (144-pin SAM3X)/RMII (all SAM3X) interface to the physical layer
- Interrupt generation to signal receive and transmit completion

- 128-byte transmit FIFO and 128-byte receive FIFO
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Support Promiscuous Mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Physical layer management through MDIO interface
- Half-duplex flow control by forcing collisions on incoming frames
- Full-duplex flow control with recognition of incoming pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged
- Frames
- Multiple buffers per receive and transmit frame
- Jumbo frames up to 10,240 bytes supported

12.14 True Random Number Generator (TRNG)

- Passed NIST Special Publication 800-22 Tests Suite
- Passed Diehard Random Tests Suite
- Provides a 32-bit Random Number Every 84 Clock Cycles

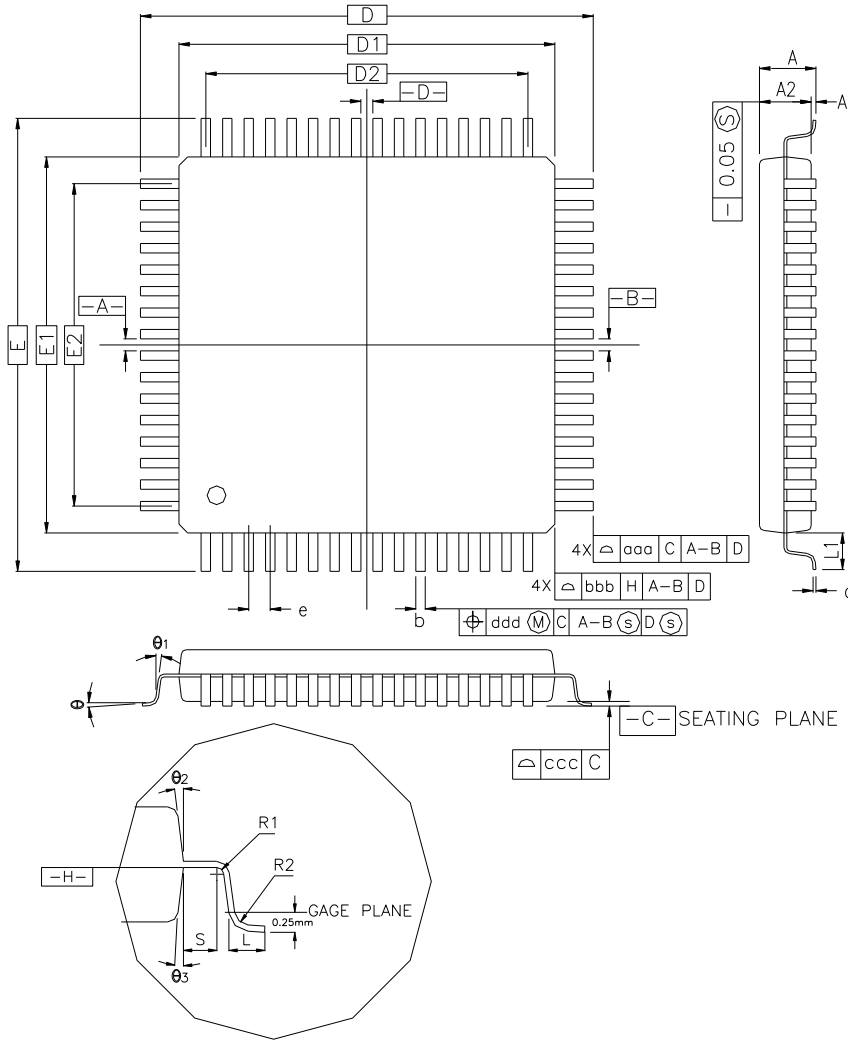
12.15 External Bus Interface (EBI)

- Only present on 144-pin version of SAM3X
- Managing SMC, Nand Flash accesses offering:
 - Up to 8 Configurable chip select
 - Programmable timing on a per chip select basis
 - 16-Mbyte Address Space per Chip Select
 - 8- or 16-bit Data Bus
 - Word, Halfword, Byte Transfers
 - Byte Write or Byte Select Lines
 - Programmable Setup, Pulse and Hold Time for Read Signals per Chip Select
 - Programmable Setup, Pulse and Hold Time for Write Signals per Chip Select
 - Programmable Data Float Time per Chip Select
 - External Wait Request
 - Automatic Switch to Slow Clock Mode
 - Asynchronous Read in Page Mode Supported: Page Size Ranges from 4 to 32 Bytes
 - NAND Flash Controller supporting NAND Flash with Multiplexed Data/Address buses
 - Supports SLC NAND Flash technology
 - Supports Hardware Error Correcting Code (ECC), 1-bit error correction, 2-bit error detection
 - Detection and Correction by Software

13. Package Drawings

The SAM3X/A series devices are available in QFP (LQFP or PQFP) and LFBGA packages.

Figure 13-1. 100-lead LQFP Package Drawing



CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---------------------------------|------------|------|------|------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BSC. | | | 0.630 BSC. | | |
| D1 | 14.00 BSC. | | | 0.551 BSC. | | |
| E | 16.00 BSC. | | | 0.630 BSC. | | |
| E1 | 14.00 BSC. | | | 0.551 BSC. | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ_1 | 0° | — | — | 0° | — | — |
| θ_2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ_3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L ₁ | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 12.00 | | | 0.472 | | |
| E2 | 12.00 | | | 0.472 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Figure 13-2. 100-ball LFBGA Package Drawing

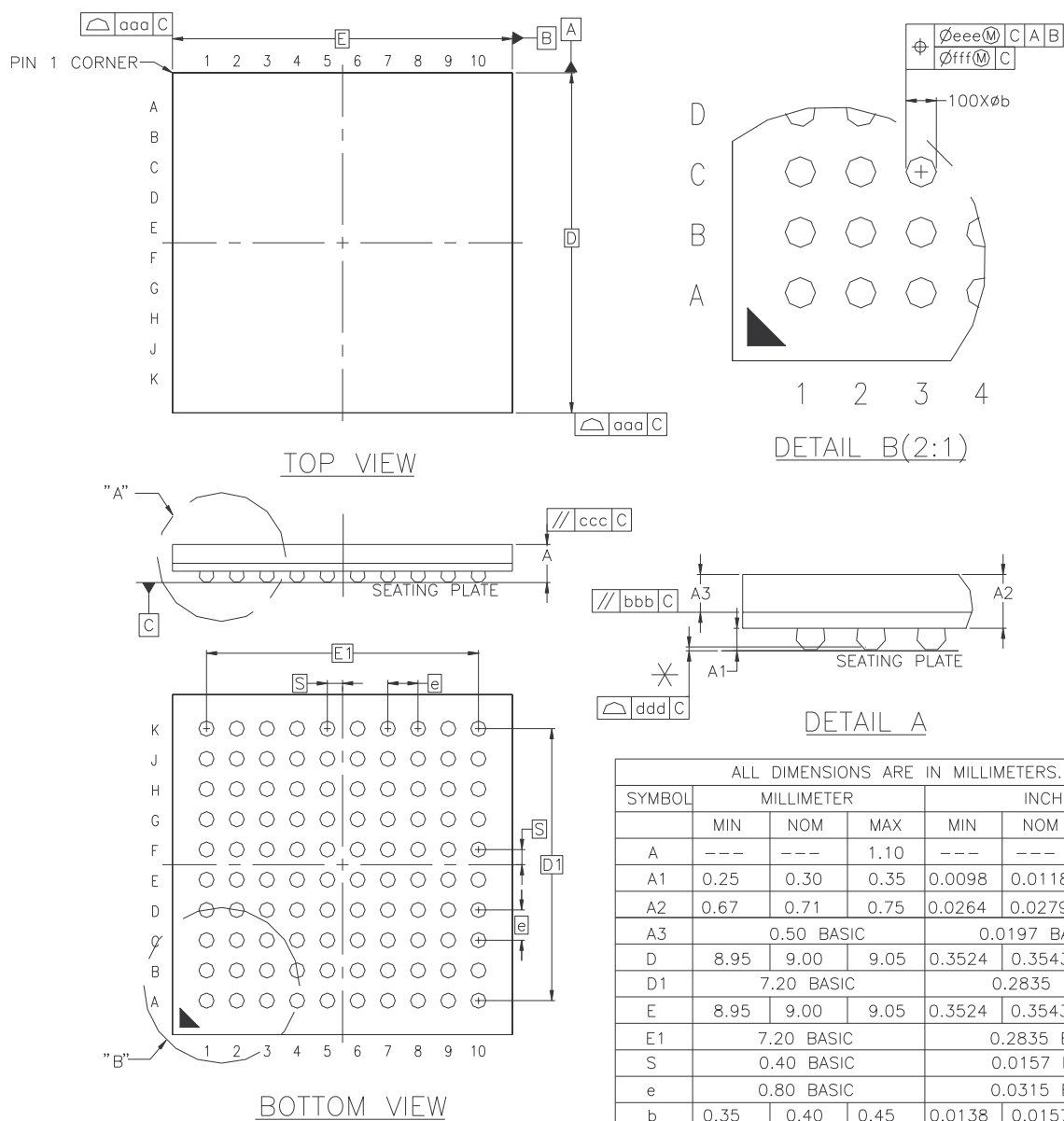
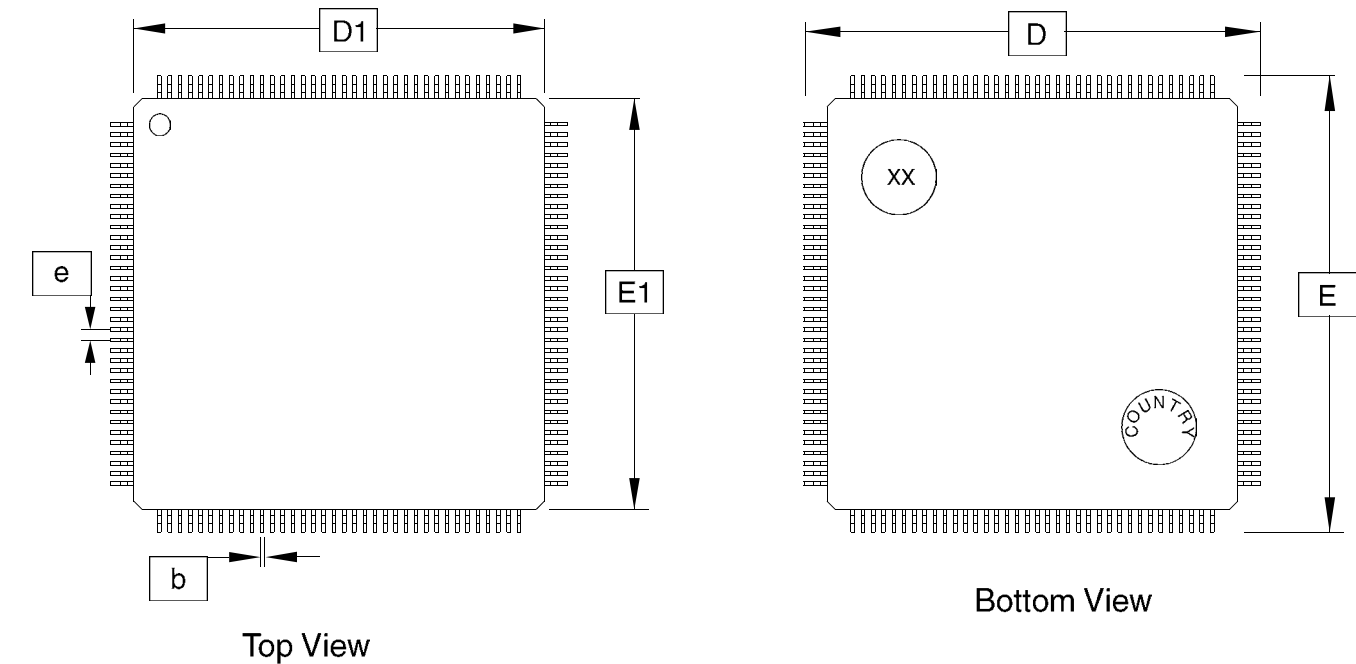


Figure 13-3. 144-lead LQFP Package Drawing

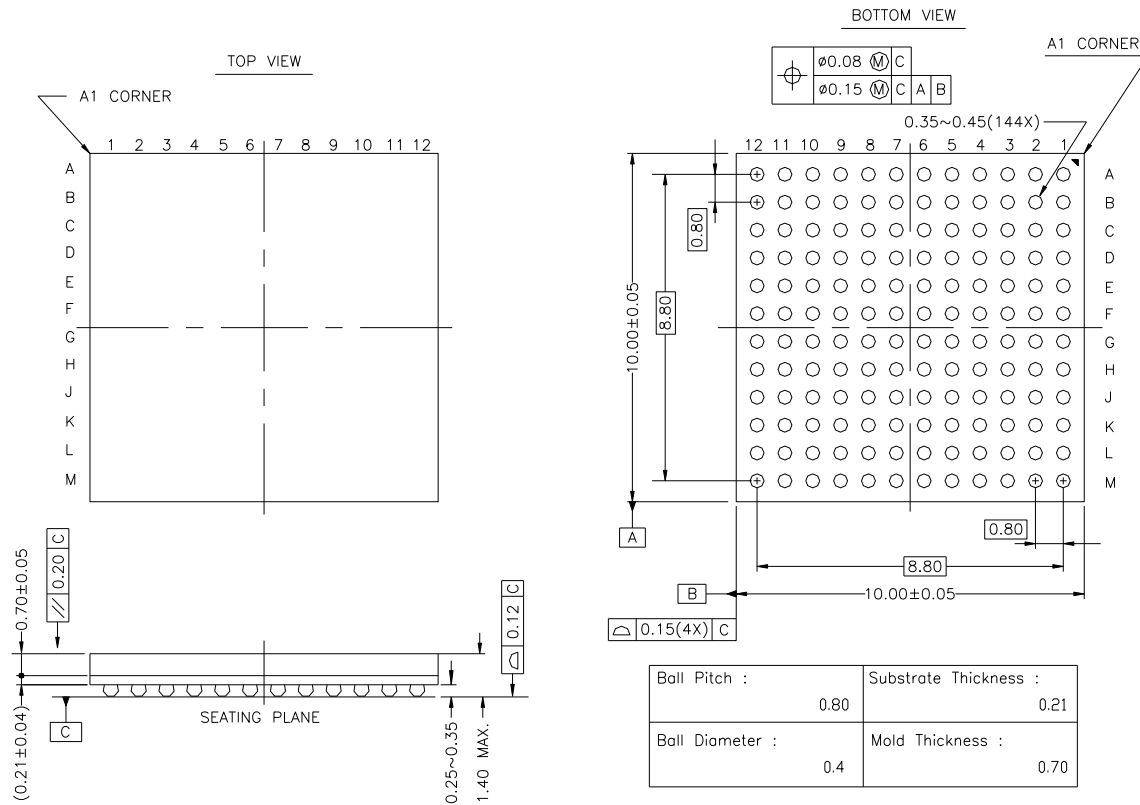


COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|------|------|------|
| A1 | 0.05 | | 0.15 | 6 |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | 22.00 BSC | | | |
| D1 | 20.00 BSC | | | 2, 3 |
| E | 22.00 BSC | | | |
| E1 | 20.00 BSC | | | 2, 3 |
| e | 0.50 BSC | | | |
| b | 0.17 | 0.22 | 0.27 | 4, 5 |
| L1 | 1.00 REF | | | |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-026 for additional information.
 2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
 3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
 5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
 6. A1 is defined as the distance from the seating place to the lowest point on the package body.

Figure 13-4. 144-ball LFBGA Package Drawing

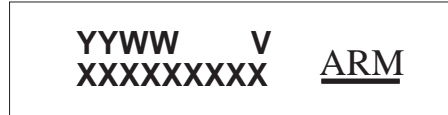


All dimensions are in mm

13.1 Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking may be in one of the following formats:



where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision

“XXXXXXXXXX”: lot number

14. Ordering Information

Table 14-1. SAM3X/A Ordering Information

| Ordering Code | MRL | Flash (Kbytes) | Package | Package Type | Temperature Operating Range |
|---------------|-----|----------------|----------|--------------|-----------------------------|
| ATSAM3A4CA-AU | A | 256 | LQFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3A8CA-AU | A | 512 | LQFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3A4CA-CU | A | 256 | LFPGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3A8CA-CU | A | 512 | LFPGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3X4CA-AU | A | 256 | LQFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3X8CA-AU | A | 512 | LQFP100 | Green | Industrial -40°C to 85°C |
| ATSAM3X4CA-CU | A | 256 | LFPGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3X8CA-CU | A | 512 | LFPGA100 | Green | Industrial -40°C to 85°C |
| ATSAM3X4EA-AU | A | 256 | LQFP144 | Green | Industrial -40°C to 85°C |
| ATSAM3X8EA-AU | A | 512 | LQFP144 | Green | Industrial -40°C to 85°C |
| ATSAM3X4EA-CU | A | 256 | LFPGA144 | Green | Industrial -40°C to 85°C |
| ATSAM3X8EA-CU | A | 512 | LFPGA144 | Green | Industrial -40°C to 85°C |

Revision History

In the tables that follow, the most recent version of the document appears first.

“rfo” indicates changes requested during the review and approval loop.

| Doc. Rev 11057BS | Comments | Change Request Ref. |
|---------------------|---|--------------------------------------|
| | SDRAM Controller info removed: Section “Features” ; Table 1-1, “Configuration Summary” ; Table 3-1, “Signal Description List” ; Section 9.2.1 “External Memory Bus” ; Section 10. “System Controller” ; Table 11.1, “Peripheral Identifiers” ; Section 12.15 “External Bus Interface (EBI)” , and Figure 8-1 “SAM3X/A Product Mapping” . I/O info modified in Section “Features” . Section 1. “SAM3X/A Description” updated. Figure 2-3 “SAM3X4/8E (144 pins) Block Diagram” updated. Table 11-5, “Multiplexing on PIO Controller D (PIOD)” updated. “Write protected Registers” added to Section “Features” . | 8316 8213 |

| Doc. Rev 11057AS | Comments | Change Request Ref. |
|---------------------|-------------|---------------------|
| | First issue | |



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