

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$	I_D $T_A = 25^\circ C$
Q1	30V	28m Ω @ $V_{GS} = 10V$	7.1A
		45m Ω @ $V_{GS} = 4.5V$	5.6A
Q2	-30V	25m Ω @ $V_{GS} = -10V$	-7.4A
		41m Ω @ $V_{GS} = -4.5V$	-5.7A

Description and Applications

This new generation complementary dual MOSFET features low on-resistance and fast switching, making it ideal for high efficiency power management applications.

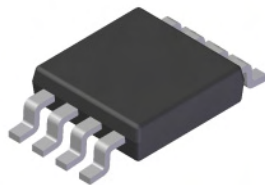
- Motor control
- Backlighting
- DC-DC Converters
- Power management functions

Features and Benefits

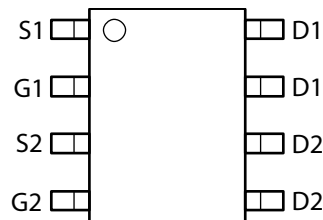
- Low on-resistance
- Fast switching speed
- "Green" Component and RoHS Compliant (Note 1)

Mechanical Data

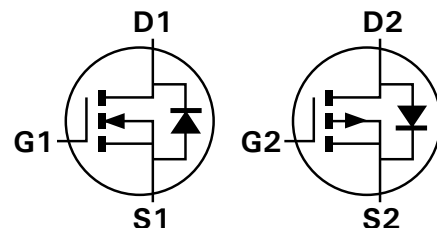
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)



TOP VIEW



Top view



Q1 N-Channel

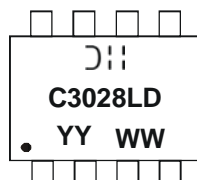
Q2 P-Channel

Ordering Information (Note 1)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMC3028LSD-13	C3028LD	13	12	2,500

Note: 1. Diodes, Inc. defines "Green" products as those which are Eu RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.'s "Green" Policy can be found on our website. For packaging details, go to our website

Marking Information



$\text{D} \parallel \parallel$ = Manufacturer's Marking
 C3028LD = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 09 = 2009)
 WW = Week (01-52)

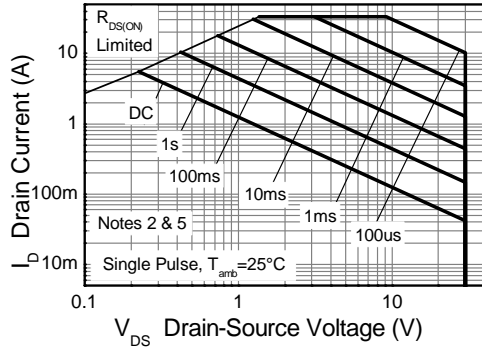
Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage			V _{DSS}	30	-30	V
Gate-Source Voltage			V _{GSS}	±20	±20	V
Continuous Drain Current	V _{GS} = 10V	(Notes 3 & 5)	I _D	7.1	-7.4	A
		T _A = 70°C (Notes 3 & 5)		5.7	-5.9	
		(Notes 2 & 5)		5.5	-5.8	
		(Notes 2 & 6)		6.6	-6.8	
Pulsed Drain Current	V _{GS} = 10V	(Notes 4 & 5)	I _{DM}	34	-36	A
Continuous Source Current (Body diode)		(Notes 3 & 5)	I _S	3.5	-3.5	A
Pulsed Source Current (Body diode)		(Notes 4 & 5)	I _{SM}	34	-36	A

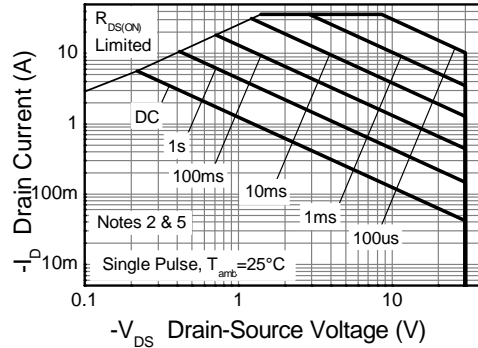
Thermal Characteristics @T_A = 25°C unless otherwise specified

Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation	(Notes 2 & 5)	P _D	1.3		W
Linear Derating Factor			10		mW/°C
Power Dissipation	(Notes 2 & 6)	P _D	1.8		W
Linear Derating Factor			14		mW/°C
Power Dissipation	(Notes 3 & 5)	P _D	2.1		W
Linear Derating Factor			17		mW/°C
Thermal Resistance, Junction to Ambient	(Notes 2 & 5)	R _{θJA}	100		°C/W
	(Notes 2 & 6)		70		
	(Notes 3 & 5)		60		
Thermal Resistance, Junction to Lead	(Notes 5 & 7)	R _{θJL}	51	46	°C/W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150		°C

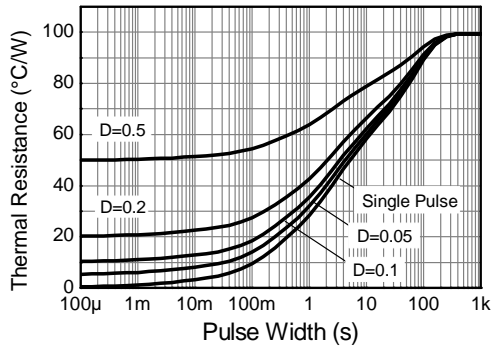
- Notes:
2. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 3. Same as note (2), except the device is measured at t ≤ 10 sec.
 4. Same as note (2), except the device is pulsed with D= 0.02 and pulse width 300 μs. The pulse current is limited by the maximum junction temperature.
 5. For a dual device with one active die.
 6. For a device with two active die running at equal power.
 7. Thermal resistance from junction to solder-point (at the end of the drain lead).



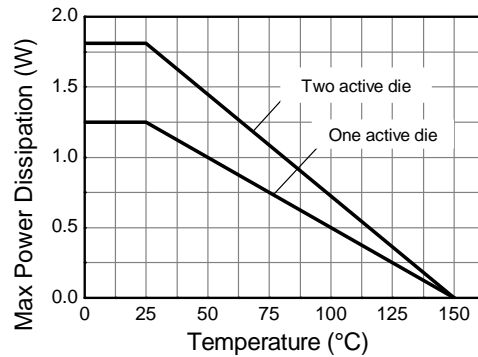
N-channel Safe Operating Area



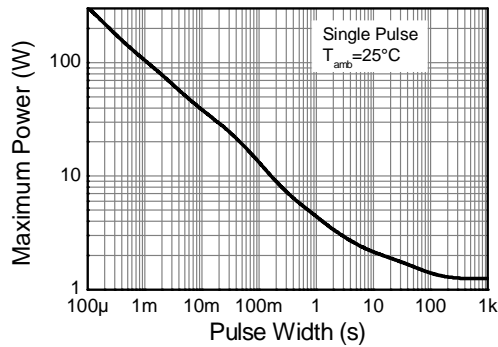
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



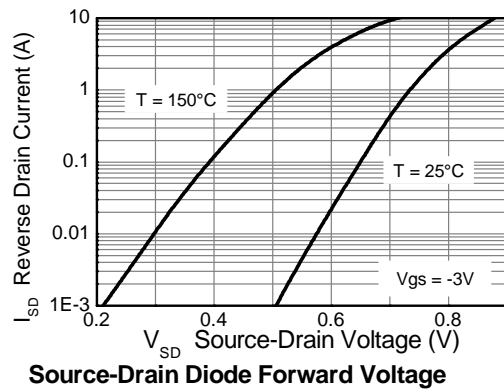
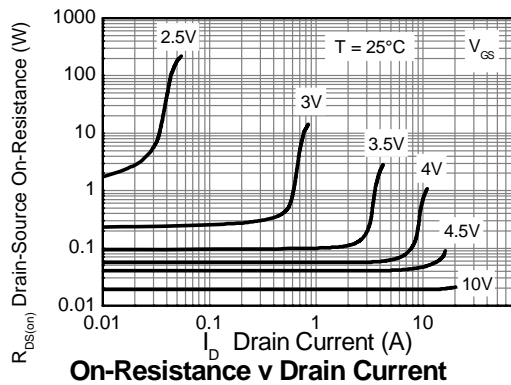
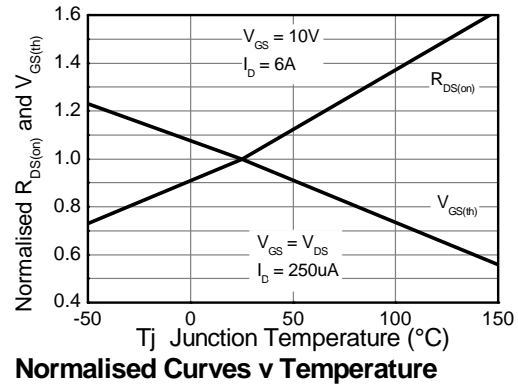
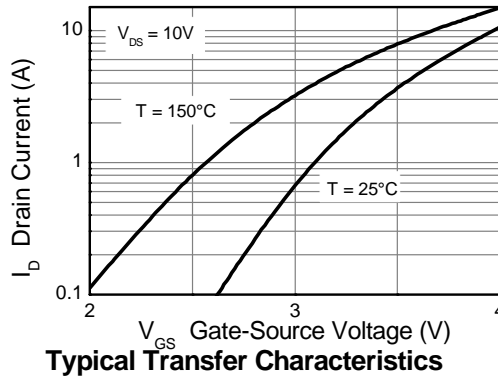
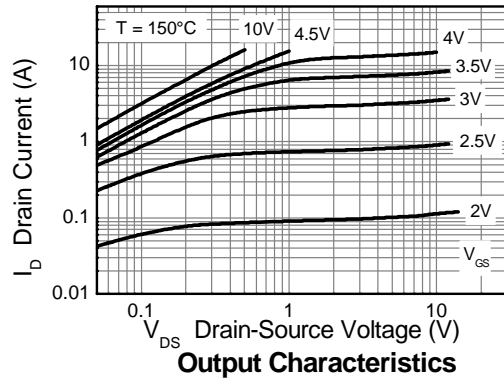
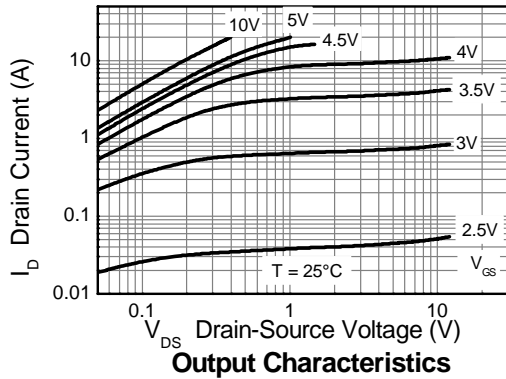
Pulse Power Dissipation

Electrical Characteristics – Q1 N-Channel @ $T_A = 25^\circ\text{C}$ unless otherwise specified

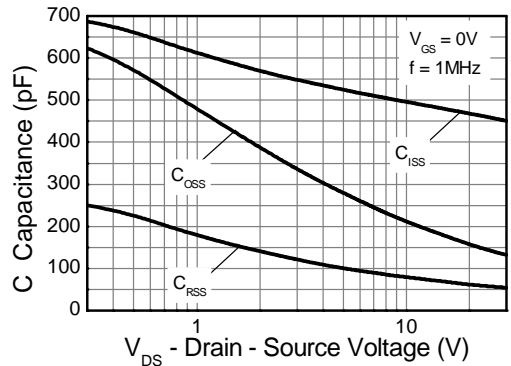
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	0.5	μA	$V_{DS} = 30\text{V}$, $V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 8)	$R_{DS(on)}$	—	—	0.028	Ω	$V_{GS} = 10\text{V}$, $I_D = 6.0\text{A}$
				0.045		$V_{GS} = 4.5\text{V}$, $I_D = 4.9\text{A}$
Forward Transconductance (Notes 8 & 9)	g_{fs}	—	12	—	S	$V_{DS} = 15\text{V}$, $I_D = 6.0\text{A}$
Diode Forward Voltage (Note 8)	V_{SD}	—	0.68	1.2	V	$I_S = 1.7\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time (Note 9)	t_{rr}	—	11.5	—	ns	$I_S = 1.7\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$
Reverse recovery charge (Note 9)	Q_{rr}	—	4.4	—	nC	
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	472	—	pF	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	178	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	65	—	pF	
Total Gate Charge	Q_g	—	5.2	—	nC	$V_{DS} = 15\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 6\text{A}$
Total Gate Charge	Q_g	—	10.5	—	nC	$V_{DS} = 15\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 6\text{A}$
Gate-Source Charge	Q_{gs}	—	1.86	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.3	—	nC	
Turn-On Delay Time (Note 10)	$t_{D(on)}$	—	2.5	—	ns	$V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 1\text{A}$, $R_G \cong 6.0\Omega$
Turn-On Rise Time (Note 10)	t_r	—	3.1	—	ns	
Turn-Off Delay Time (Note 10)	$t_{D(off)}$	—	14	—	ns	
Turn-Off Fall Time (Note 10)	t_f	—	9.7	—	ns	

- Notes:
8. Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$
 9. For design aid only, not subject to production testing.
 10. Switching characteristics are independent of operating junction temperatures.

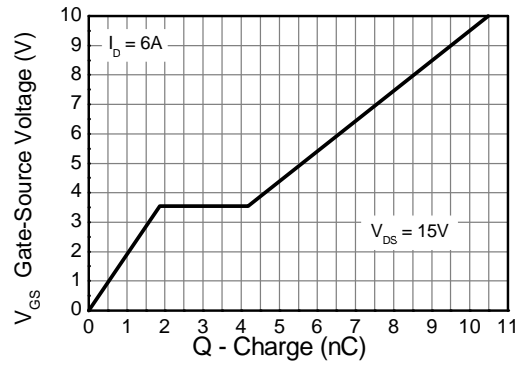
Q1 N-Channel



Q1 N-Channel continued

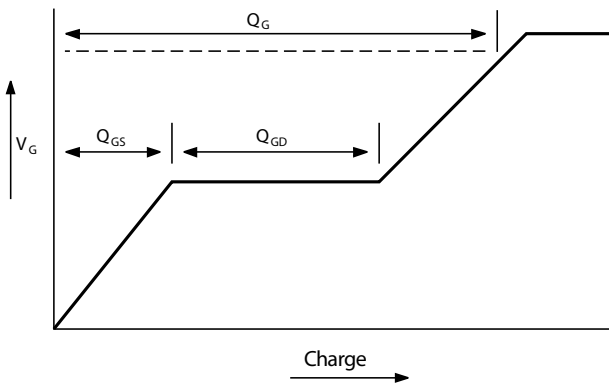


Capacitance v Drain-Source Voltage

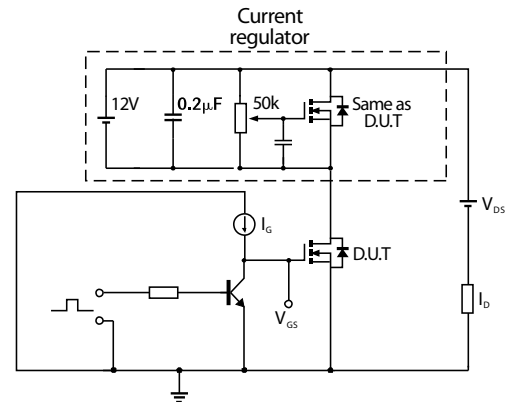


Gate-Source Voltage v Gate Charge

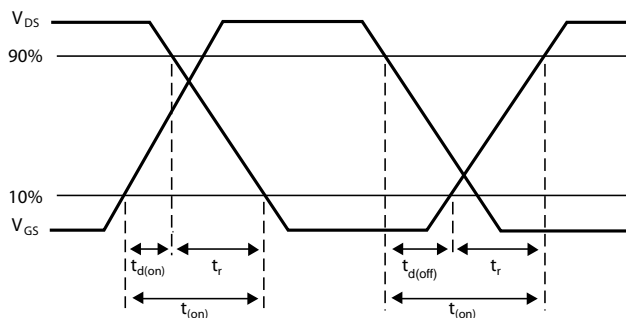
Test Circuits – Q1 N-Channel



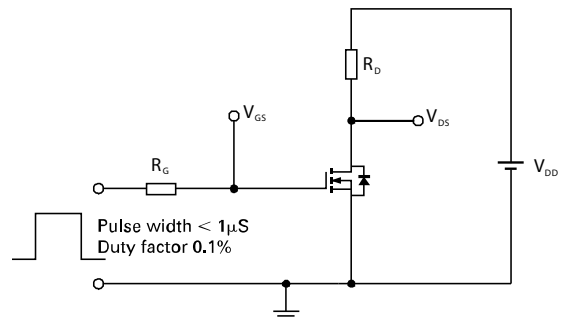
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



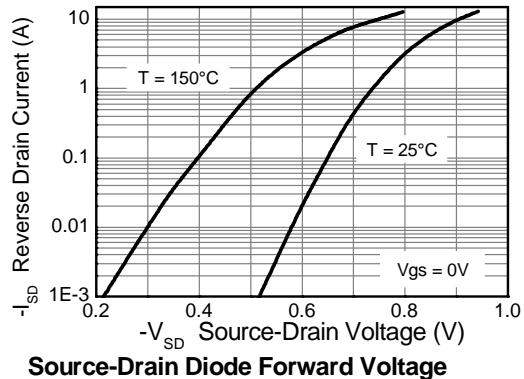
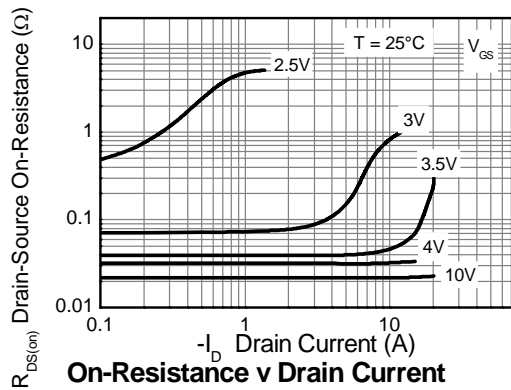
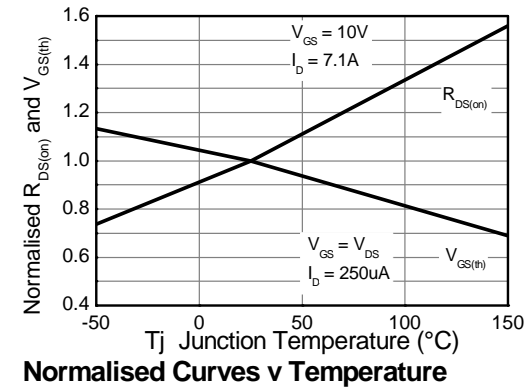
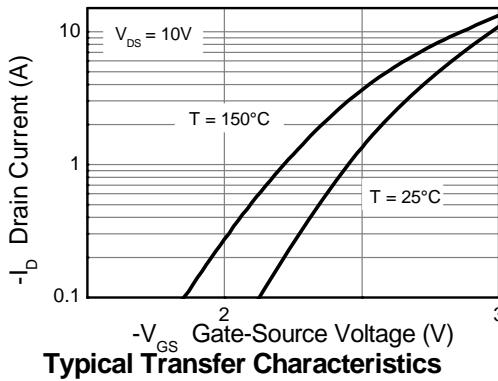
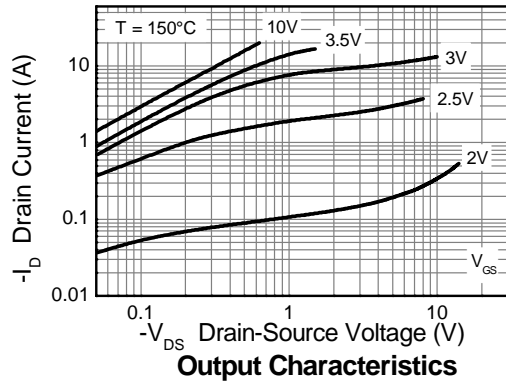
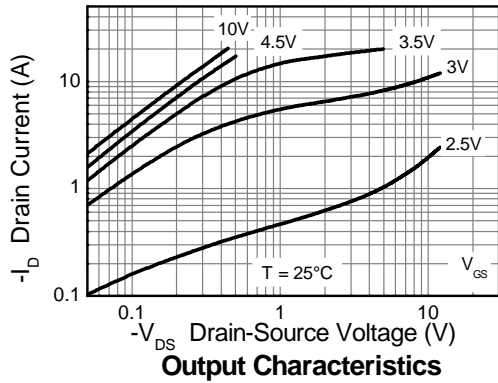
Switching time test circuit

Electrical Characteristics – Q2 P-Channel @T_A = 25°C unless otherwise specified

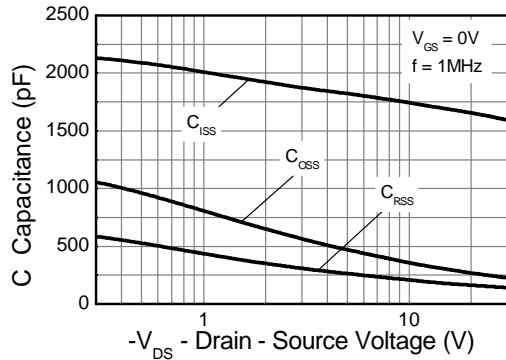
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	—	—	V	I _D = -250μA, V _{GS} = 0V
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-0.5	μA	V _{DS} = -30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(th)}	-1.0	—	-3.0	V	I _D = -250μA, V _{DS} = V _{GS}
Static Drain-Source On-Resistance (Note 8)	R _{DS(ON)}	—	—	0.025	Ω	V _{GS} = -10V, I _D = -7.1A
				0.041		V _{GS} = -4.5V, I _D = -5.5A
Forward Transconductance (Notes 8 & 9)	g _{fs}	—	18.6	—	S	V _{DS} = -15V, I _D = -7.1A
Diode Forward Voltage (Note 8)	V _{SD}	—	-0.80	-1.2	V	I _S = -1.7A, V _{GS} = 0V
Reverse recovery time (Note 9)	t _{rr}	—	16.2	—	ns	I _S = -2.2A, di/dt = 100A/μs
Reverse recovery charge (Note 9)	Q _{rr}	—	10	—	nC	
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1678	—	pF	V _{DS} = -15V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	303	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	178	—	pF	
Total Gate Charge	Q _g	—	16.4	—	nC	V _{DS} = -15V, V _{GS} = -4.5V I _D = -7.1A
Total Gate Charge	Q _g	—	31.6	—	nC	V _{DS} = -15V, V _{GS} = -10V I _D = -7.1A
Gate-Source Charge	Q _{gs}	—	4.3	—	nC	
Gate-Drain Charge	Q _{gd}	—	6.2	—	nC	
Turn-On Delay Time (Note 10)	t _{D(on)}	—	3.5	—	ns	V _{DD} = -15V, V _{GS} = -10V I _D = -1A, R _G = 6.0Ω
Turn-On Rise Time (Note 10)	t _r	—	4.9	—	ns	
Turn-Off Delay Time (Note 10)	t _{D(off)}	—	44	—	ns	
Turn-Off Fall Time (Note 10)	t _f	—	28	—	ns	

- Notes:
8. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
 9. For design aid only, not subject to production testing.
 10. Switching characteristics are independent of operating junction temperatures.

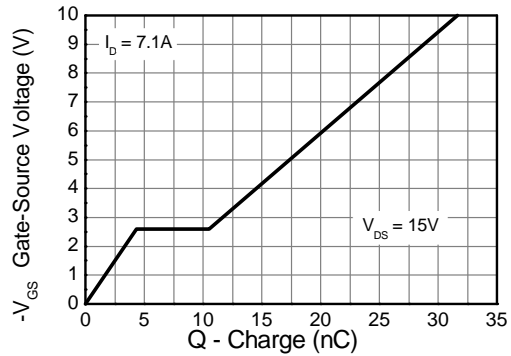
Q2 P-Channel



Q2 P-Channel continued

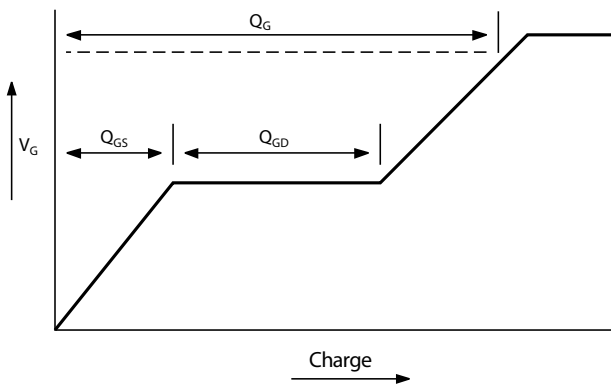


Capacitance v Drain-Source Voltage

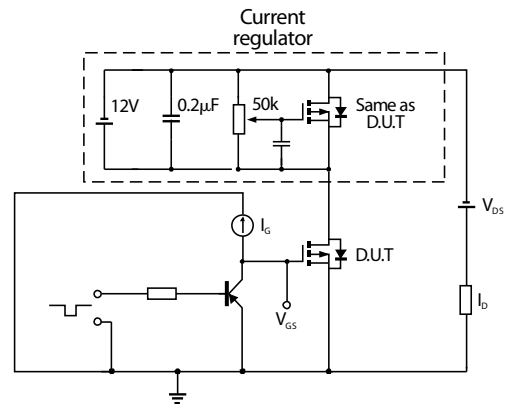


Gate-Source Voltage v Gate Charge

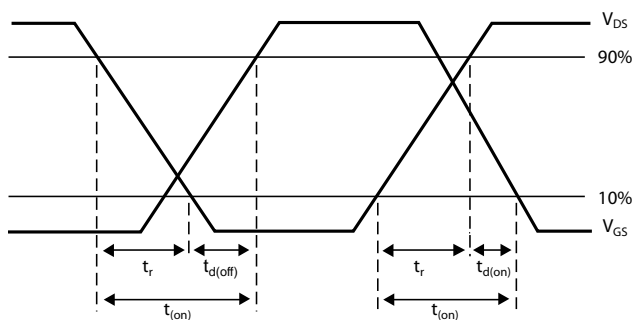
Test Circuits – Q2 P-Channel



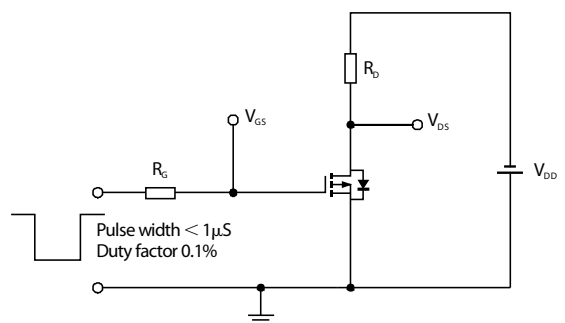
Basic gate charge waveform



Gate charge test circuit

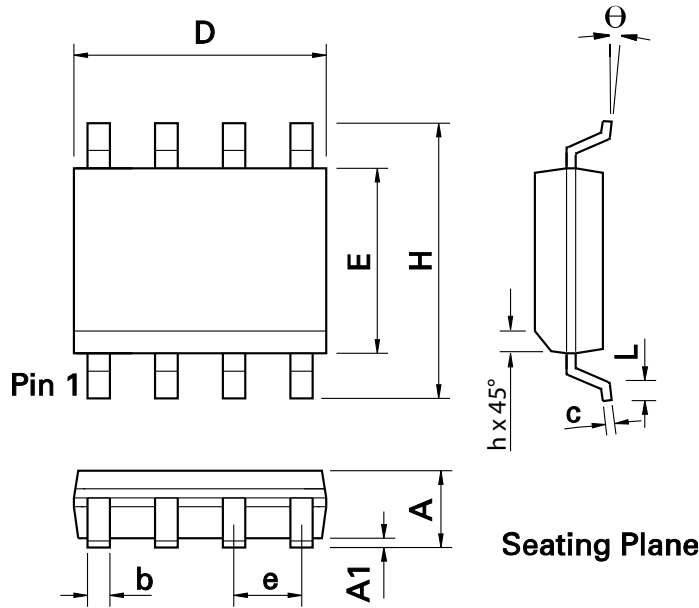


Switching time waveforms



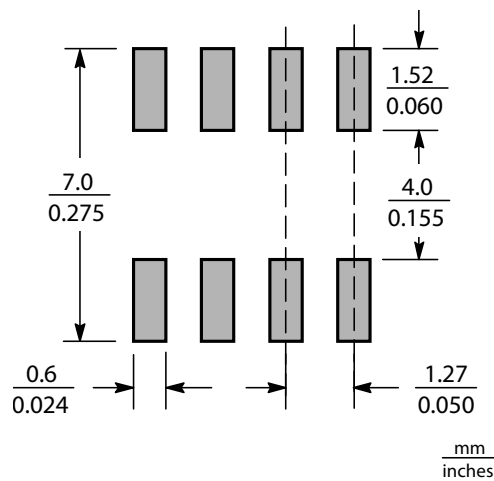
Switching time test circuit

Package Outline Dimensions



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Suggested Pad Layout



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