

**DUAL HIGH-EFFICIENCY PWM STEP-DOWN DC-DC CONVERTER**

**Description**

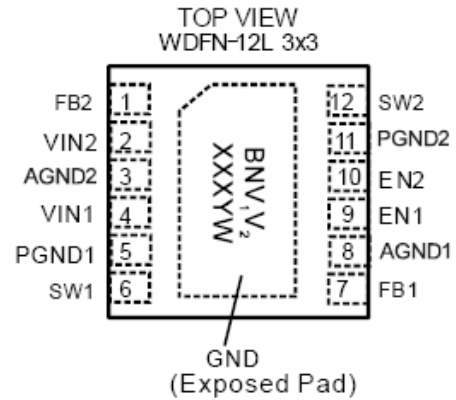
The PAM2319 is a dual step-down current-mode, DC-DC converter. At heavy load, the constant frequency PWM control performs excellent stability and transient response. To ensure the longest battery life in portable applications, the PAM2319 provides a power-saving Pulse-Skipping Modulation (PSM) mode to reduce quiescent current under light load operation.

The PAM2319 supports a range of input voltages from 2.7V to 5.5V, allowing the use of a single Li+/Li-polymer cell, multiple Alkaline/NiMH cell, USB, and other standard power sources. The dual output voltages are adjustable from 1.0V to 3.3V. Both channels employ internal power switch and synchronous rectifier to minimize external part count and realize high efficiency. During shutdown, the input is disconnected from the output and the shutdown current is less than 0.1µA. Other key features include under-voltage lockout, soft-start, short circuit protection and thermal shutdown.

**Features**

- Supply Voltage: 2.7V to 5.5V
- Output Voltage:
  - Vo1 ADJ/1000mA
  - Vo2 ADJ/2000mA
- Low Quiescent Current: Channel 1: 40µA; Channel 2: 55µA
- High Efficiency:
- Switching Frequency: 3MHz(Channel 1)  
2.5MHz(Channel 2)
- Internal Synchronous Rectifier
- Soft Start
- Under-Voltage Lockout
- Short Circuit Protection
- Thermal Shutdown
- Small W-DFN3X3-12L Pb-Free/Halogen Free Package
- RoHS/REACH Compliant

**Pin Assignments**



**Applications**

- Portable Electronics
- Personal Information Appliances
- Wireless and DSL Modems

## Typical Applications Circuit

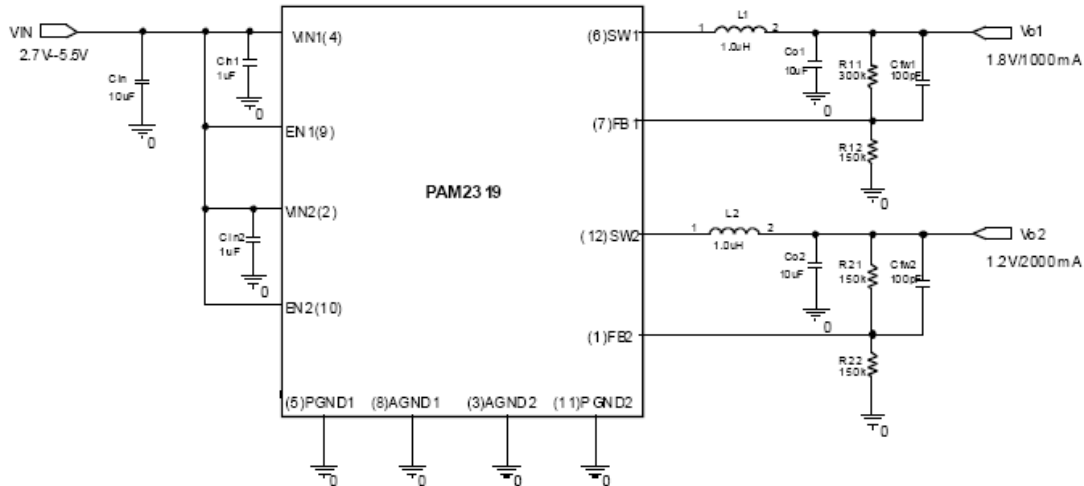
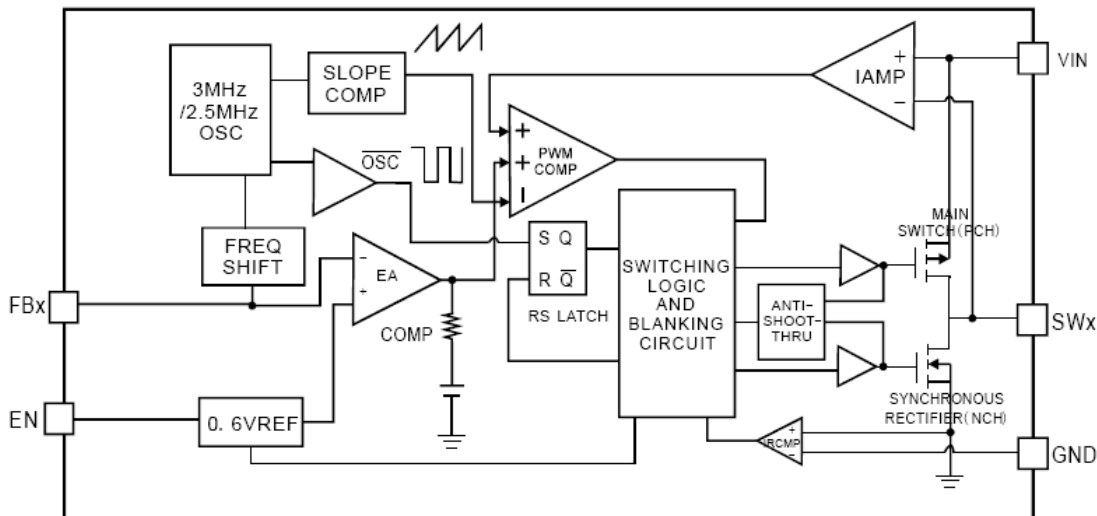


Figure 1. Adjustable Voltage Regulator

## Pin Descriptions

Pin Number	W-DFN3x3-12L Pin Name	Function
1	FB2	Channel 2 feedback pin internally set to 0.6V.
2	VIN2	Input voltage pin of channel 2.
3	AGND2	Signal ground of channel 2 for small signal components.
4	VIN1	Input voltage pin of channel 1.
5	PGND1	Main power ground pin of channel 1
6	SW1	Channel 1 switching pin. The drains of the internal main and synchronous power MOSFET.
7	FB1	Channel 1 feedback pin internally set to 0.6V.
8	AGND1	Signal ground of channel 1 for small signal components.
9	EN1	Enable control input. Pull logic high to enable Vo1. Pull logic low to disable.
10	EN2	Enable control input. Pull logic high to enable Vo2. Pull logic low to disable.
11	PGND2	Main power ground pin of channel 2.
12	SW2	Channel 2 switching pin. The drains of the internal main and synchronous power MOSFET.
—	Exposed Pad	Connect to GND

## Functional Block Diagram



Note: 1. The diagram above just shows one channel.

## Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Input Voltage	-0.3 to 6.5	V
EN1, FB1, SW1, EN2, FB2 and SW2 Pin Voltage	-0.3 to ( $V_{IN} + 0.3$ )	V
Maximum Junction Temperature	150	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$
Soldering Temperature	260, 10sec	$^\circ\text{C}$

## Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage	2.7 to 5.5	V
Ambient Temperature Range	-40 to +85	$^\circ\text{C}$
Junction Temperature Range	-40 to +125	

## Thermal Information

Parameter	Symbol	Package	Max	Unit
Thermal Resistance (Junction to Ambient)	$\theta_{JA}$	W-DFN3x3-12L	60	$^\circ\text{C/W}$
Thermal Resistance (Junction to Case)	$\theta_{JC}$	W-DFN3x3-12L	8.5	

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, V<sub>IN</sub> = 3.3V, V<sub>O</sub> = 1.8V, C<sub>IN</sub> = 10μF, C<sub>O</sub> = 10μF, L = 1μH, unless otherwise specified.)

**Channel 1**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range	V <sub>IN</sub>		2.7		5.5	V
UVLO Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> Rising		2.4	2.5	V
		Hysteresis		240		mV
		V <sub>IN</sub> Falling	1.8			V
Regulated Feedback Voltage	V <sub>FB</sub>		0.588	0.600	0.612	V
Reference Voltage Line Regulation	ΔV <sub>FB</sub>			0.3		%/V
Regulated Output Voltage Accuracy	V <sub>O</sub>	I <sub>O</sub> = 100mA	-3		+3	%
Peak Inductor Current	I <sub>PK</sub>	V <sub>O</sub> = 90%		1.5		A
Output Voltage Line Regulation	LNR	V <sub>IN</sub> = 2.7V to 5V, I <sub>O</sub> = 10mA		0.2	0.5	%/V
Output Voltage Load Regulation	LDR	I <sub>O</sub> = 1mA to 1000mA	-2		+2	%
Quiescent Current	I <sub>Q</sub>	No Load		40	80	μA
Shutdown Current	I <sub>SD</sub>	V <sub>EN</sub> = 0V		0.1	1	μA
Oscillator Frequency	f <sub>OSC</sub>	V <sub>O</sub> = 100%		3		MHz
		V <sub>FB</sub> = 0V or V <sub>O</sub> = 0V		1		MHz
Drain-Source On-State Resisitance	R <sub>DS(ON)</sub>	P MOSFET		0.35	0.45	Ω
		N MOSFET		0.35	0.45	Ω
SW Leakage Current	I <sub>LSW</sub>			±0.01	1	μA
Efficiency	η	Output1, I <sub>O</sub> = 500mA, V <sub>IN</sub> = 3.3V		84		%
PSM Threshold	I <sub>TH</sub>	V <sub>IN</sub> = 3.3V		100		mA
EN Threshold High	V <sub>EH</sub>		1.5			V
EN Threshold Low	V <sub>EL</sub>				0.3	V
EN Leakage Current	I <sub>EN</sub>			±0.01		μA
Soft-Start	T <sub>ON</sub>	From EN1 to Output		2		ms
Over Temperature Protection	OTP			150		°C
OTP Hysteresis	OTH			30		°C

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.3\text{V}$ ,  $V_O = 1.2\text{V}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_O = 10\mu\text{F}$ ,  $L = 1\mu\text{H}$ , unless otherwise specified.)

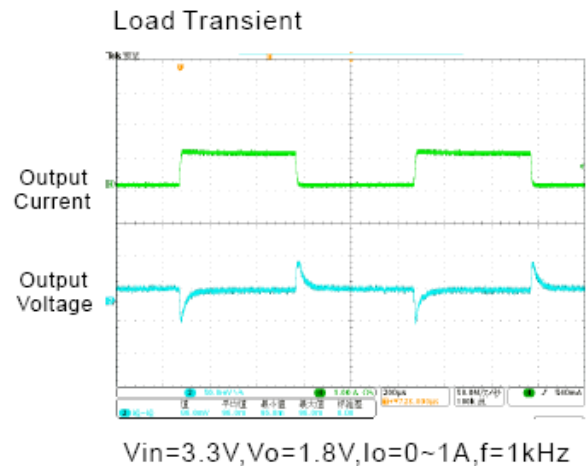
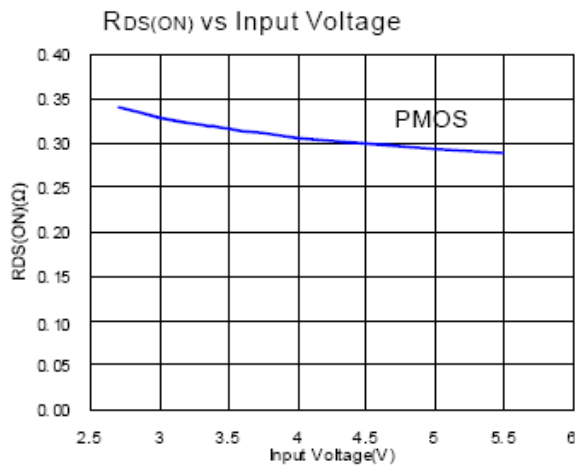
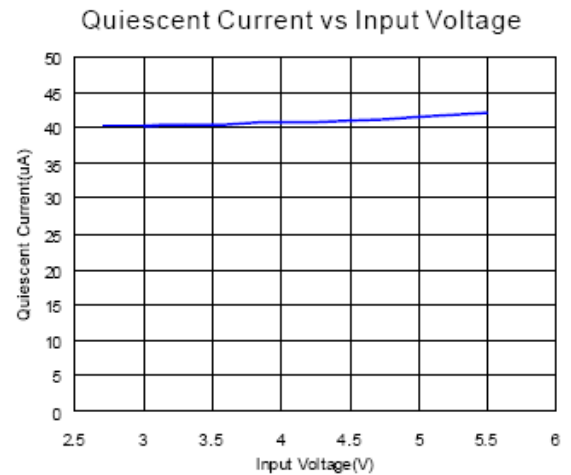
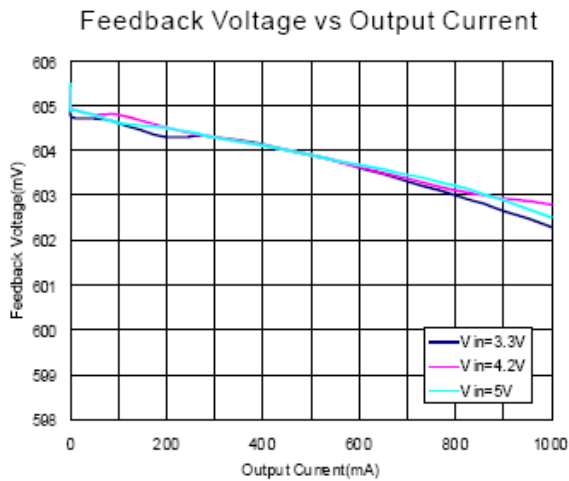
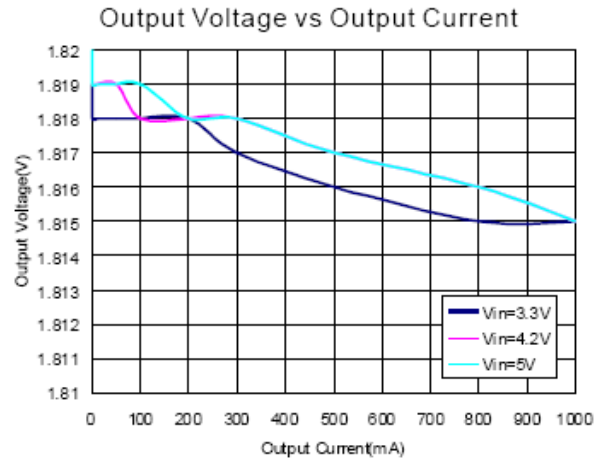
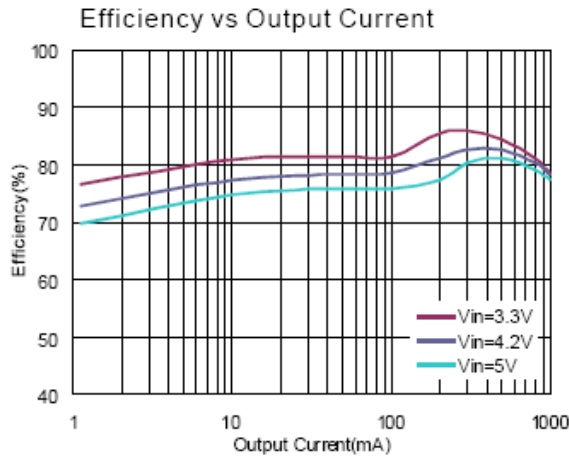
**Channel 2**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range	$V_{IN}$		2.7		5.5	V
UVLO Threshold	$V_{UVLO}$	$V_{IN}$ Rising		2.6	2.7	V
		Hysteresis		250		mV
		$V_{IN}$ Falling	12			V
Regulated Feedback Voltage	$V_{FB}$		0.588	0.600	0.612	V
Reference Voltage Line Regulation	$\Delta V_{FB}$			0.3		%/V
Regulated Output Voltage Accuracy	$V_O$	$I_O = 100\text{mA}$	-3		+3	%
Peak Inductor Current	$I_{PK}$	$V_O = 90\%$		3		A
Output Voltage Line Regulation	LNR	$V_{IN} = 2.7\text{V to } 5\text{V}$ , $I_O = 10\text{mA}$		0.2	0.5	%/V
Output Voltage Load Regulation	LDR	$I_O = 1\text{mA to } 1000\text{mA}$	-2		+2	%
Quiescent Current	$I_Q$	No Load		55	100	$\mu\text{A}$
Shutdown Current	$I_{SD}$	$V_{EN} = 0\text{V}$		0.1	1.0	$\mu\text{A}$
Oscillator Frequency	$f_{OSC}$	$V_O = 100\%$		2.5		MHz
Drain-Source On-State Resisitance	$R_{DS(ON)}$	P MOSFET		0.11		$\Omega$
		N MOSFET		0.85		$\Omega$
SW Leakage Current	$I_{LSW}$			$\pm 0.01$	1	$\mu\text{A}$
Efficiency	$\eta$	Output1, $I_O = 500\text{mA}$ , $V_{IN} = 3.3\text{V}$		87		%
PSM Threshold	$I_{TH}$	$V_{IN} = 3.3\text{V}$		250	450	mA
EN Threshold High	$V_{EH}$		1.5			V
EN Threshold Low	$V_{EL}$				0.3	V
EN Leakage Current	$I_{EN}$			$\pm 0.01$		$\mu\text{A}$
Soft-Start	$T_{ON}$	From EN1 to Output		250		ms
Over Temperature Protection	OTP			150		$^\circ\text{C}$
OTP Hysteresis	OTH			30		$^\circ\text{C}$

## Typical Performance Characteristics

(@T<sub>A</sub> = +25°C, V<sub>O</sub> = 1.8V, C<sub>IN</sub> = 10μF, C<sub>O</sub> = 10μF, L = 1μH, unless otherwise specified.)

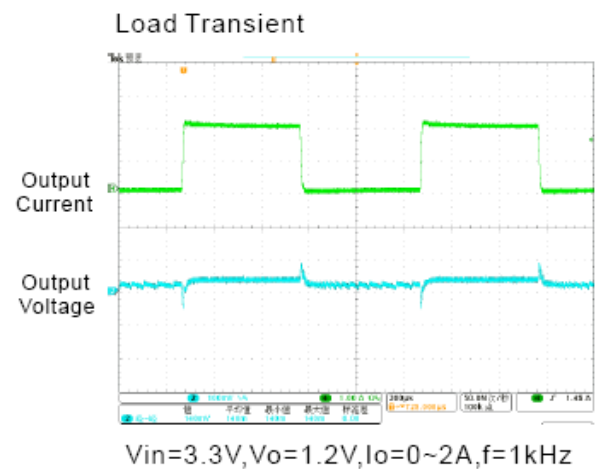
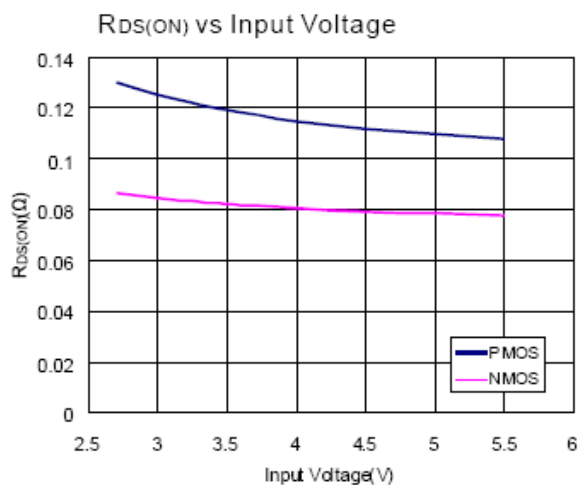
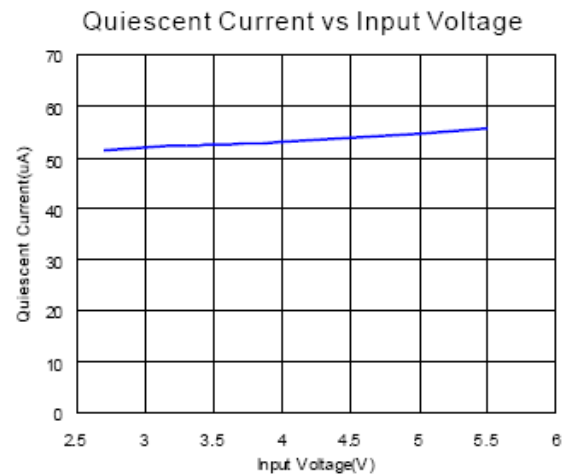
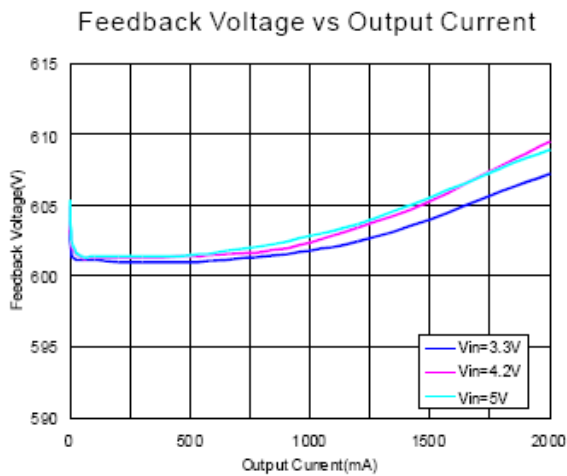
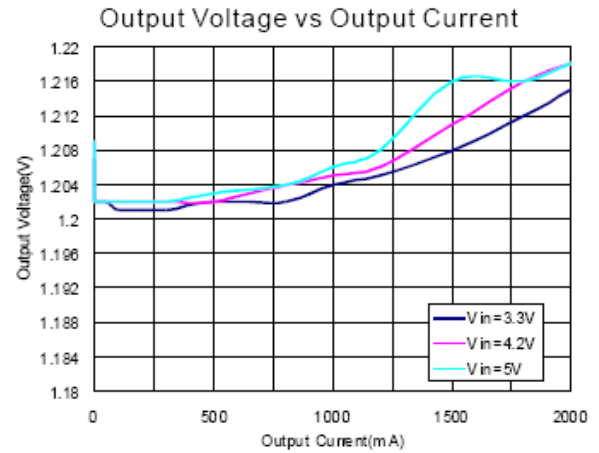
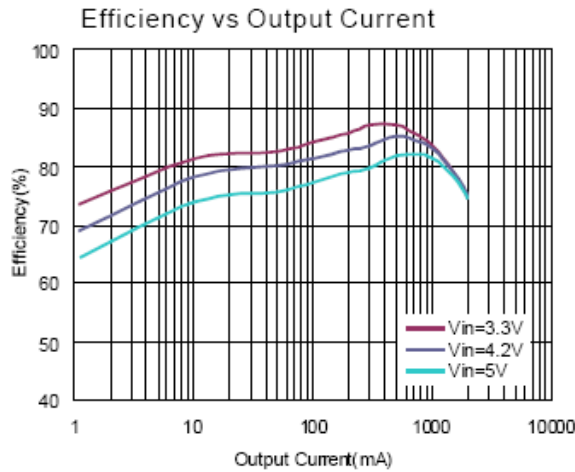
### Channel 1



**Typical Performance Characteristics** (cont.)

(@T<sub>A</sub> = +25°C, V<sub>O</sub> = 1.2V, C<sub>IN</sub> = 10μF, C<sub>O</sub> = 10μF, L = 1μH, unless otherwise specified.)

**Channel 2**



## Application Information

The basic PAM2319 application circuit is shown in Page 2. External component selection is determined by the load requirement, selecting L first and then C<sub>IN</sub> and C<sub>OUT</sub>.

### Inductor Selection

For most applications, the value of the inductor will fall in the range of 0.47μH to 2μH. Its value is chosen based on the desired ripple current and efficiency. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V<sub>IN</sub> or V<sub>OUT</sub> also increases the ripple current as shown in equation. For channel 1, 1A reasonable starting point for setting ripple current is ΔI<sub>L</sub> = 400mA (40% of 1A) and for channel 2, 2A setting ripple current is 800mA.

$$\Delta I_L = \frac{1}{fL} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \quad \text{Equation (1)}$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 4.2A rated inductor should be enough for most applications (3A + 1.2A). For better efficiency, choose a low DC-resistance inductor.

V <sub>O</sub>	1.2V	1.5V	1.8V	2.5V	3.3V
L	1.2μH	1.5μH	2.2μH	2.2μH	2.2μH

### C<sub>IN</sub> and C<sub>OUT</sub> Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V<sub>OUT</sub>/V<sub>IN</sub>. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN\text{required}} I_{RMS} \cong I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at V<sub>IN</sub> = 2V<sub>OUT</sub>, where I<sub>RMS</sub> = I<sub>OUT</sub> / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Consult the manufacturer if there is any question.

The selection of C<sub>OUT</sub> is driven by the required effective series resistance (ESR).

Typically, once the ESR requirement for C<sub>OUT</sub> has been met, the RMS current rating generally far exceeds the I<sub>RIPPLE</sub> (P-P) requirement. The output ripple ΔV<sub>OUT</sub> is determined by:

$$\Delta V_{OUT} \approx \Delta I_L (ESR + 1/8f C_{OUT})$$

Where f = operating frequency, C<sub>OUT</sub> = output capacitance and ΔI<sub>L</sub> = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI<sub>L</sub> increases with input voltage.

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Using ceramic capacitors can achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

### Thermal Consideration

Thermal protection limits power dissipation in the PAM2319. When the junction temperature exceeds +150°C, the OTP (Over Temperature Protection) starts the thermal shutdown and turns the pass transistor off. The pass transistor resumes operation after the junction temperature drops below +120°C.

For continuous operation, the junction temperature should be maintained below +125°C. The power dissipation is defined as:

$$P_D = I_O^2 \frac{V_O R_{DS(ON)H} + (V_{IN} - V_O) R_{DS(ON)L}}{V_{IN}} + (t_{sw} F_s I_O + I_Q) V_{IN}$$

I<sub>Q</sub> is the step-down converter quiescent current. The term t<sub>sw</sub> is used to estimate the full load step-down converter switching losses.



## Application Information (cont.)

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_D = I_O^2 R_{DS(ON)H} + I_Q V_{IN}$$

Since  $R_{DS(ON)}$ , quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surrounding airflow and temperature difference between junction and ambient. The maximum power dissipation can be calculated by the following formula:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where  $T_{J(max)}$  is the maximum allowable junction temperature +125°C.  $T_A$  is the ambient temperature and  $\theta_{JA}$  is the thermal resistance from the junction to the ambient. Based on the standard JEDEC for a two layers thermal test board, the thermal resistance  $\theta_{JA}$  of WDFN3x3 is 60°C/W. The maximum power dissipation at  $T_A = +25^\circ\text{C}$  can be calculated by following formula:

$$P_D = (125^\circ\text{C} - 25^\circ\text{C}) / 60^\circ\text{C/W} = 1.67\text{W}$$

### Setting the Output Voltage

The internal reference is 0.6V (Typical). The output voltage is calculated as below:

The output voltage is given by Table 1.

$$V_O = 0.6 \times \left( 1 + \frac{R_1}{R_2} \right)$$

Table 1: Resistor selection for output voltage setting.

$V_O$	R1	R2
1.2V	150k	150k
1.5V	150k	100k
1.8V	300k	150k
2.5V	380k	120k
3.3V	680k	150k

### Pulse Skipping Mode (PSM) Description

When load current decreases, the peak switch current in Power-PMOS will be lower than skip current threshold and the device will enter into Pulse Skipping Mode.

In this mode, the device has two states, working state and idle state. First, the device enters into working state controlled by internal error amplifier. When the feedback voltage gets higher than internal reference voltage, the device will enter into low  $I_Q$  idle state with most of internal blocks disabled. The output voltage will be reduced by loading or leakage current. When the feedback voltage gets lower than the internal reference voltage, the convertor will start a working state again.

### 100% Duty Cycle Operation

As the input voltage approaches the output voltage, the converter turns the P-Channel transistor continuously on. In this mode the output voltage is equal to the input voltage minus the voltage drop across the P-Channel transistor:

$$V_{OUT} = V_{IN} - I_{LOAD} (R_{DS(ON)} + R_L)$$

where  $R_{DS(ON)}$  = P-Channel switch ON resistance,  $I_{LOAD}$  = Output Current,  $R_L$  = Inductor DC Resistance

### UVLO and Soft-Start

The reference and the circuit remain reset until the  $V_{IN}$  crosses its UVLO threshold.

The PAM2319 has an internal soft-start circuit that limits the in-rush current during start-up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot.

### Thermal Shutdown

When the die temperature exceeds +150°C, a reset occurs and the reset remains until the temperature decrease to +120°C, at which time the circuit can be restarted.

## Application Information (cont.)

### Short Circuit Protection

Channel 1:

The switch peak current is limited cycle-by-cycle to a typical value in the event of an output voltage short circuit. The device operates with a frequency of 1MHz and minimum duty cycle. Therefore the average input current is typical 350mA ( $V_{IN} = 3.3V$ ).

Channel 2:

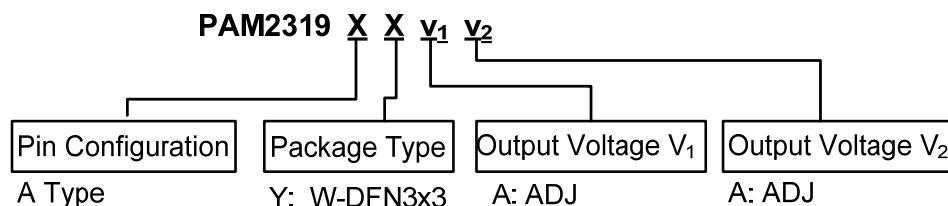
When the converter output is shorted or the device is overloaded, each high-side MOSFET current-limit event (3A typ) turns off the high-side MOSFET and turns on the low-side MOSFET. An internal counter is used to count the each current-limit event. The counter is reset after consecutive high-side MOSFETs turn on without reaching current limit. If the current-limit condition persists, the counter fills up. The control logic then stops both high-side and lowside MOSFETs and waits for a hiccup period, before attempting a new soft-start sequence. The counter bits is decided by  $V_{FB}$  voltage. If  $V_{FB} < 0.2$ , the counter is 3-bit counter; if  $V_{FB} > 0.2$  the counter is 6-bit counter. The typical hiccup made duty cycle is 1.7%. The hiccup mode is disable during soft-start time.

### PCB Layout Check List

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the PAM2319. Check the following in your layout:

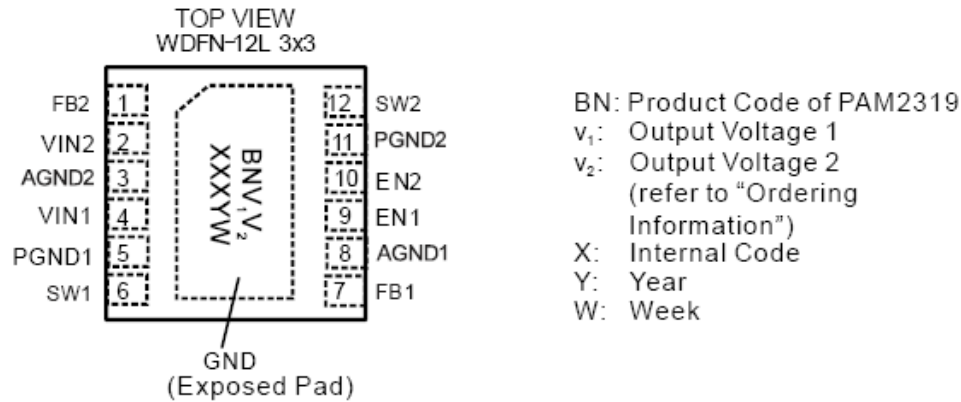
1. The input capacitor should be close to IC as close as possible.
2. Minimize the switching loop area to avoid excessive switching noise.
3. Two parts GND should be separately layout to avoid disturbing by each other.
4. Must put a small decoupling capacitor between Vin2 Pin and AGND2 Pin.
5. Vo2 output capacitor should be close to output connector to minimize PCB trace resistance affect on ripple voltage. Recommend use two output capacitor, one close to inductor and IC, another close to output connector.
6. PGND1 Pin should not directly connect to the thermal pad (PGND), it should connect to input capacitor GND then to other GND.
7. AGND should connect to PGND at input capacitor GND.
8. For the good thermal dissipation, PAM2316 has a heat dissipate pad in the bottom side, it should be soldered to PCB surface. For the copper area can't be large in the component side, so we can use multiple vias connect to other side of the PCB.
9. Avoid using vias in the high-current paths. If vias are unavoidable, use multiple vias in parallel to reduce resistance and inductance.

## Ordering Information



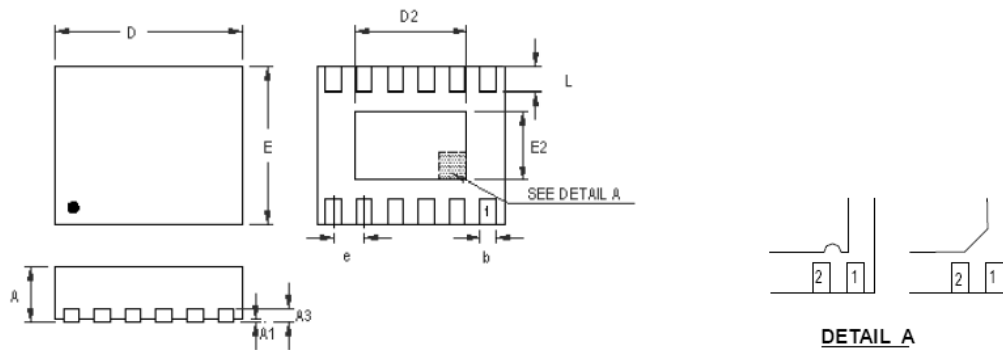
Part Number	Part Marking	Package Type	Standard Package
PAM2319AYAA	BNAA XXXYYW	W-DFN3x3-12L	3000 Units/Tape & Reel

## Marking Information



## Package Outline Dimensions (All dimensions in mm.)

### W-DFN3x3-12



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.400	1.750	0.055	0.069
e	0.450		0.018	
L	0.350	0.450	0.014	0.018

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