



# FDMC86265P

## P-Channel PowerTrench<sup>®</sup> MOSFET

-150 V, -1 A, 1.2 Ω

### Features

- Max  $r_{DS(on)} = 1.2 \Omega$  at  $V_{GS} = -10 V$ ,  $I_D = -1 A$
- Max  $r_{DS(on)} = 1.4 \Omega$  at  $V_{GS} = -6 V$ ,  $I_D = -0.9 A$
- Very low RDS-on mid voltage P-channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL Tested
- RoHS Compliant

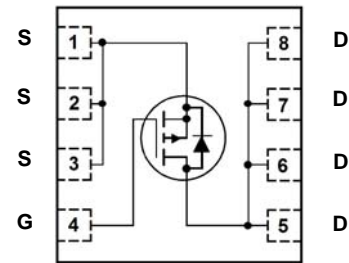
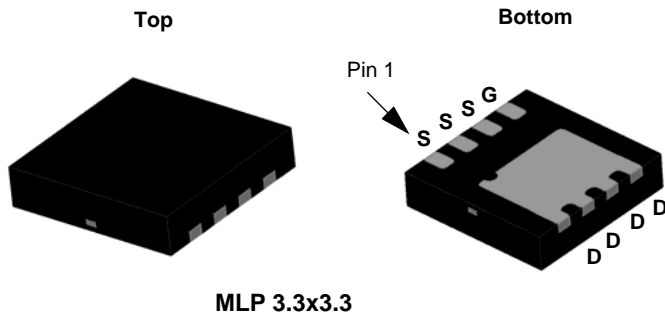


### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been optimized for the on-state resistance and yet maintain superior switching performance.

### Applications

- Active Clamp Switch
- Load Switch



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-150	V
$V_{GS}$	Gate to Source Voltage	$\pm 25$	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ C$	-1.8
	-Continuous	$T_A = 25^\circ C$ (Note 1a)	-1
	-Pulsed		-2
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	6
$P_D$	Power Dissipation	$T_C = 25^\circ C$	16
	Power Dissipation	$T_A = 25^\circ C$ (Note 1a)	2.3
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86265P	FDMC86265P	Power 33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-125		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -120\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-2	-3.2	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}$ , $I_D = -1\text{ A}$		0.86	1.2	$\Omega$
		$V_{GS} = -6\text{ V}$ , $I_D = -0.9\text{ A}$		0.95	1.4	
		$V_{GS} = -10\text{ V}$ , $I_D = -1\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		1.53	2.2	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}$ , $I_D = -1\text{ A}$		1.9		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		158	210	pF
$C_{oss}$	Output Capacitance			16	25	pF
$C_{rss}$	Reverse Transfer Capacitance			0.7	5	pF
$R_g$	Gate Resistance		0.1	3	7.5	$\Omega$

### Switching Characteristics

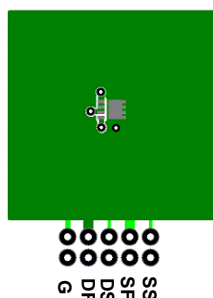
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\text{ V}$ , $I_D = -1\text{ A}$ , $V_{GS} = -10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		5.8	12	ns
$t_r$	Rise Time			2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			8	16	ns
$t_f$	Fall Time			6.4	13	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$		2.8	4
$Q_{gs}$	Total Gate Charge	$V_{DD} = -75\text{ V}$ , $I_D = -1\text{ A}$		0.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.7		nC

### Drain-Source Diode Characteristics

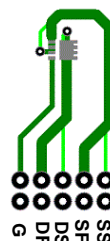
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -1\text{ A}$ (Note 2)		-0.87	-1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = -1\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		50	80	ns
$Q_{rr}$	Reverse Recovery Charge			78	124	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $53\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper

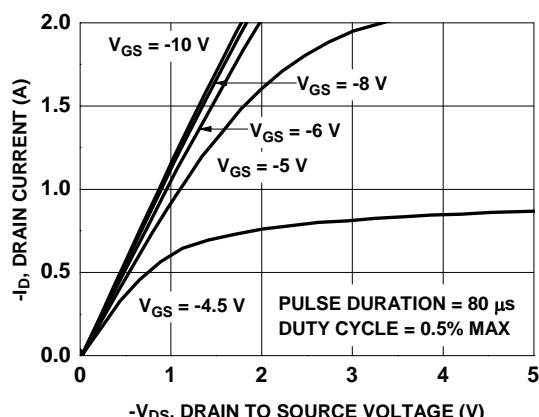


b)  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

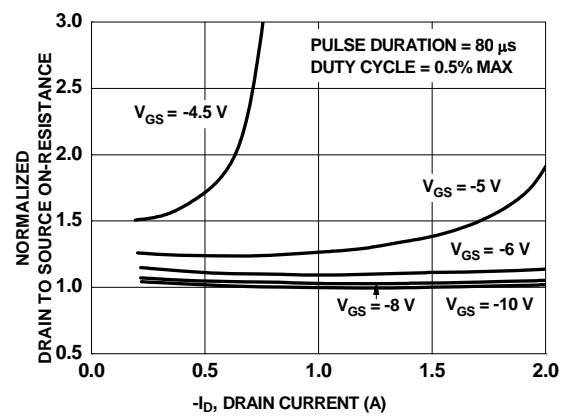
- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

- Starting  $T_J = 25\text{ }^\circ\text{C}$ ; P-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = -2\text{ A}$ ,  $V_{DD} = -150\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = -9\text{ A}$ .

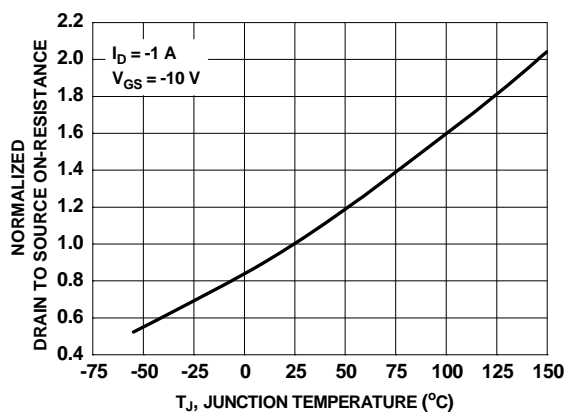
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



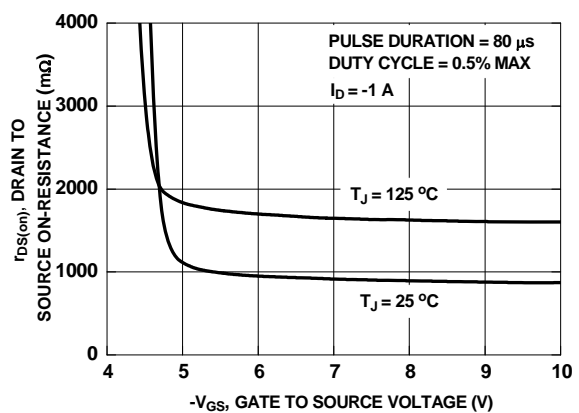
**Figure 1. On Region Characteristics**



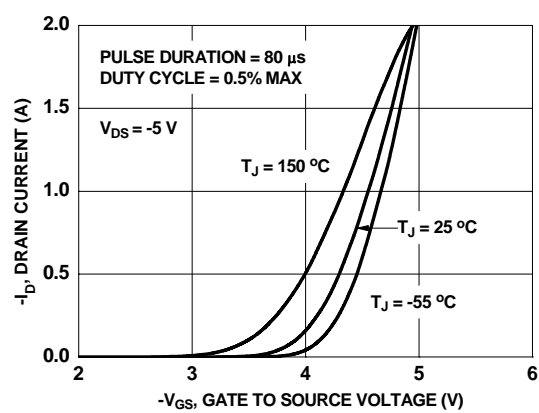
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



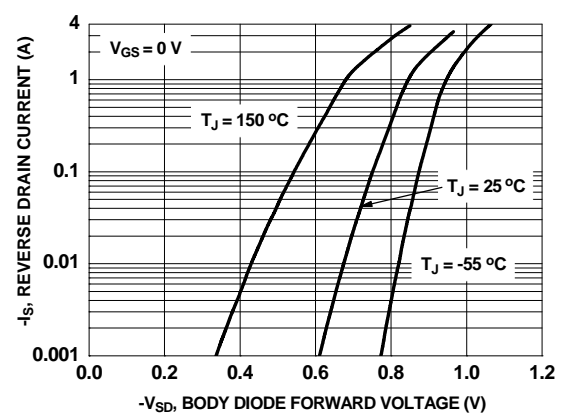
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

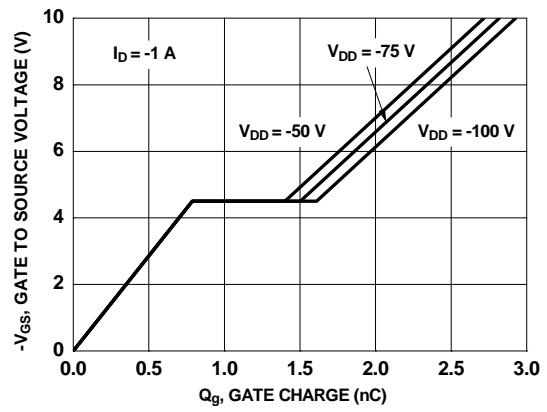


**Figure 5. Transfer Characteristics**

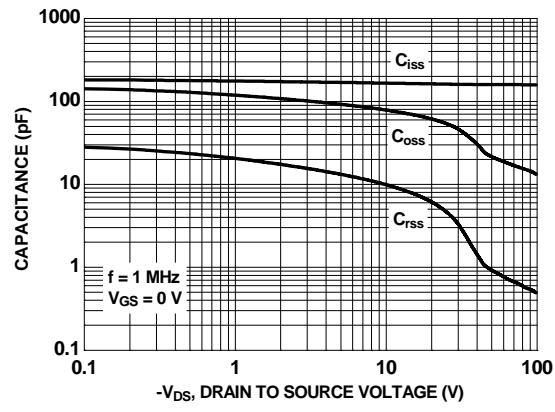


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

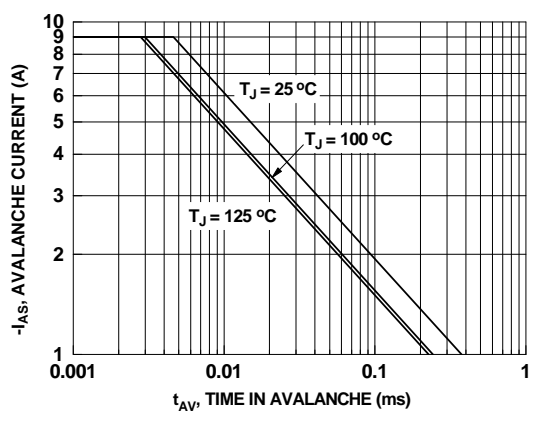
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



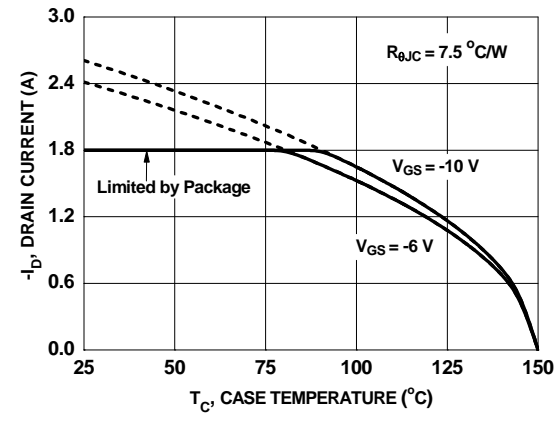
**Figure 7. Gate Charge Characteristics**



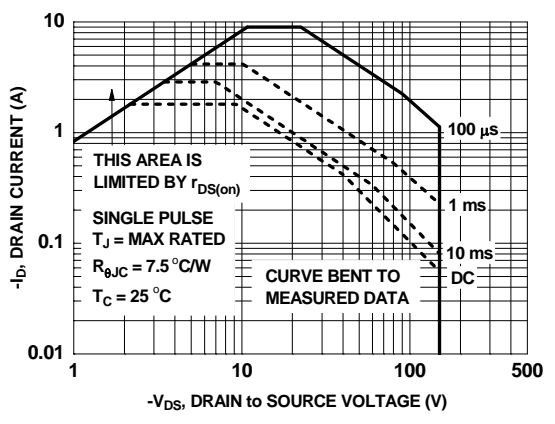
**Figure 8. Capacitance vs Drain to Source Voltage**



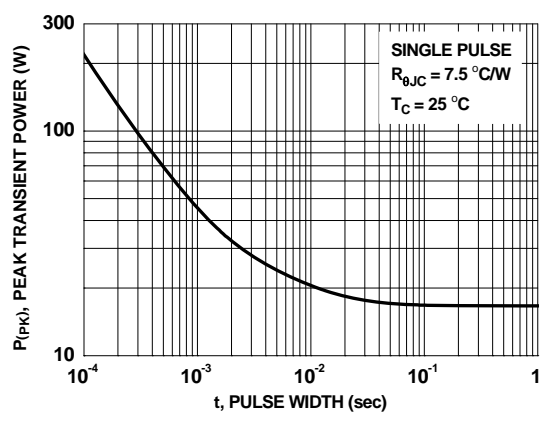
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

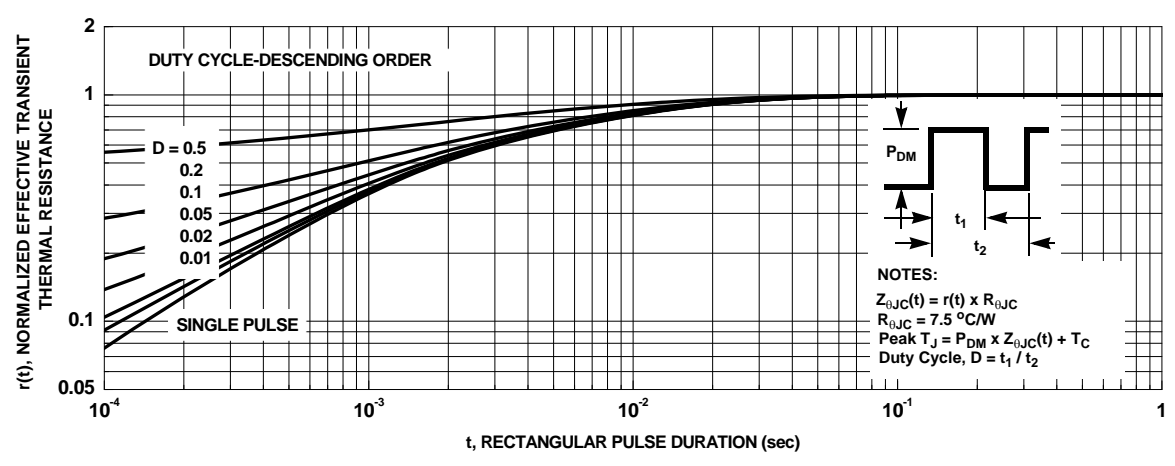


**Figure 11. Forward Bias Safe Operating Area**



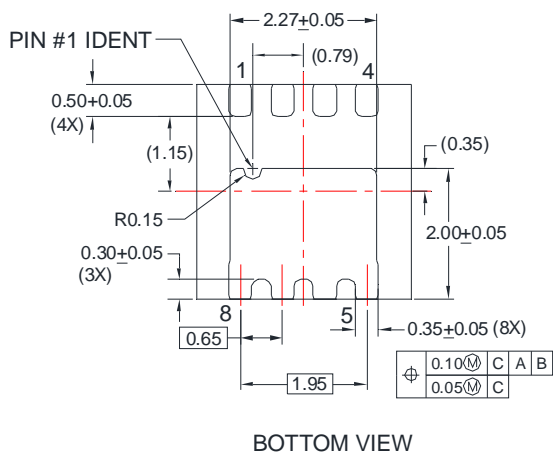
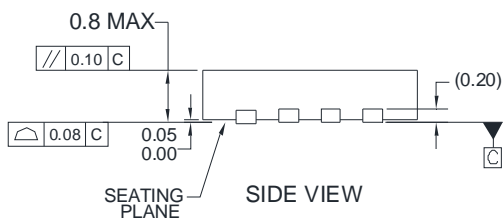
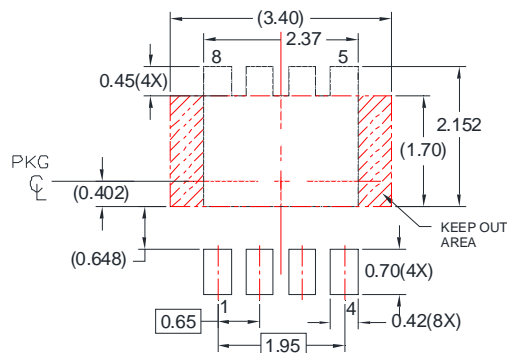
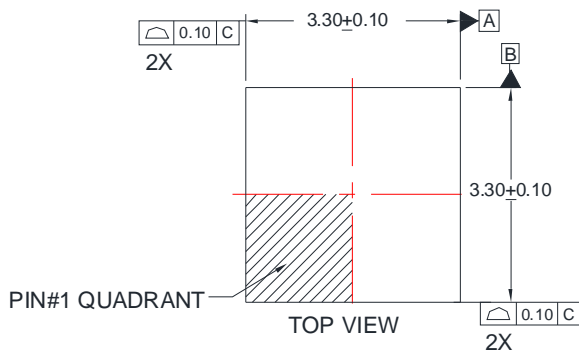
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



### NOTES:

- DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
- DRAWING FILE NAME : MKT-MLP08Srev2
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| ESBC™   | MicroFET™                                       | SuperFET®                   | UHC®             |
|  | MicroPak™                                       | SuperSOT™-3                 | Ultra FRFET™     |
| Fairchild®  | MicroPak2™                                      | SuperSOT™-6                 | UniFET™          |
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| FastvCore™  | OPTOLOGIC®                                      |                             | 仙童™              |
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