FAIRCHILD™

October 2014

FDMS8023S

N-Channel PowerTrench® SyncFET™

30 V, 49 A, 2.4 mΩ

Features

- Max $r_{DS(on)}$ = 2.4 mΩ at V_{GS} = 10 V, I_D = 26 A
- Max $r_{DS(on)}$ = 3.0 mΩ at V_{GS} = 4.5 V, I_D = 23 A
- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

The FDMS8023S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance.This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification

Top

Bottom ← Pin 1

S
S
S G

D D D D

Power 56

D	5		4	G
D	6		3	S
D	7		2	S
D	8		1	S
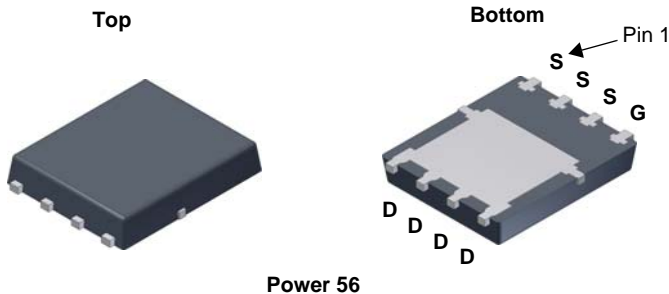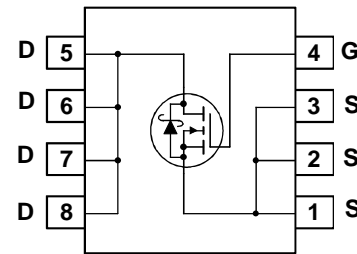
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage		(Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		49	A
	-Continuous (Silicon limited)	T_C = 25°C		128	
	-Continuous	T_A = 25°C	(Note 1a)	26	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	86	mJ
P_D	Power Dissipation	T_C = 25°C		59	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{θJC}$	Thermal Resistance, Junction to Case			2.1	°C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient		(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8023S	FDMS8023S	Power 56	13 "	12 mm	3000 units

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Electrical Characteristics $T_J = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1$ mA, $V_{GS} = 0$ V	30			V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10$ mA, referenced to 25°C		16		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V			500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1$ mA	1.2	1.7	3.0	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10$ mA, referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10$ V, $I_D = 26$ A		2.0	2.4	mΩ
		$V_{GS} = 4.5$ V, $I_D = 23$ A		2.6	3.0	
		$V_{GS} = 10$ V, $I_D = 26$ A, $T_J = 125°C$		2.7	3.3	
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 26$ A		168		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, f = 1MHz		2670	3550	pF
C_{oss}	Output Capacitance			975	1300	pF
C_{rss}	Reverse Transfer Capacitance			95	140	pF
R_g	Gate Resistance			0.7	2.5	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15$ V, $I_D = 26$ A, $V_{GS} = 10$ V, $R_{GEN} = 6$ Ω		12	21	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			32	52	ns
t_f	Fall Time			4	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0$ V to 10 V, $V_{DD} = 15$ V, $I_D = 26$ A		41	57	nC
Q_g	Total Gate Charge	$V_{GS} = 0$ V to 4.5 V		20	28	nC
Q_{gs}	Gate to Source Charge			7.0		nC
Q_{gd}	Gate to Drain "Miller" Charge			5.4		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 2$ A (Note 2)		0.63	0.8	V
		$V_{GS} = 0$ V, $I_S = 26$ A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 26$ A, di/dt = 300 A/μs		29	46	ns
Q_{rr}	Reverse Recovery Charge			32	51	nC

Notes:

1. $R_{θJA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design.
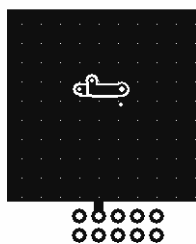
a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.

b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 86 mJ is based on starting $T_J = 25$ °C, L = 0.3 mH, $I_{AS} = 24$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

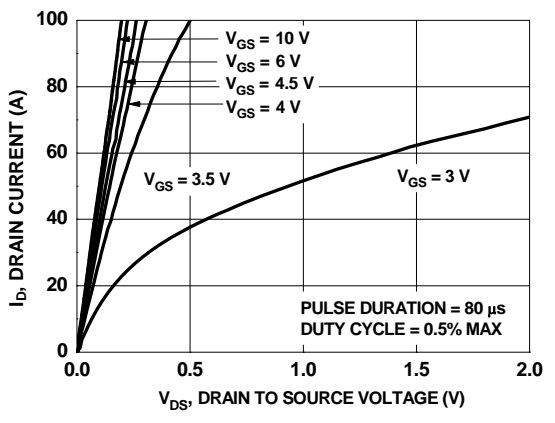## Typical Characteristics T_J = 25°C unless otherwise noted
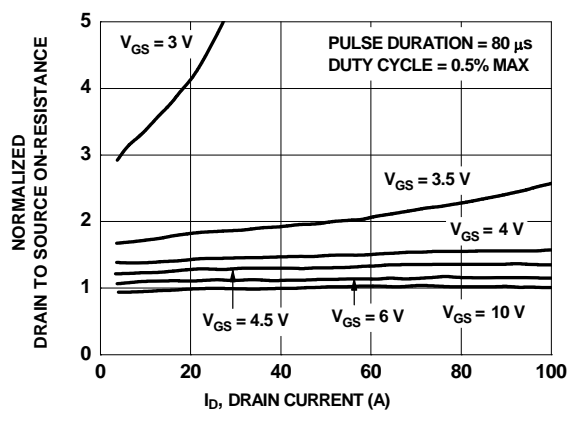

Figure 1. On Region Characteristics

Figure 2. Normalized On-Resistance
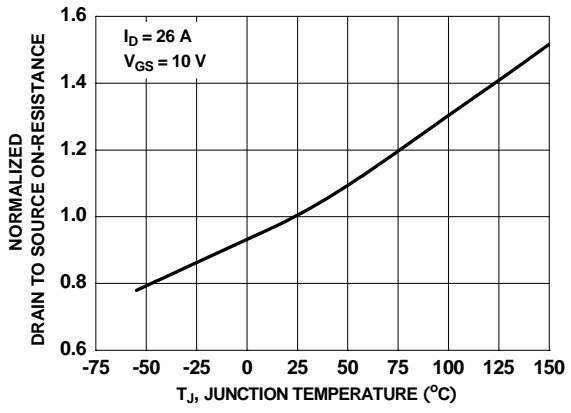vs Drain Current and Gate Voltage

Figure 3. Normalized On Resistance
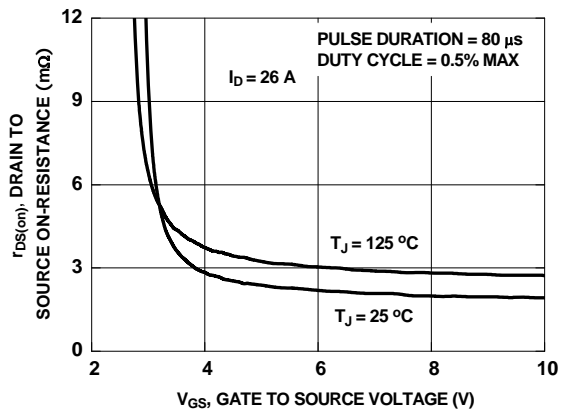vs Junction Temperature
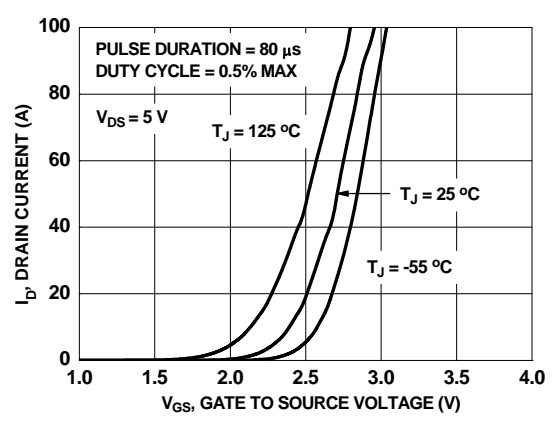

Figure 4. On-Resistance vs Gate to
Source Voltage

Figure 5. Transfer Characteristics
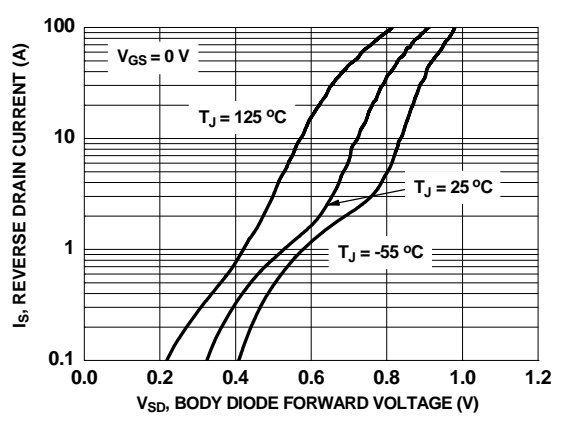

Figure 6. Source to Drain Diode
Forward Voltage vs Source Current

FDMS8023S Rev.C2

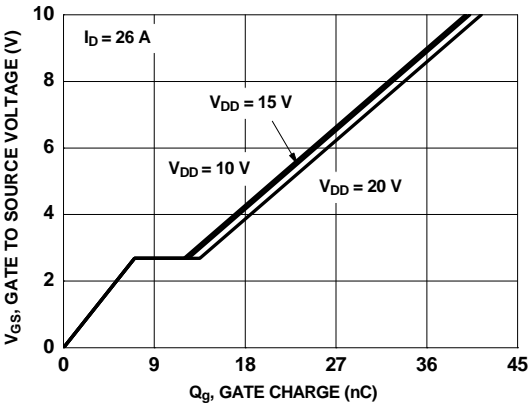**Typical Characteristics** $T_J = 25°C$ unless otherwise noted

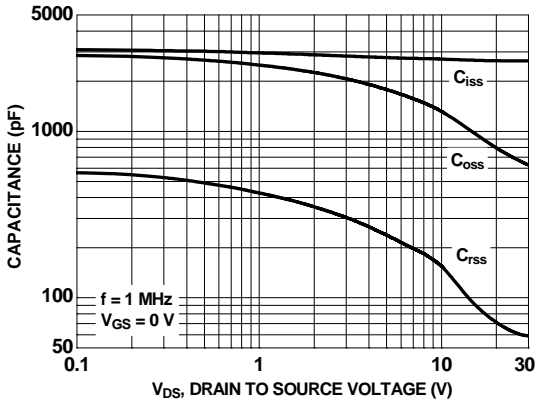Figure 7. Gate Charge Characteristics

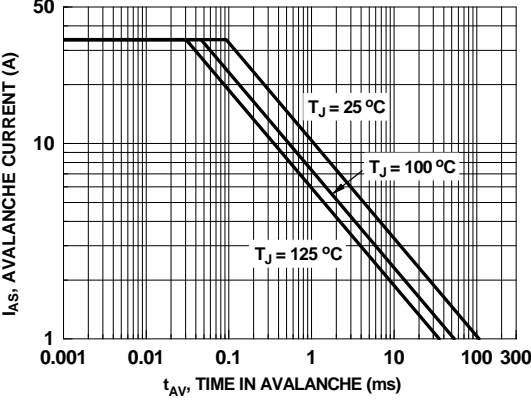Figure 8. Capacitance vs Drain to Source Voltage

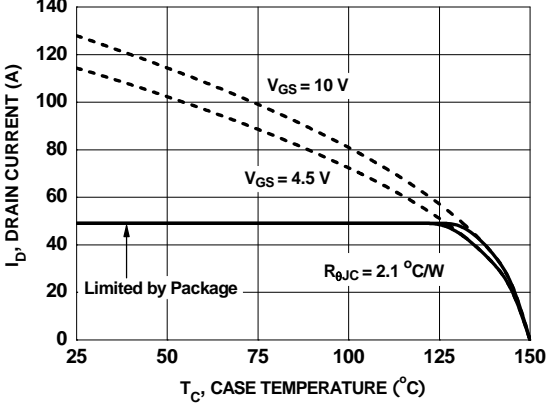Figure 9. Unclamped Inductive Switching Capability

Figure 10. Maximum Continuous Drain Current vs Case Temperature
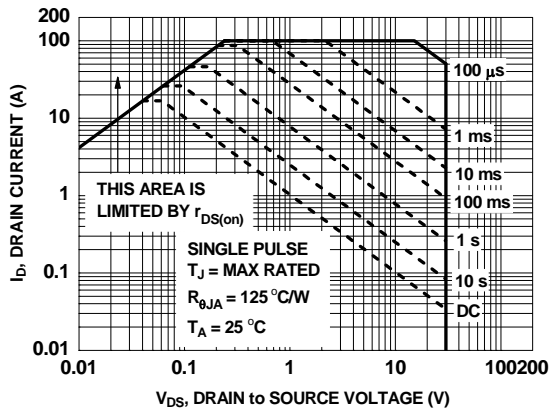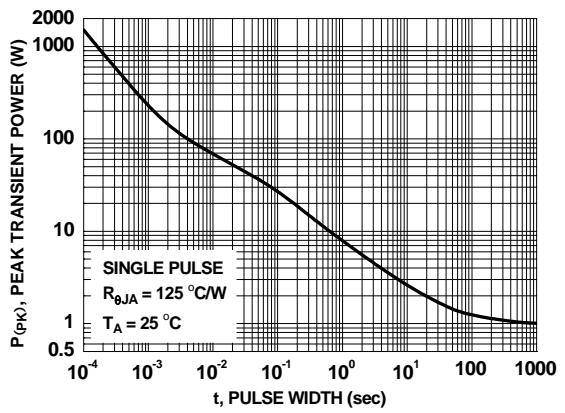

Figure 11. Forward Bias Safe Operating Area

Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted
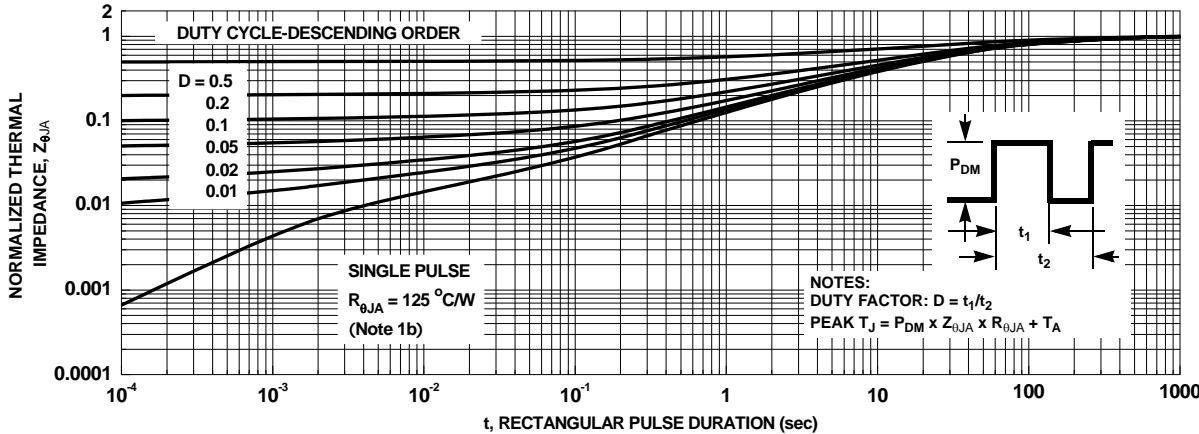
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8023S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

Figure 14. FDMS8023S SyncFET body diode reverse recovery characteristic

Figure 15. SyncFET body diode reverse leakage versus drain-source voltage

TOP VIEW

5.10 A

PKG ℄

8   5

PKG ℄

1   4

6.15

SEE DETAIL B

5.85
5.65

LAND PATTERN RECOMMENDATION

5.10
3.91
0.64
1.27

8 7 6 5

0.77

4.52

3.75

6.61

KEEP OUT AREA

1.27

1 2 3 4

1.27

0.61

3.81

SIDE VIEW
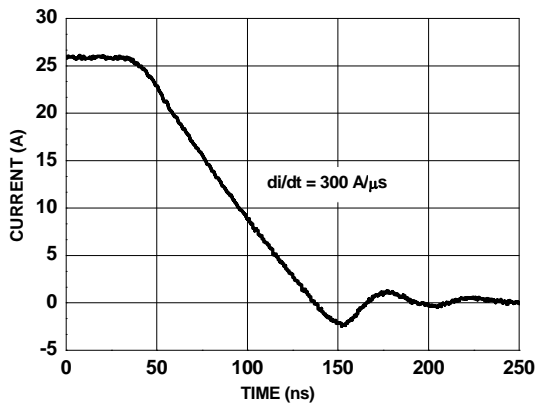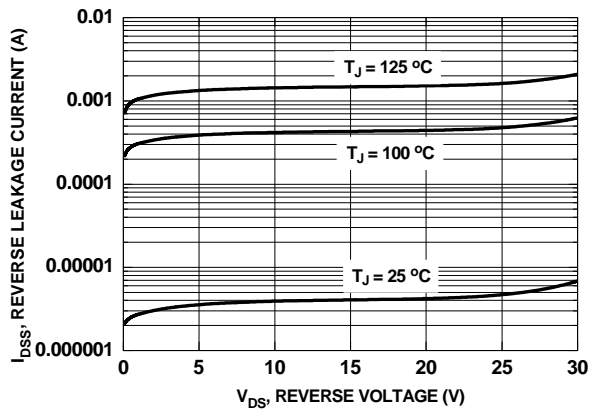
5.00
4.80

SEE DETAIL C

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE

0°-12°

// 0.10 C

8X
⌓ 0.08 C

0.05
0.00

0.35
0.15

1.10
0.90

C

SEATING PLANE

DETAIL C
SCALE: 2:1

0.35
0.15

0.30
0.05

0°-12°
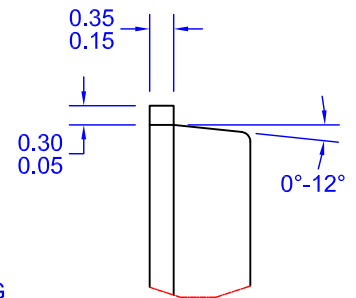
DETAIL B
SCALE: 2:1

BOTTOM VIEW

5.20
4.80

3.81

1.27

(0.34)

0.51
0.31 (8X)

⊕ 0.10(M) C A B

1 2   3 4

0.76
0.51

(0.52)

6.25
5.90

(0.50)

(0.30)
(2X)

3.48 +0.30 -0.10

8 7   6 5

0.20 +0.10 -0.15 (8X)

3.96
3.61

0.44±0.10

NOTES: UNLESS OTHERWISE SPECIFIED
A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F. DRAWING FILE NAME: PQFN08AREV10

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