FAIRCHILD™

October 2014

FDMS86250

N-Channel Shielded Gate PowerTrench® MOSFET

150 V, 30 A, 25 mΩ

Features

- Shielded Gate MOSFET Technology

- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = 10 V, I_D = 6.7 A

- Max $r_{DS(on)}$ = 33 mΩ at V_{GS} = 6 V, I_D = 5.8 A

- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency

- MSL1 robust package design

- 100% UIL tested

- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

- DC-DC Conversion

Top

Bottom

Pin 1

S S S G

D D D D

Power 56

S 1   8 D
S 2   7 D
S 3   6 D
G 4   5 D
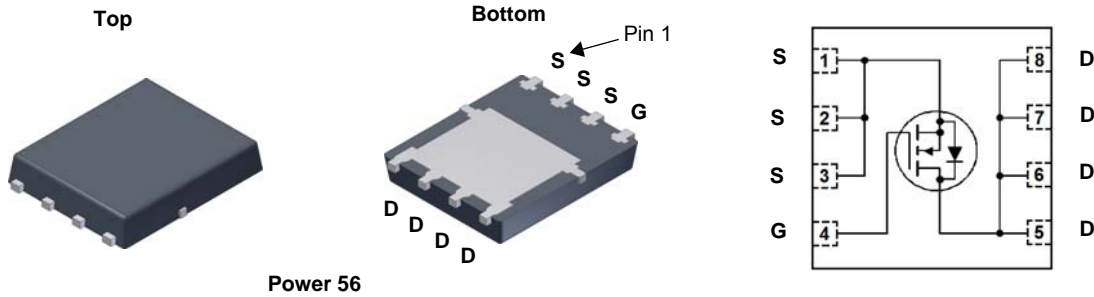
MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			150	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		30	A
	-Continuous	T_A = 25 °C	(Note 1a)	6.7	
	-Pulsed		(Note 4)	100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	180	mJ
P_D	Power Dissipation	T_C = 25 °C		96	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86250	FDMS86250	Power 56	13 ''	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		106		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6.7 A		19	25	mΩ
		V_{GS} = 6 V, I_D = 5.8 A		23	33	
		V_{GS} = 10 V, I_D = 6.7 A, T_J = 125 °C		35	46	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 6.7 A		24		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz		1750	2330	pF
C_{oss}	Output Capacitance			165	220	pF
C_{rss}	Reverse Transfer Capacitance			8.8	15	pF
R_g	Gate Resistance			0.5		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 75 V, I_D = 6.7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		14	25	ns
t_r	Rise Time			4.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
t_f	Fall Time			4.2	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V		25	36	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V	V_{DD} = 75 V, I_D = 6.7 A	14	20	nC
Q_{gs}	Gate to Source Charge			7.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			5.5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.72	1.2	V
		V_{GS} = 0 V, I_S = 6.7 A (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	I_F = 6.7 A, di/dt = 100 A/µs		73	117	ns
Q_{rr}	Reverse Recovery Charge			112	180	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
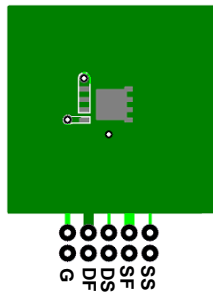
a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.
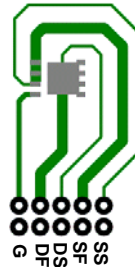
b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C, L = 1 mH, I_{AS} = 19 A, V_{DD} = 135 V, V_{GS} = 10 V.

4. Pulse Id limited by junction temperature, td ≤ 100 µs. Please refer to SOA curve for more details.

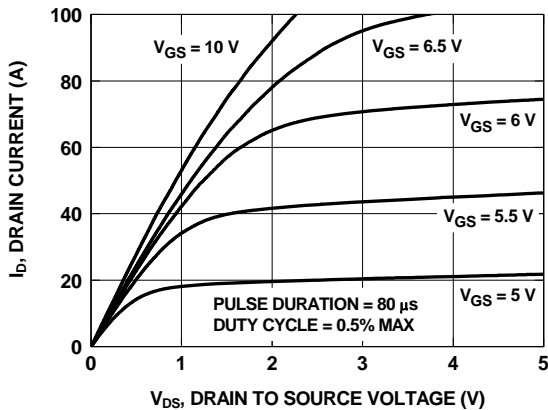**Typical Characteristics** T_J = 25 °C unless otherwise noted

Figure 1. On-Region Characteristics
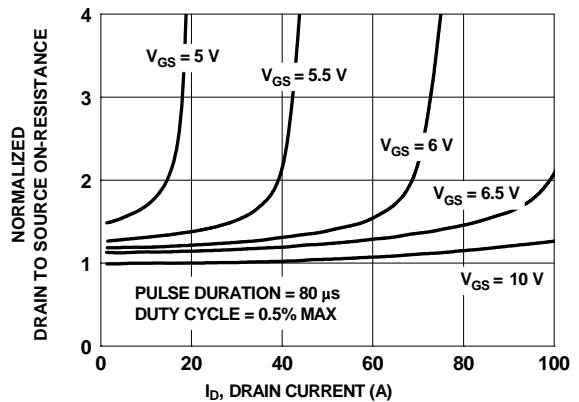

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
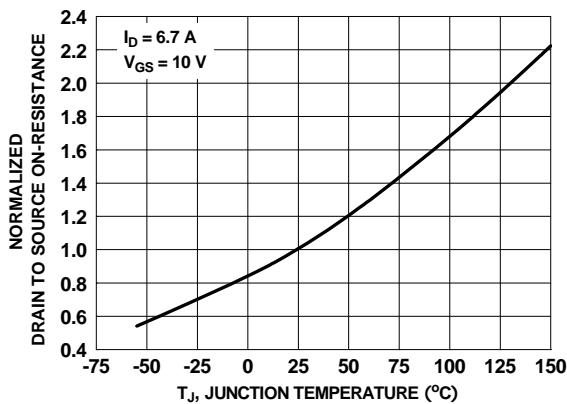

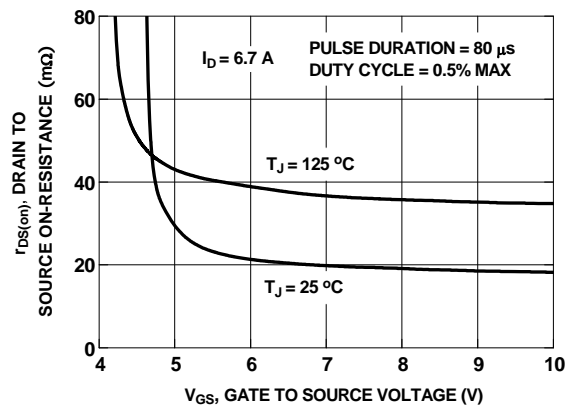**Figure 3. Normalized On-Resistance vs Junction Temperature**
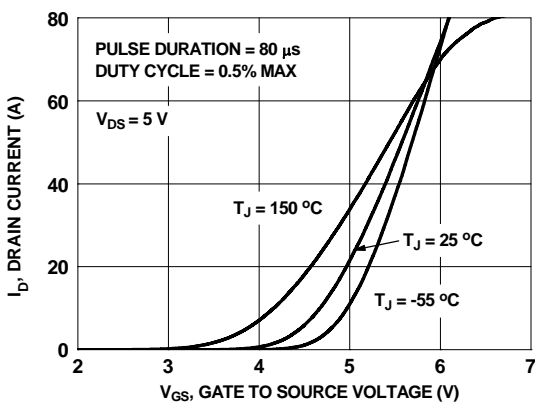

Figure 4. On-Resistance vs Gate to Source Voltage
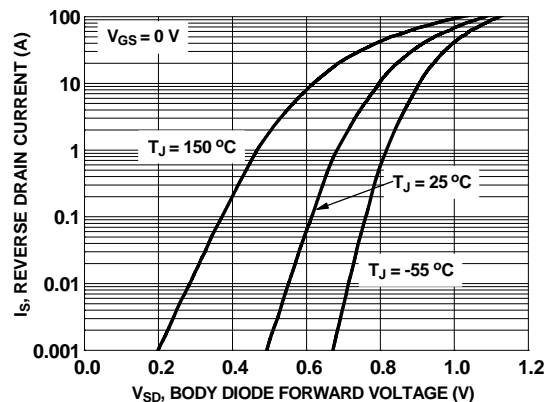

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

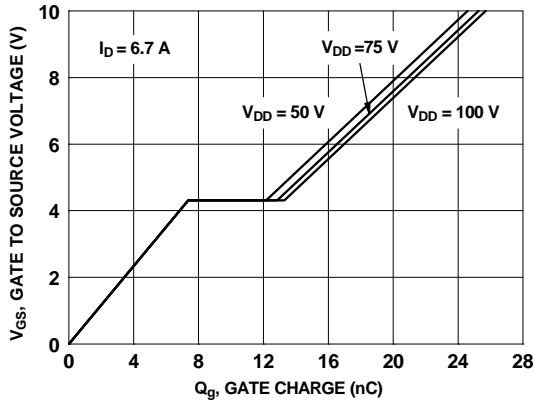## Typical Characteristics $T_J = 25\ °C$ unless otherwise noted

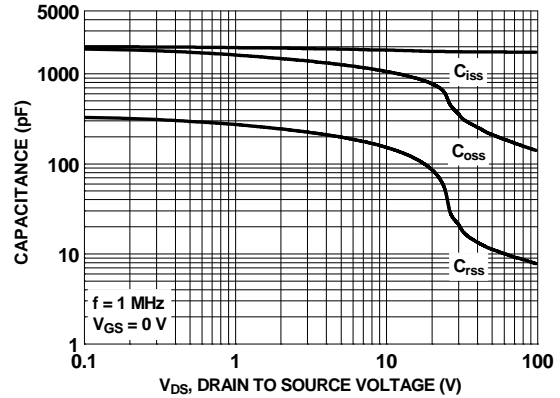**Figure 7. Gate Charge Characteristics**

Figure 8. Capacitance vs Drain to Source Voltage
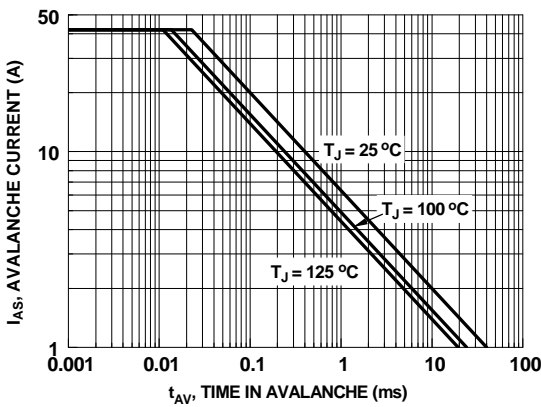

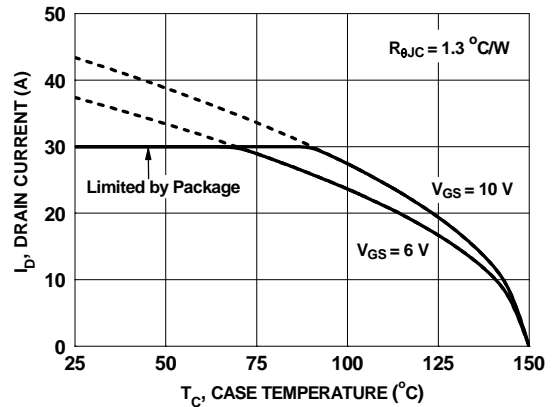**Figure 9. Unclamped Inductive Switching Capability**

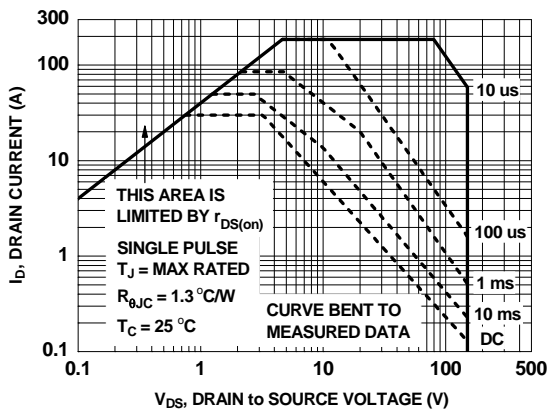**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

Figure 11. Forward Bias Safe Operating Area
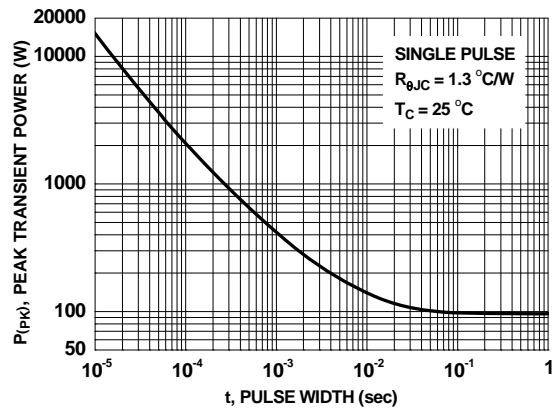
Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE

t, RECTANGULAR PULSE DURATION (sec)

NOTES:
$Z_{\theta JC}(t) = r(t) \times R_{\theta JC}$
$R_{\theta JC} = 1.3$ °C/W
Peak $T_J = P_{DM} \times Z_{\theta JC}(t) + T_C$
Duty Cycle, $D = t_1 / t_2$
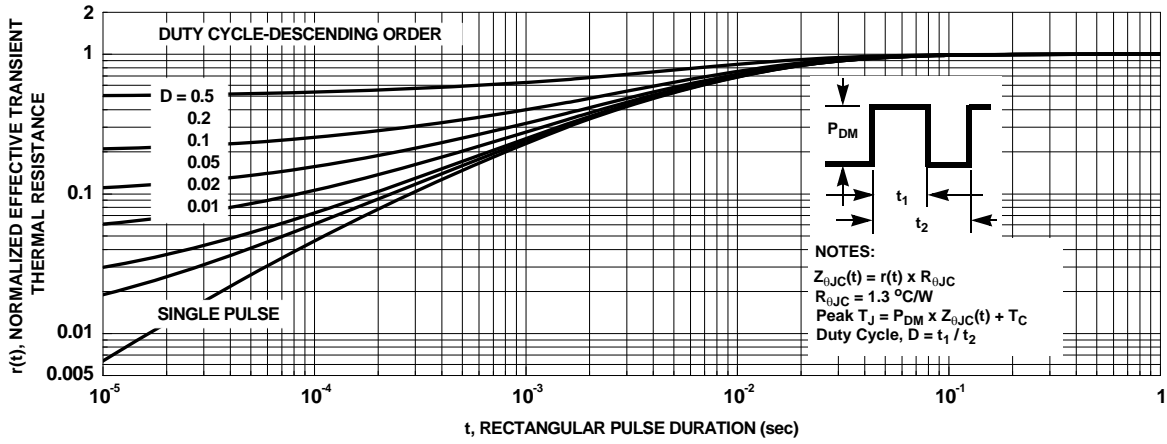
Figure 13. Junction-to-Case Transient Thermal Response Curve

TOP VIEW

5.10 — A

PKG ℄

PKG ℄

6.15

8 5

1 4

SIDE VIEW

5.00 / 4.80

SEE DETAIL C

BOTTOM VIEW

5.20 / 4.80

3.81

1.27

(0.34)

0.51 / 0.31 (8X)

⊕ | 0.10 Ⓜ | C | A | B

1 2 3 4

0.76 / 0.51

(0.52)

(0.50)

6.25 / 5.90

(0.30) (2X)

$3.48^{+0.30}_{-0.10}$

8 7 6 5

$0.20^{+0.10}_{-0.15}$ (8X)

3.96 / 3.61

0.44±0.10

SEE DETAIL B

5.85 / 5.65
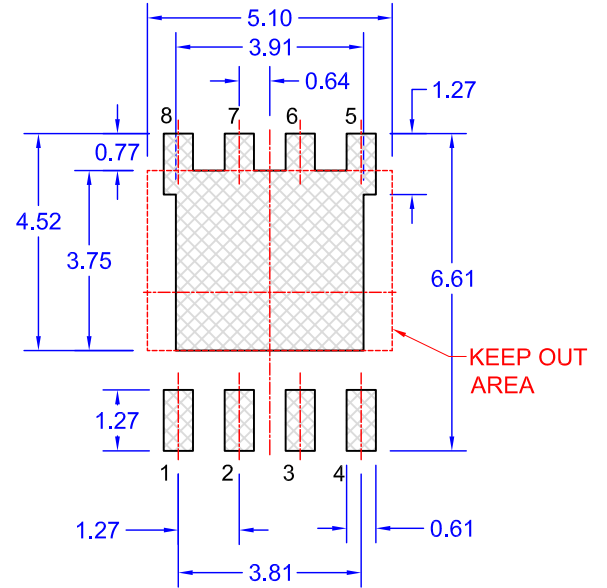
LAND PATTERN RECOMMENDATION

5.10

3.91

0.64

1.27

8 7 6 5

0.77

4.52

3.75

6.61

KEEP OUT AREA

1.27

1 2 3 4

1.27

0.61

3.81

DETAIL C
SCALE: 2:1

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE

0°-12°

// | 0.10 | C

0.05 / 0.00

8X

⌓ | 0.08 | C

0.35 / 0.15

1.10 / 0.90

C

SEATING PLANE

DETAIL B
SCALE: 2:1

0.35 / 0.15

0.30 / 0.05

0°-12°
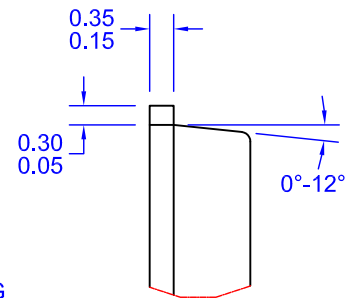
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A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.

B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F. DRAWING FILE NAME: PQFN08AREV10

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