

FDP18N20F / FDPF18N20FT

N-Channel UniFET™ FRFET® MOSFET

200 V, 18 A, 140 mΩ

Features

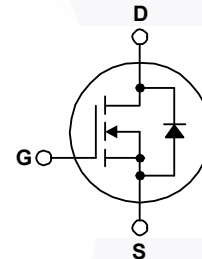
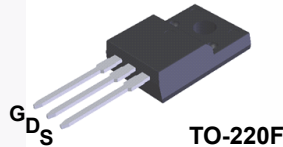
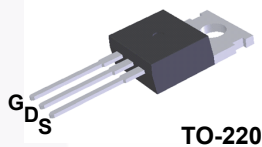
- $R_{DS(on)} = 120 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 9 \text{ A}$
- Low Gate Charge (Typ. 20 nC)
- Low C_{rss} (Typ. 24 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- LCD/LED TV
- Consumer Appliances
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP18N20F	FDPF18N20FT	Unit
V_{DSS}	Drain to Source Voltage	200		V
V_{GSS}	Gate to Source Voltage	±30		V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	18	18*
		- Continuous ($T_C = 100^\circ\text{C}$)	10.8	10.8*
I_{DM}	Drain Current	- Pulsed (Note 1)	72	72*
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	324		mJ
I_{AR}	Avalanche Current (Note 1)	18		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	10		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	100	41
		- Derate Above 25°C	0.83	0.33
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FDP18N20F	FDPF18N20FT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.2	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP18N20F	FDP18N20F	TO-220	Tube	N/A	N/A	50 units
FDPF18N20FT	FDPF18N20FT	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}, T_J = 25^\circ\text{C}$	200	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.2	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200 \text{V}, V_{GS} = 0 \text{V}$	-	-	10	μA
		$V_{DS} = 160 \text{V}, T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{V}, V_{DS} = 0 \text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{V}, I_D = 9 \text{A}$	-	0.12	0.14	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{V}, I_D = 9 \text{A}$	-	13.6	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{V}, V_{GS} = 0 \text{V}, f = 1 \text{MHz}$	-	885	1180	pF
C_{oss}	Output Capacitance		-	200	270	pF
C_{rss}	Reverse Transfer Capacitance		-	24	35	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 160 \text{V}, I_D = 18 \text{A}, V_{GS} = 10 \text{V}$	-	20	26	nC
Q_{gs}	Gate to Source Gate Charge		-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	9	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100 \text{V}, I_D = 18 \text{A}, V_{GS} = 10 \text{V}, R_G = 25 \Omega$	-	16	40	ns
t_r	Turn-On Rise Time		-	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	110	ns
t_f	Turn-Off Fall Time		(Note 4)	-	40	90

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	18	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	72	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{V}, I_{SD} = 18 \text{A}$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{V}, I_{SD} = 18 \text{A}, di_F/dt = 100 \text{A}/\mu\text{s}$	-	80	-	ns
Q_{rr}	Reverse Recovery Charge		-	240	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 2 \text{mH}, I_{AS} = 18 \text{A}, V_{DD} = 50 \text{V}, R_G = 2.5 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 18 \text{A}, di/dt \leq 200 \text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

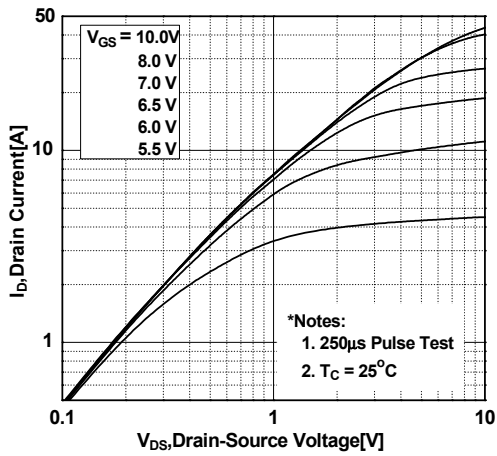


Figure 2. Transfer Characteristics

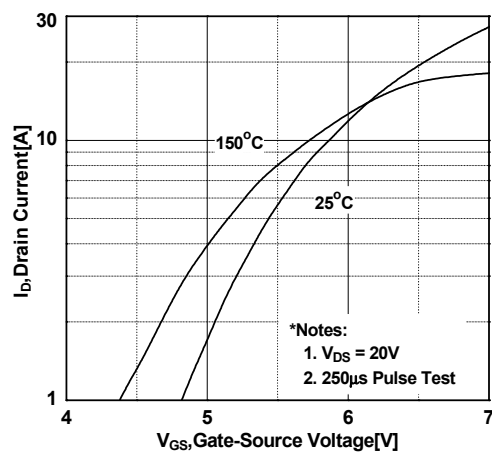


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

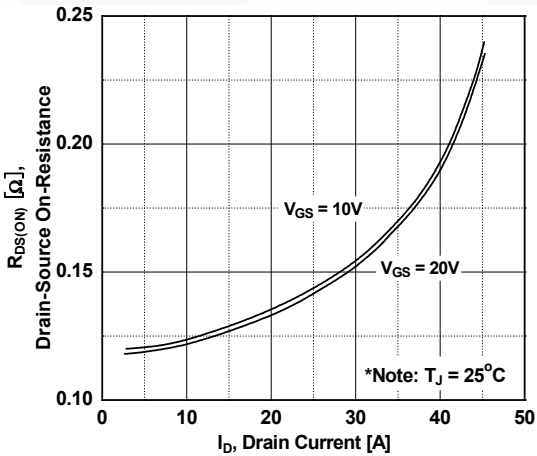


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

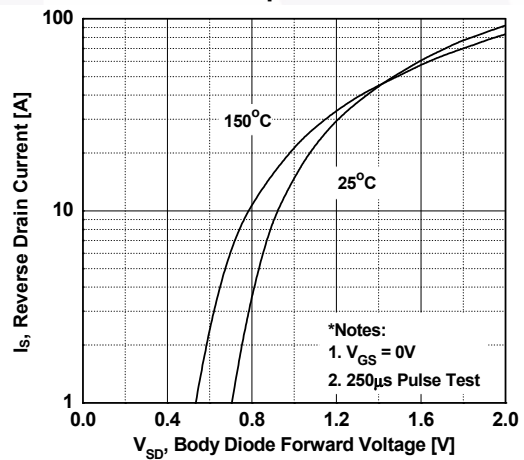


Figure 5. Capacitance Characteristics

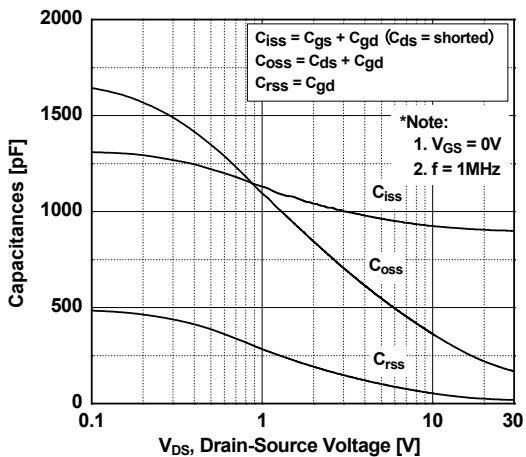
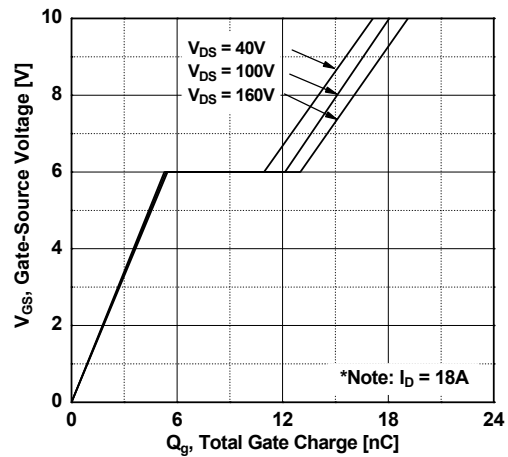


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

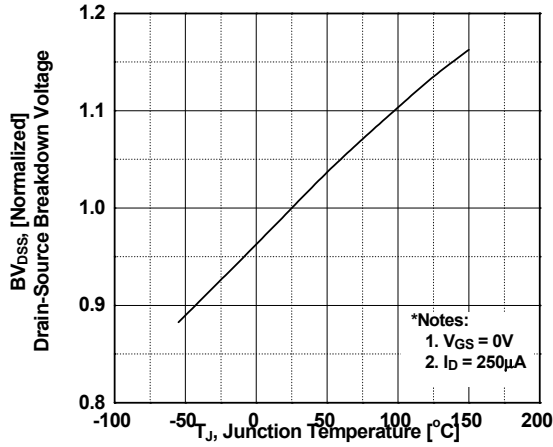


Figure 8-1. Maximum Safe Operating Area - FDP18N20F

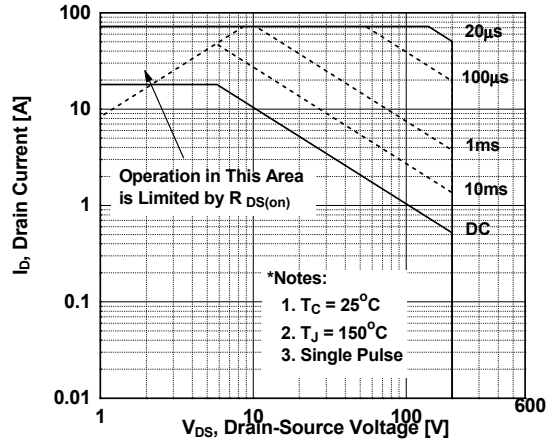


Figure 8-2. Maximum Safe Operating Area - FDPF18N20FT

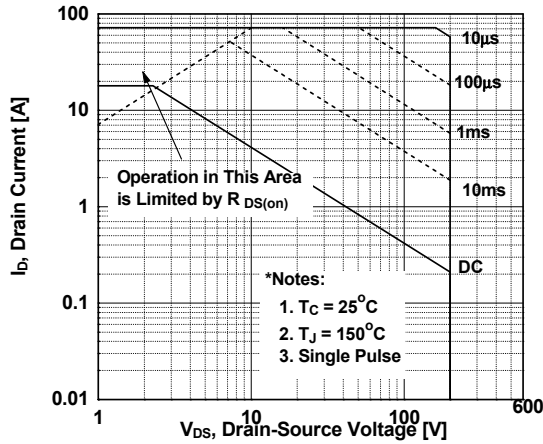


Figure 9. Maximum Drain Current vs. Case Temperature

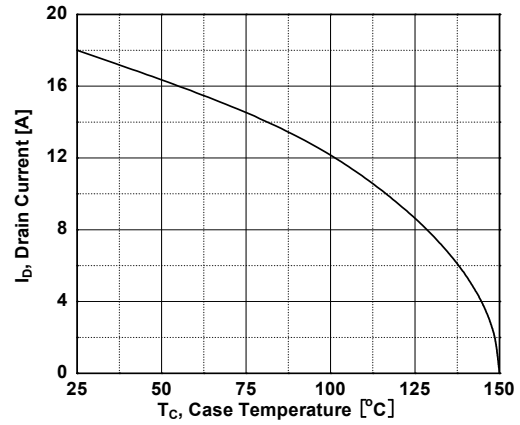


Figure 10-1. Transient Thermal Response Curve - FDP18N20F

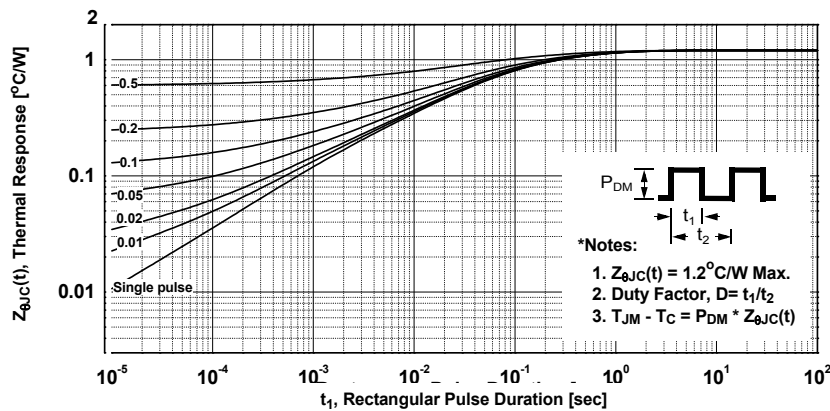


Figure 10-2. Transient Thermal Response Curve - FDPF18N20FT

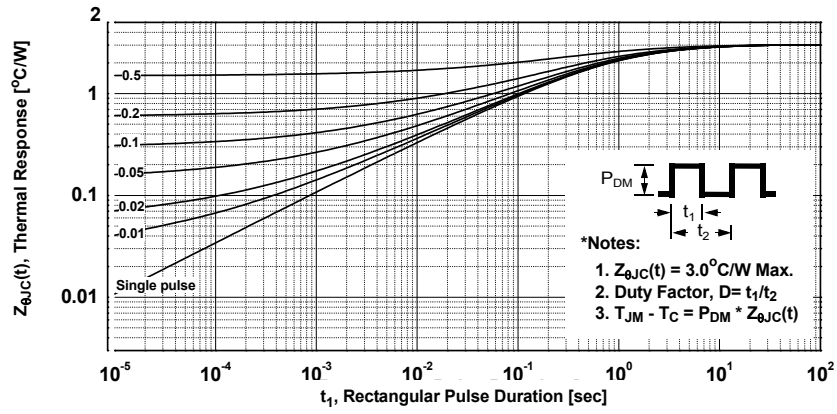




Figure 11. Gate Charge Test Circuit & Waveform



Figure 12. Resistive Switching Test Circuit & Waveforms

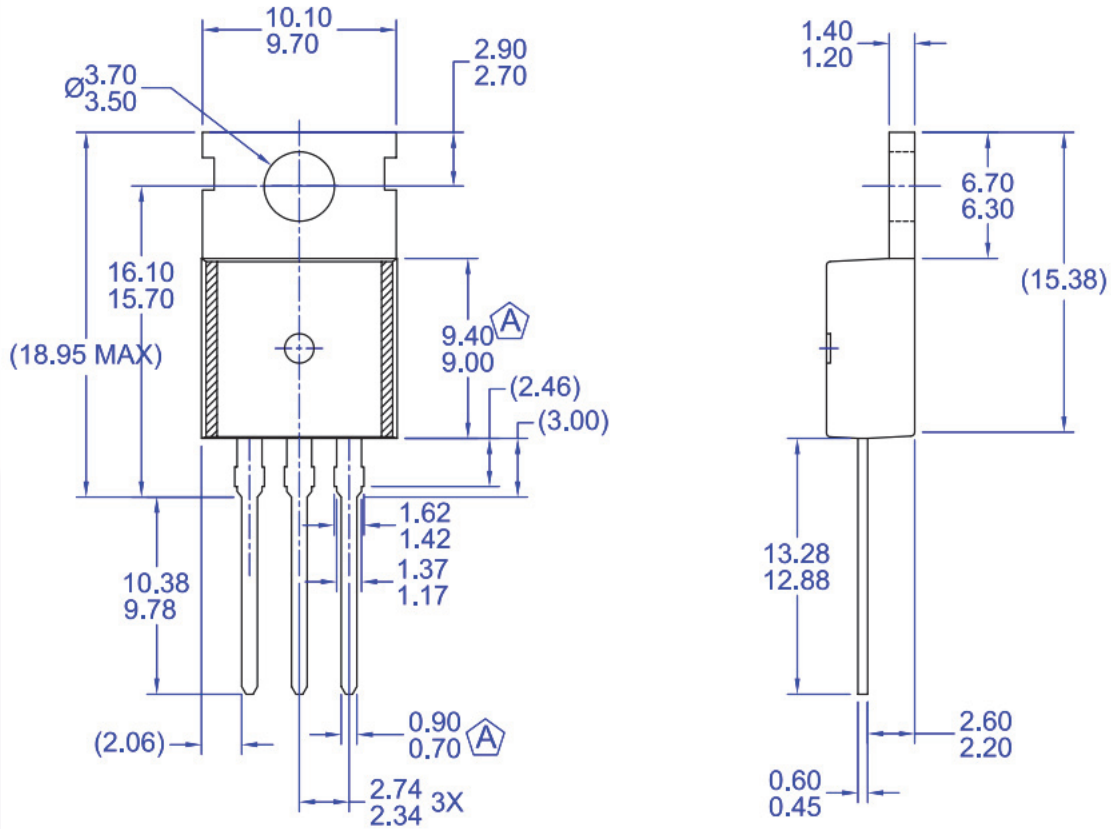


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

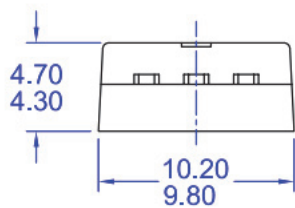


Figure 15. TO220, Molded, 3-Lead, Jedec Variation AB

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Mechanical Dimensions

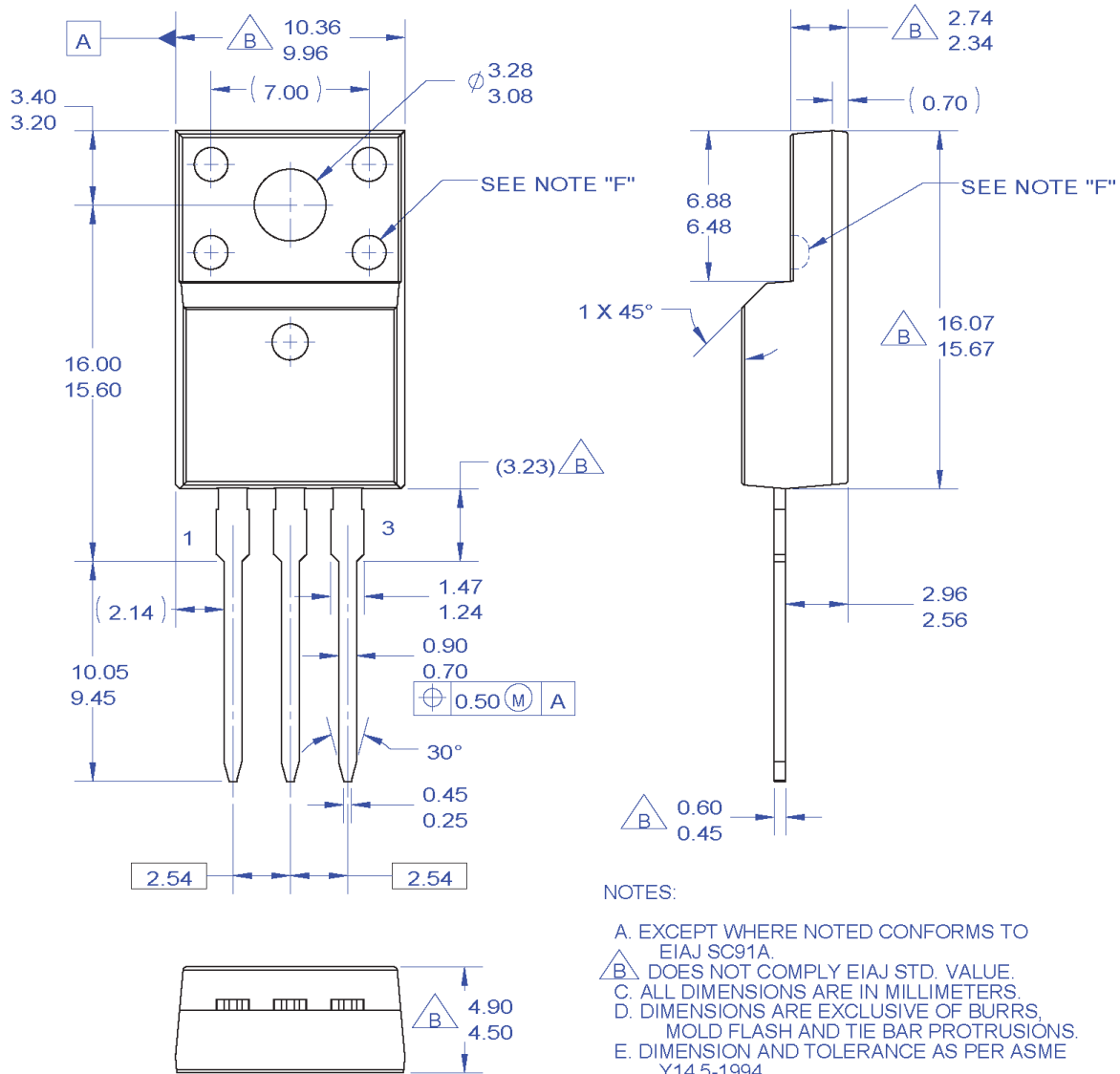


Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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