

# FDD3N40 / FDU3N40

## N-Channel UniFET™ MOSFET

400 V, 2 A, 3.4 Ω

### Features

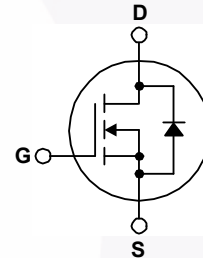
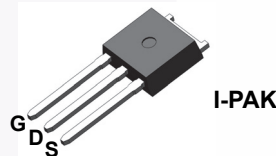
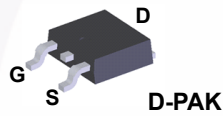
- $R_{DS(on)} = 3.4 \Omega$  (Typ.) @  $V_{GS} = 10 V, I_D = 1 A$
- Low Gate Charge (Typ. 4.5 nC)
- Low  $C_{rss}$  (Typ. 3.7 pF)
- 100% Avalanche Tested

### Applications

- LED TV
- Consumer Appliances
- Lighting
- Uninterruptible Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FDD3N40TM / FDU3N40TU	Unit
$V_{DSS}$	Drain-Source Voltage	400	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ C$ ) - Continuous ( $T_C = 100^\circ C$ )	A A
$I_{DM}$	Drain Current	- Pulsed (Note 1)	8.0 A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2) 46	mJ
$I_{AR}$	Avalanche Current	(Note 1) 2	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1) 3	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3) 4.5	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ C$ ) - Derate Above $25^\circ C$	30 W 0.24 W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FDD3N40TM / FDU3N40TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	4.2	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	$^\circ C/W$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD3N40TM	FDD3N40	DKPAK	Tape and Reel	330 mm	16 mm	2500 units
FDU3N40TU	FDU3N40	IPAK	Tube	N/A	N/A	75 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

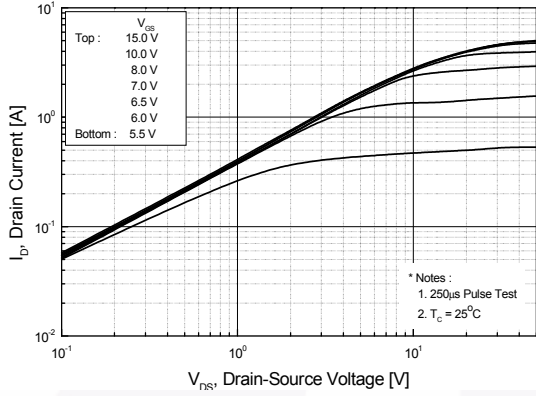
Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	400	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.4	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 320 V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1 A	--	2.8	3.4	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 1 A	--	2	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	--	173	225	pF
C <sub>oss</sub>	Output Capacitance		--	30	40	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	3.7	6	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 200 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 25 Ω  (Note 4)	--	10	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	30	70	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	10	30	ns
t <sub>f</sub>	Turn-Off Fall Time		--	25	60	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 320 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V  (Note 4)	--	4.5	6	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.2	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	2	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	2	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	8	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A, di/dt = 100 A/μs	--	210	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.75	--	μC

### Notes:

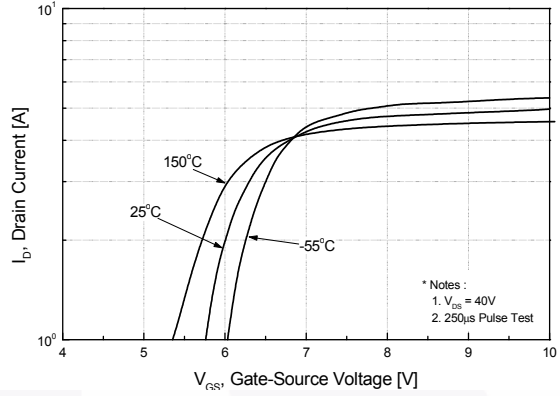
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 20 mH, I<sub>AS</sub> = 2 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 2 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

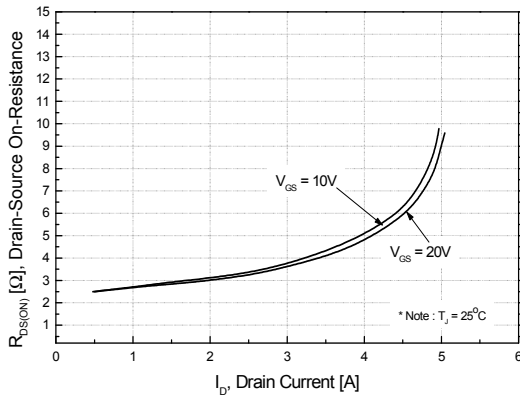
**Figure 1. On-Region Characteristics**



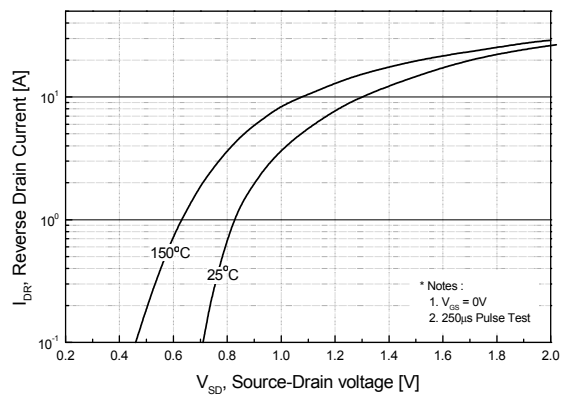
**Figure 2. Transfer Characteristics**



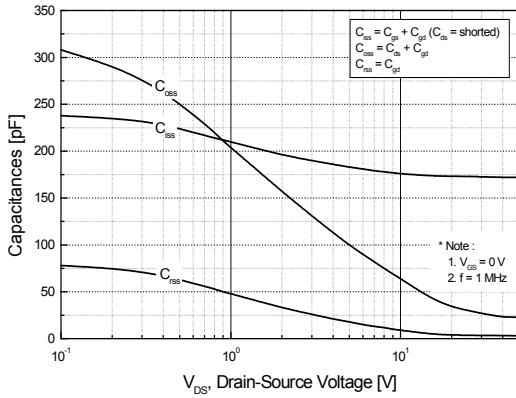
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



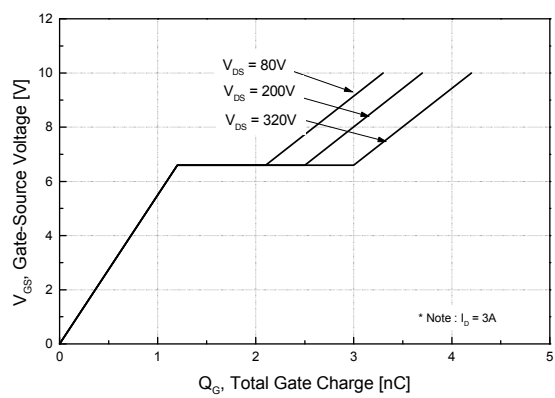
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

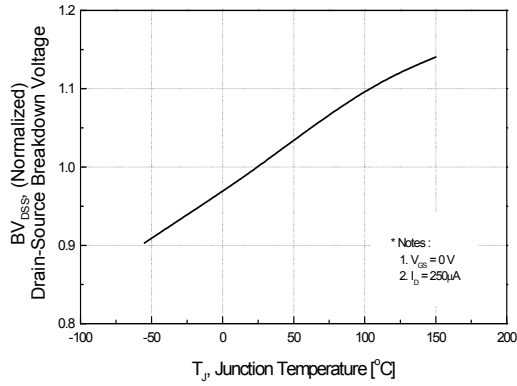


**Figure 6. Gate Charge Characteristics**

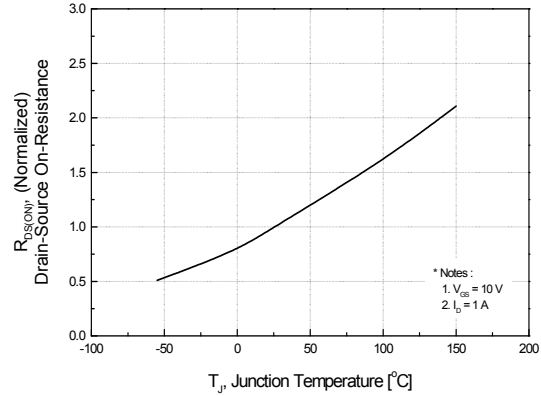


**Typical Performance Characteristics** (Continued)

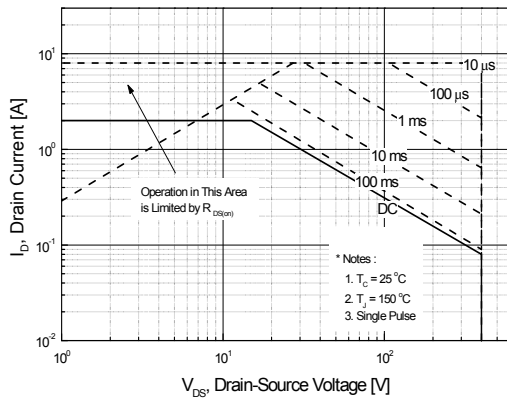
**Figure 7. Breakdown Voltage Variation vs. Temperature**



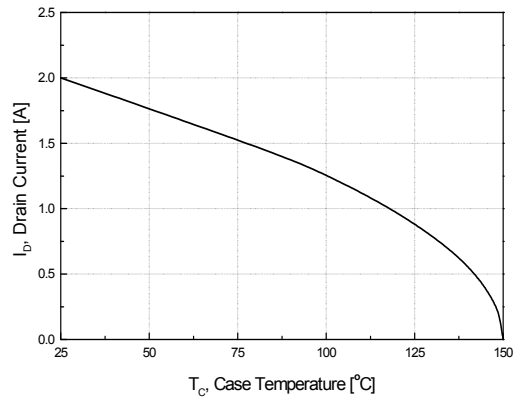
**Figure 8. On-Resistance Variation vs. Temperature**



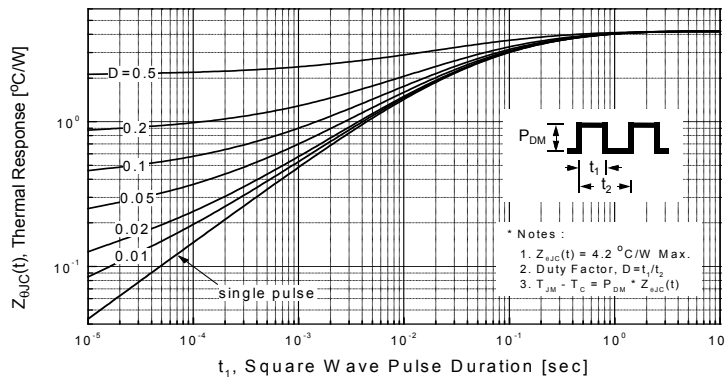
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**



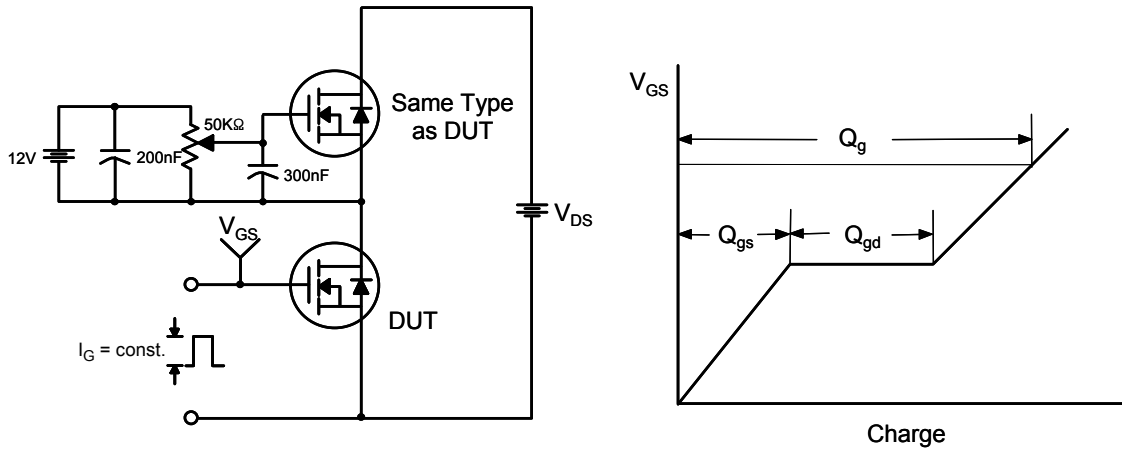


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

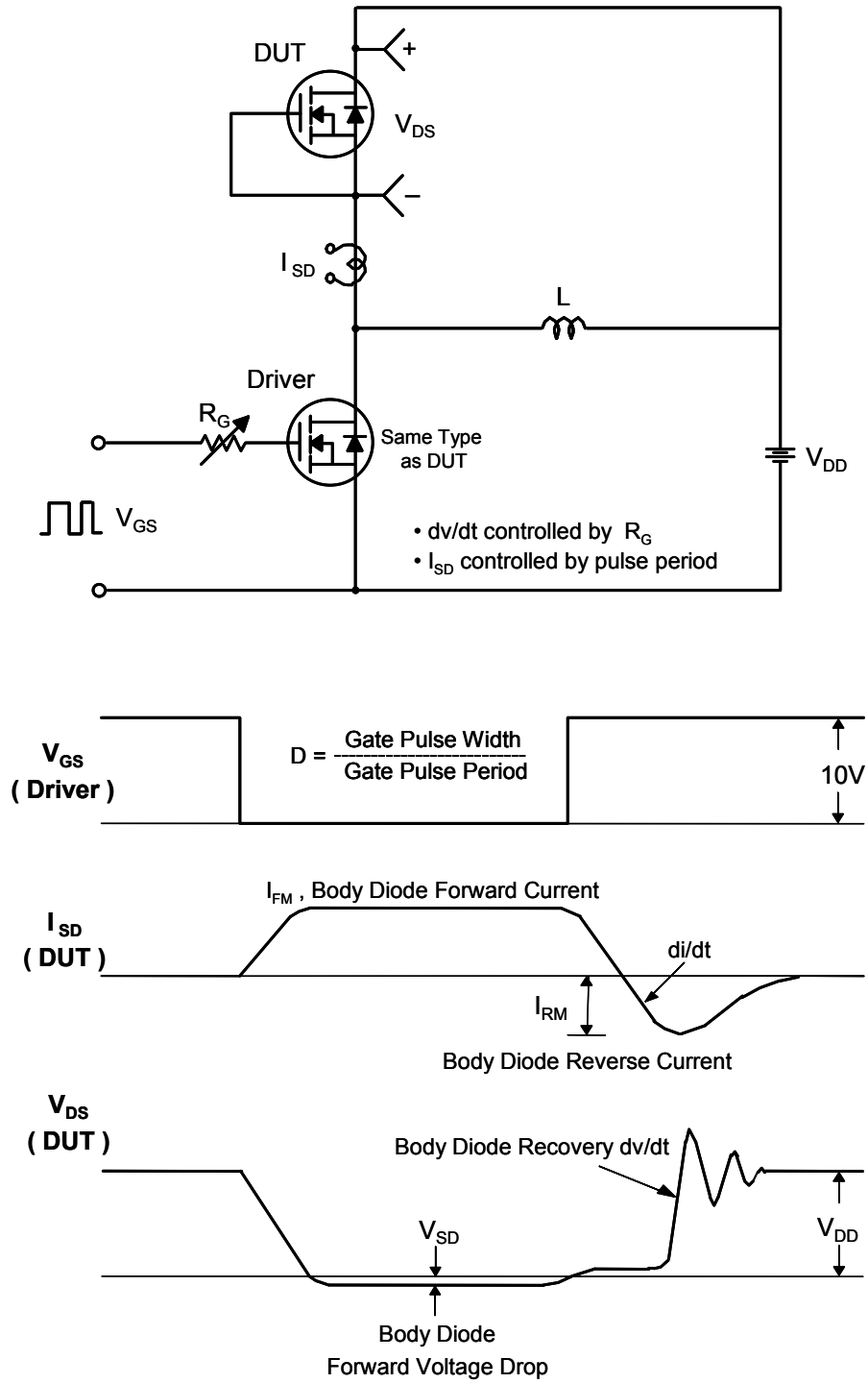
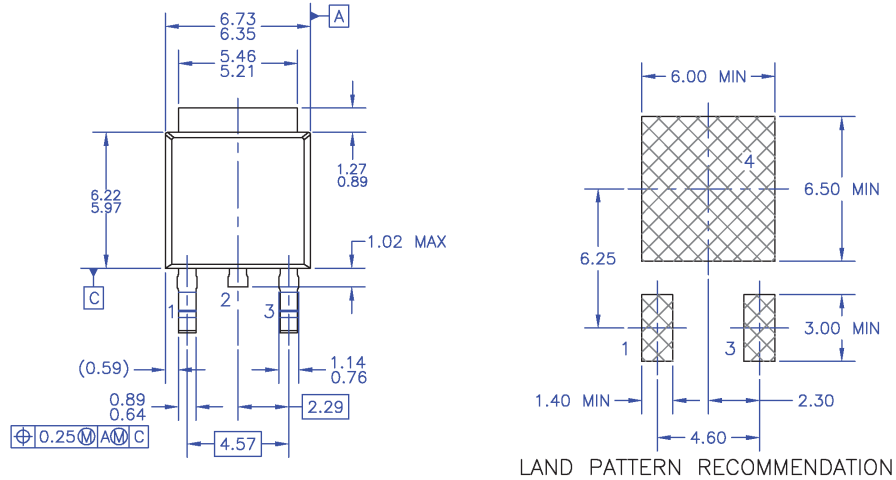


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

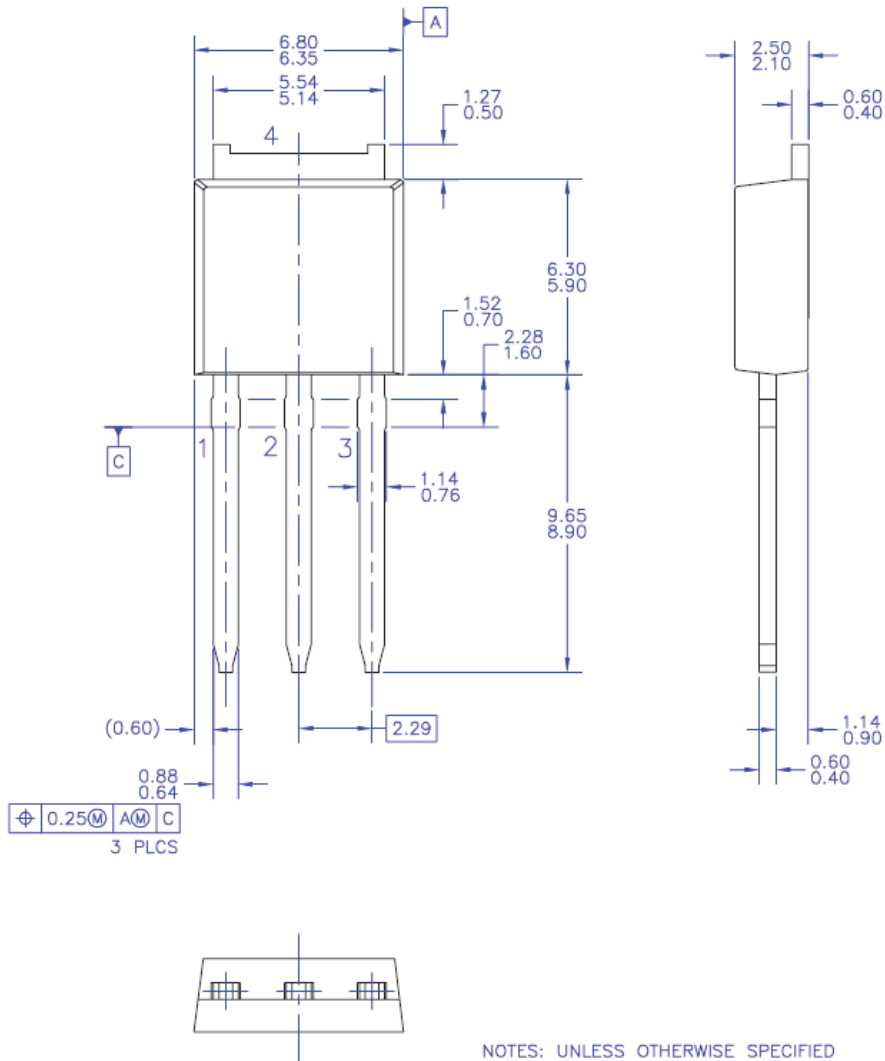
**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

**Figure 17. TO-251 (I-PAK), Molded, 3-Lead, Option AA**

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