

FDD6N50 / FDU6N50

N-Channel UniFET™ MOSFET

500 V, 6 A, 900 mΩ

Features

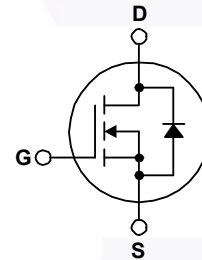
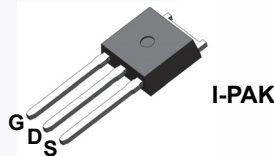
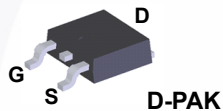
- $R_{DS(on)} = 900\text{ m}\Omega$ (Max.) @ $V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$
- Low Gate Charge (Typ. 12.8 nC)
- Low C_{rss} (Typ. 9 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FDD6N50TM / FDD6N50TM_WS / FDU6N50TU	Unit
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	6 3.8	A A
I_{DM}	Drain Current	- Pulsed (Note 1)	24	A
V_{GSS}	Gate-Source voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	270	mJ
I_{AR}	Avalanche Current	(Note 1)	6	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	8.9	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$) - Derate Above 25°C	89 0.71	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDD6N50TM / FDD6N50TM_WS / FDU6N50TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	83	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD6N50TM	FDD6N50	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FDD6N50TM_WS	FDD6N50S	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FDU6N50TU	FDU6N50	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.5	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$	--	0.76	0.9	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 3\text{ A}$	--	2.5	--	S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	720	940	pF
C_{OSS}	Output Capacitance		--	95	190	pF
C_{RSS}	Reverse Transfer Capacitance		--	9	13.5	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	--	6	20	ns
t_r	Turn-On Rise Time		--	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
t_f	Turn-Off Fall Time		(Note 4)	--	35	80
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}$	--	12.8	16.6	nC
Q_{gs}	Gate-Source Charge		--	3.7	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	5.8	--
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	24	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 6\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 6\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	--	275	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.7	--	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 6\text{ A}, V_{DD} = 50\text{ V}, L = 13.5\text{ mH}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 6\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

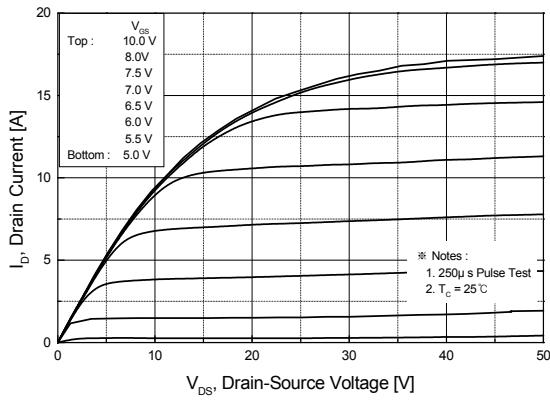


Figure 2. Transfer Characteristics

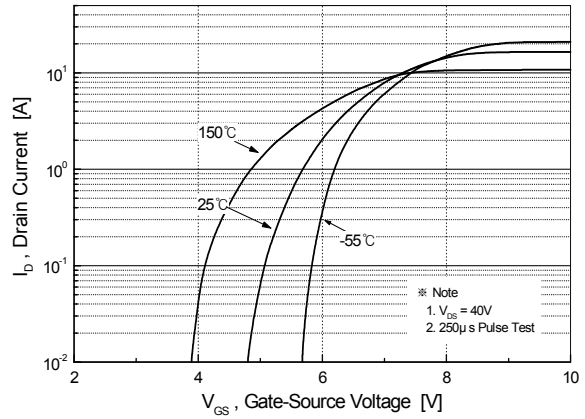


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

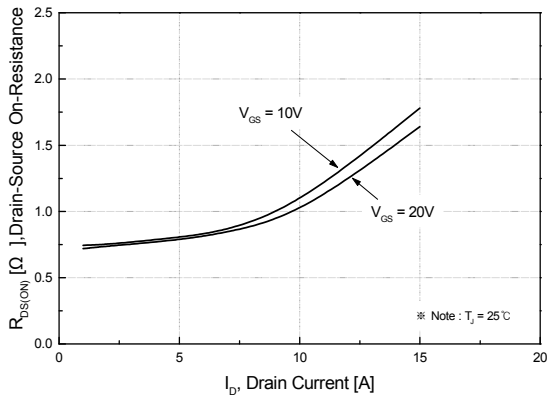


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

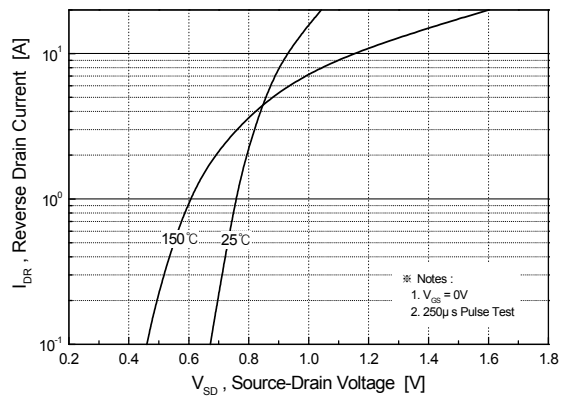


Figure 5. Capacitance Characteristics

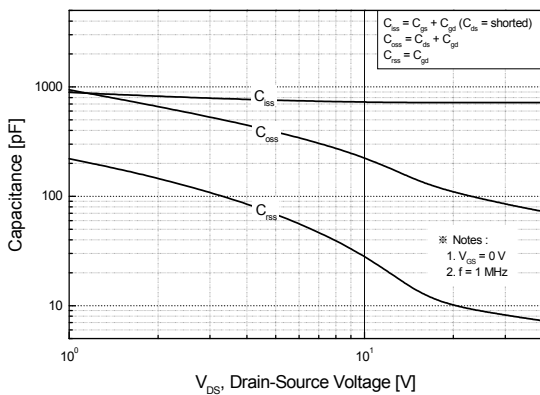
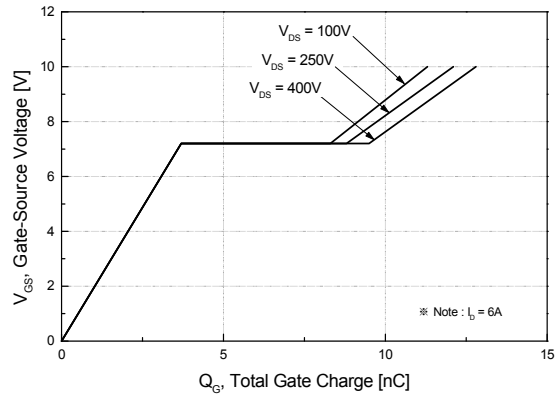


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

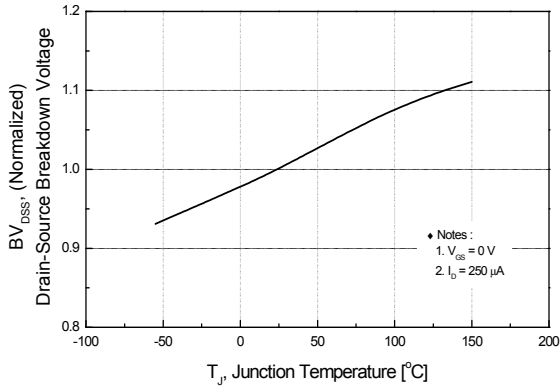


Figure 8. On-Resistance Variation vs. Temperature

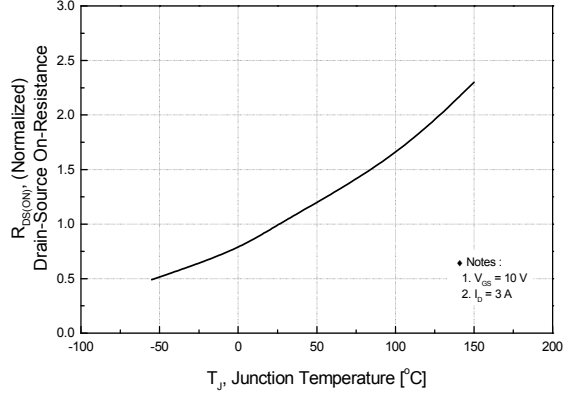


Figure 9. Maximum Safe Operating Area

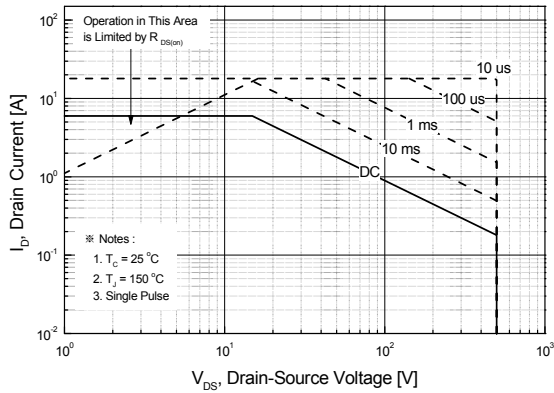


Figure 10. Maximum Drain Current vs. Case Temperature

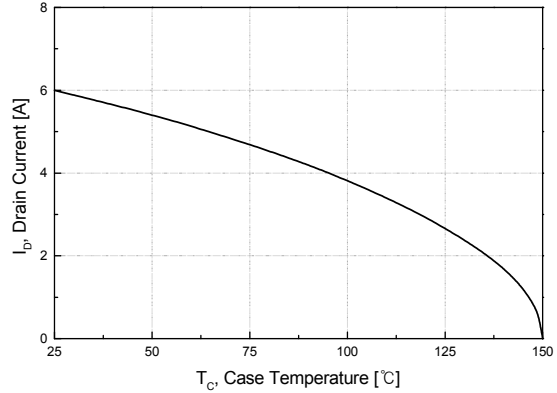
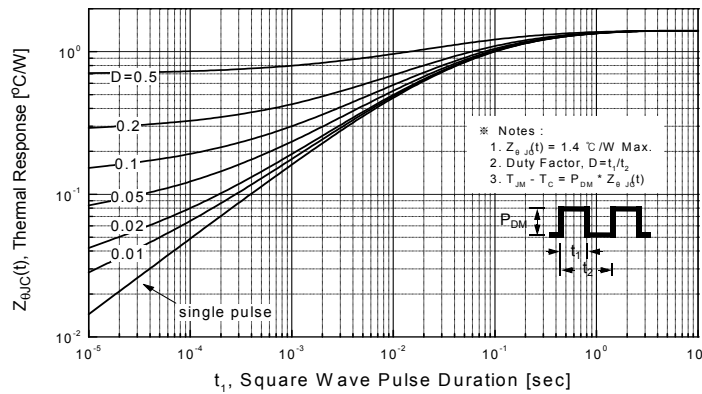


Figure 11. Transient Thermal Response Curve



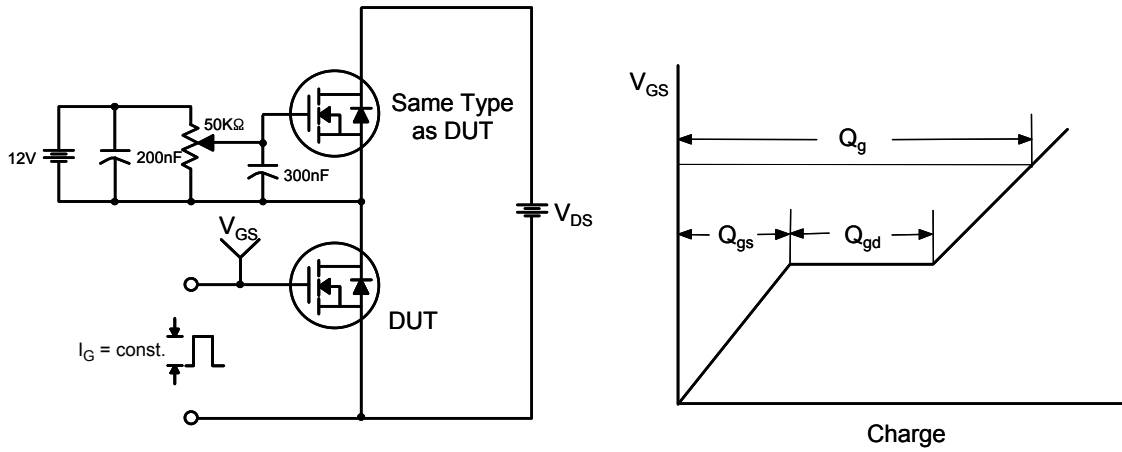


Figure 12. Gate Charge Test Circuit & Waveform

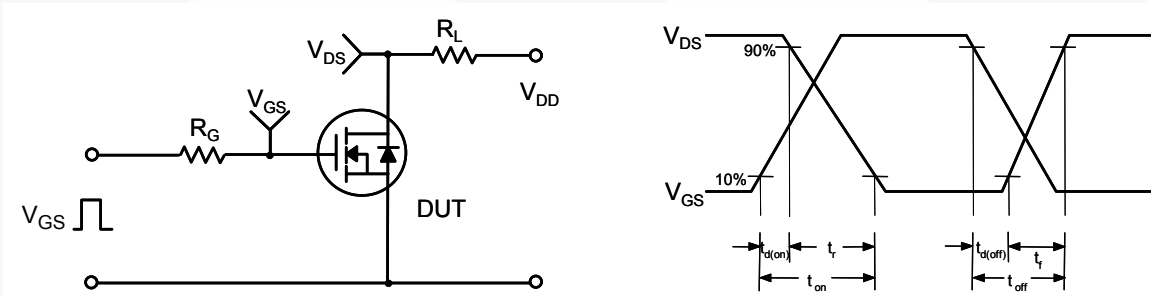


Figure 13. Resistive Switching Test Circuit & Waveforms

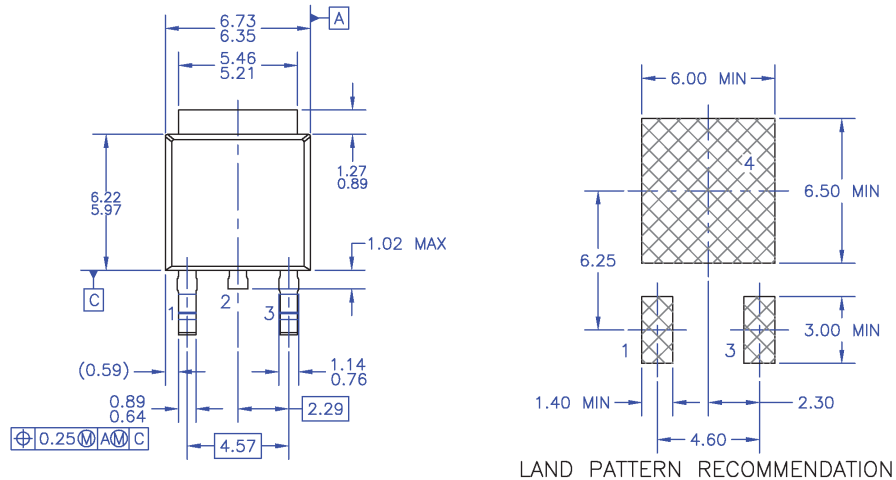


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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Mechanical Dimensions

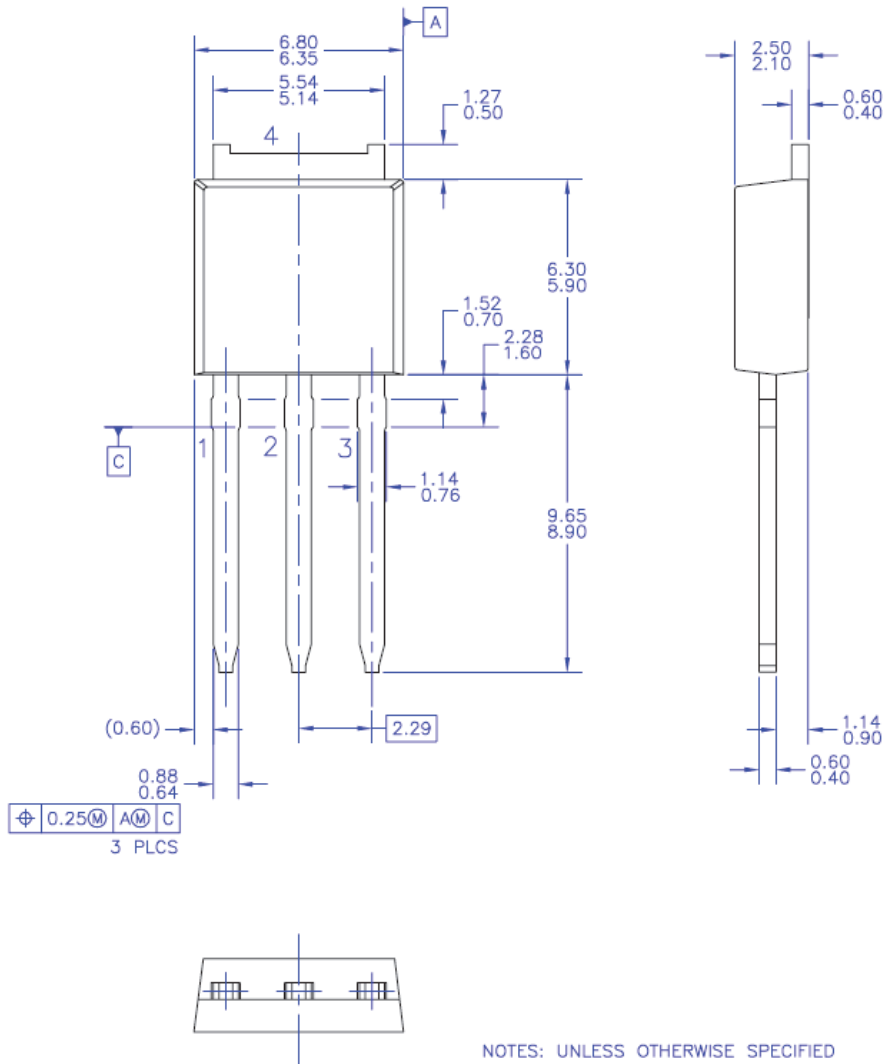


Figure 17. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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