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FAIRCHILD SEMICONDUCTOR®

April 2013

FDZ8040L
Integrated Load Switch

Features

- Optimized for Low-Voltage Core ICs in Portable Systems
- Very Small Package Dimension: WLCSP 0.8 X 0.8 X 0.5 mm^3
- Current = 1.2 A, V_{IN} Max. = 4 V
- Current = 2 A, V_{IN} Max. = 4 V (Pulsed)
- $R_{DS(on)}$ = 80 mΩ at V_{ON} = V_{IN} = 4 V
- $R_{DS(on)}$ = 85 mΩ at V_{ON} = V_{IN} = 3.6 V
- $R_{DS(on)}$ = 90 mΩ at V_{ON} = V_{IN} = 3 V
- $R_{DS(on)}$ = 360 mΩ at V_{ON} = V_{IN} = 0.9 V
- $R_{DS(on)}$ = 1000 mΩ at V_{ON} = V_{IN} = 0.8 V
- RoHS Compliant

Description

This device is particularly suited for compact power management in portable applications needing 0.8 V to 4 V input and 1.2 A output current capability. This load switch integrated a level-shifting function that drives a P-channel power MOSFET in a very small 0.8 X 0.8 X 0.5 mm^3 WLCSP package.

Applications

- Load Switch
- Power Management in Portable Applications

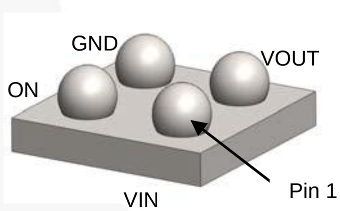


Figure 1. Bottom View

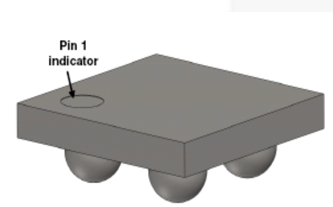


Figure 2. Top View

Ordering Information

Part Number	Device Mark	Ball Pitch	Operating Temperature Range	Switch	Package	Packing Method
FDZ8040L	ZM	0.4 mm	-40 to 85°C	80 mΩ, P-Channel MOSFET	0.8 x 0.8 x 0.5 mm^3 WLCSP	Tape & Reel

Typical Application

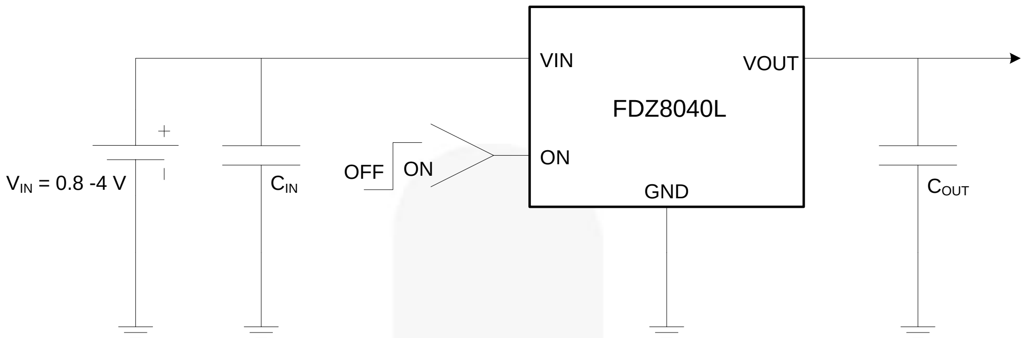


Figure 3. Typical Application

Block Diagram

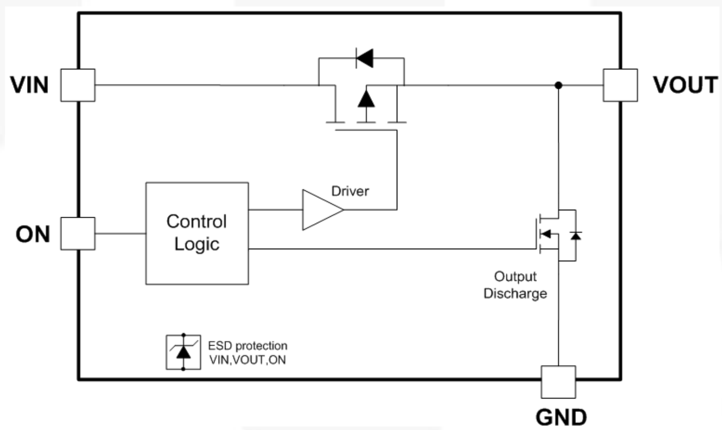


Figure 4. Internal Block Diagram

Pin Configuration

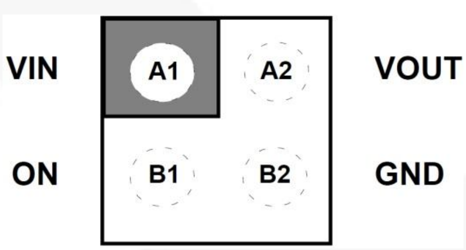


Figure 5. Top View (Bumps Down)

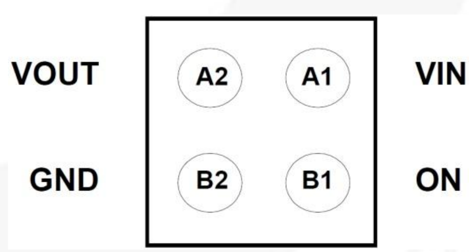


Figure 6. Bottom View (Bumps Up)

Pin Descriptions

Pin #	Name	Description
A1	VIN	Supply Input: Input to the load switch
A2	VOUT	Switch Output: Output of the load switch
B1	ON	ON/OFF Control Input
B2	GND	Ground

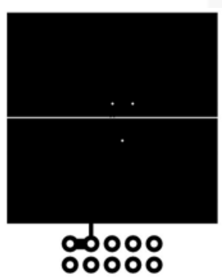
Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

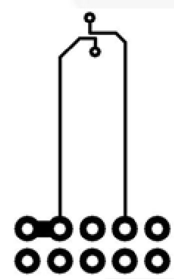
Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on VIN, VOUT, ON to GND		-0.3	4.2	V
I_{OUT_C}	I_{OUT}-Load Current (Continuous)(1a)			1.2	A
I_{OUT_P}	I_{OUT}-Load Current (Pulsed)			2	A
P_D	Power Dissipation at T_A = 25°C(1a)			0.9	W
T_A	Operating Temperature Range		-40	85	°C
T_{STG}	Storage Temperature		-65	150	°C
$R\Theta_{JA}$	Thermal Resistance, Junction to Ambient(1a)			135	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
		Charged Device Model, JESD22-C101	2		

Notes:

1. $R\Theta_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R\Theta_{JC}$ is guaranteed by design, while $R\Theta_{JA}$ is determined by the board design.



a. 135°C/W when mounted on a 1-inch square pad of 2-oz copper.



b. 360°C/W when mounted on a minimum pad of 2-oz copper.

2. Pulse test: pulse width < 300 µs; duty cycle < 2.0%.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on VIN Pin		0.8	4.0	V
V_{ON}	Voltage on ON Pin		0.7	4.0	V
T_A	Operating Temperature Range	1 V to 4 V	-40	85	°C
		0.8 V to 4 V	-10		

Electrical Characteristics

T_J = 25°C and V_{IN}=1.8 V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage		0.8		4.0	V
V_{IL}	ON Input Logic Low Voltage	1.6 V ≤ V_{IN} ≤ 4.0 V			0.35	V
		0.8 V ≤ V_{IN} ≤ 1.6 V			0.25	
V_{IH}	ON Input Logic High Voltage	1.6 V ≤ V_{IN} ≤ 4.0 V	1.0			V
		0.8 V ≤ V_{IN} ≤ 1.6 V	0.7			
I_Q	Quiescent Current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = 1.8 V			2.1	µA
$I_{Q(off)}$	Off Supply Current	I_{OUT} = 0 mA, V_{IN} = 1.8 V, V_{ON} = GND			1	µA
$I_{SD(off)}$	Off Switch Current	V_{ON} = GND, V_{OUT} = 0 V, V_{IN} = 1.8 V			100	nA
I_{ON}	ON Input Leakage	V_{ON} = V_{IN} or GND			1	µA
R_{PD}	Output Discharge Pull-Down Resistance			200		Ω
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{ON} = V_{IN} = 4 V, I_{OUT} = 300 mA		50	80	mΩ
		V_{ON} = V_{IN} = 3.6 V, I_{OUT} = 300 mA		51	85	
		V_{ON} = V_{IN} = 3 V, I_{OUT} = 300 mA		54	90	
		V_{ON} = 0.7 V, V_{IN} = 1.6 V, I_{OUT} = 300 mA		73	110	
		V_{ON} = 0.7 V, V_{IN} = 1 V, I_{OUT} = 300 mA		140	309	
		V_{ON} = V_{IN} = 0.9 V, I_{OUT} = 10 mA		186	360	
		V_{ON} = V_{IN} = 0.8 V, I_{OUT} = 10 mA		348	1000	
		V_{ON} = V_{IN} = 0.9 V, I_{OUT} = 10 mA, T_J = 10 ~ 85°C		194	370	
		V_{ON} = V_{IN} = 0.8 V, I_{OUT} = 10 mA, T_J = 10 ~ 85°C		268	750	
		V_{IN} = 3.6 V, I_{OUT} = 300 mA, T_J = 85°C		59	102	

Switching Characteristics

Symbol	Parameter	Test Conditions	Typical	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 1.6 V, V_{ON} = 0.7 V, C_L = 1 μF, R_L = 500 Ω	22	μs
t_r	Turn-On Rise Time		23	μs
$t_{d(off)}$	Turn-Off Delay Time		109	μs
t_f	Turn-Off Fall Time		285	μs
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 1 V, V_{ON} = 1.8 V, C_L = 1 μF, R_L = 500 Ω	37	μs
t_r	Turn-On Rise Time		35	μs
$t_{d(off)}$	Turn-Off Delay Time		112	μs
t_f	Turn-Off Fall Time		332	μs
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 1.8 V, V_{ON} = 1.8 V, C_L = 1 μF, R_L = 500 Ω	20	μs
t_r	Turn-On Rise Time		22	μs
$t_{d(off)}$	Turn-Off Delay Time		122	μs
t_f	Turn-Off Fall Time		296	μs
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 2.5 V, V_{ON} = 1.8 V, C_L = 1 μF, R_L = 500 Ω	15	μs
t_r	Turn-On Rise Time		19	μs
$t_{d(off)}$	Turn-Off Delay Time		160	μs
t_f	Turn-Off Fall Time		295	μs
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 3.3 V, V_{ON} = 1.8 V, C_L = 1 μF, R_L = 500 Ω	13	μs
t_r	Turn-On Rise Time		18	μs
$t_{d(off)}$	Turn-Off Delay Time		193	μs
t_f	Turn-Off Fall Time		305	μs
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 0.8 V, V_{ON} = 0.8 V, C_L = 1 μF, R_L = 500 Ω	53	μs
t_r	Turn-On Rise Time		56	μs
$t_{d(off)}$	Turn-Off Delay Time		143	μs
t_f	Turn-Off Fall Time		532	μs
$t_{d(on)}$	Turn-On Delay Time	V_{IN} = 0.9 V, V_{ON} = 0.9 V, C_L = 1 μF, R_L = 500 Ω	51	μs
t_r	Turn-On Rise Time		54	μs
$t_{d(off)}$	Turn-Off Delay Time		148	μs
t_f	Turn-Off Fall Time		525	μs

Typical Performance Characteristics

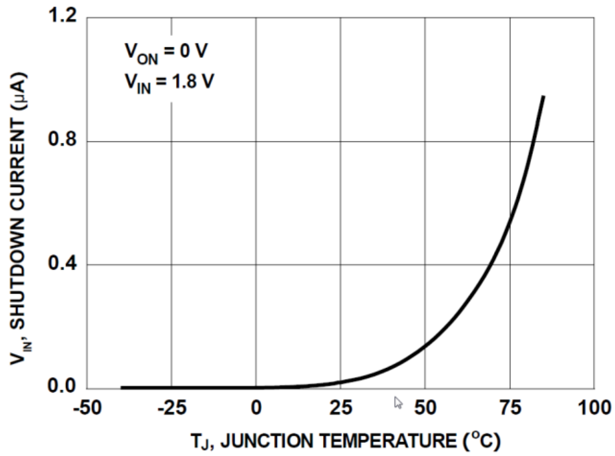


Figure 7. Shutdown Current vs. Temperature

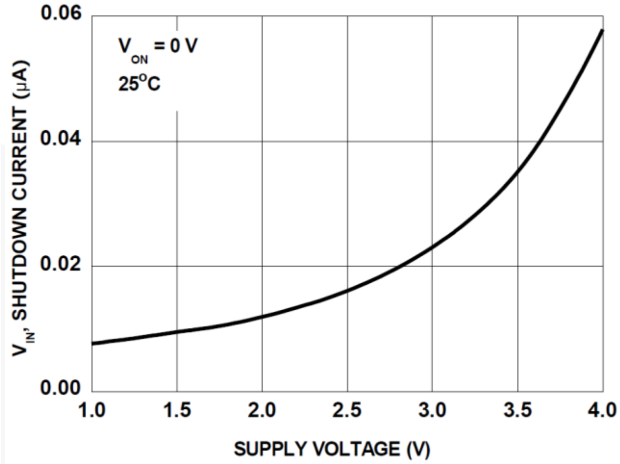


Figure 8. Shutdown Current vs. Supply Voltage

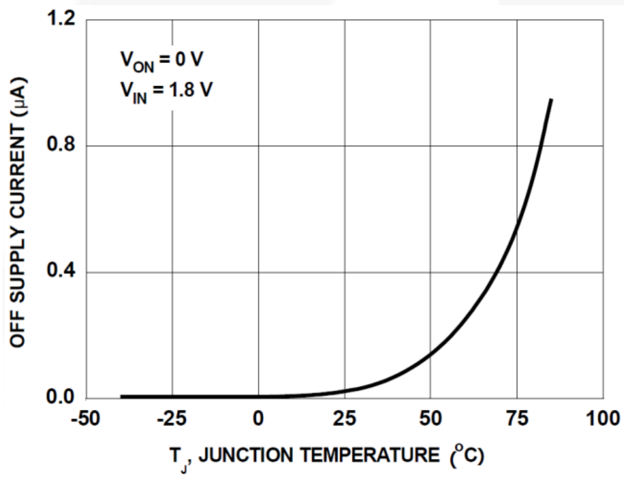


Figure 9. Off Supply Current vs. Temperature

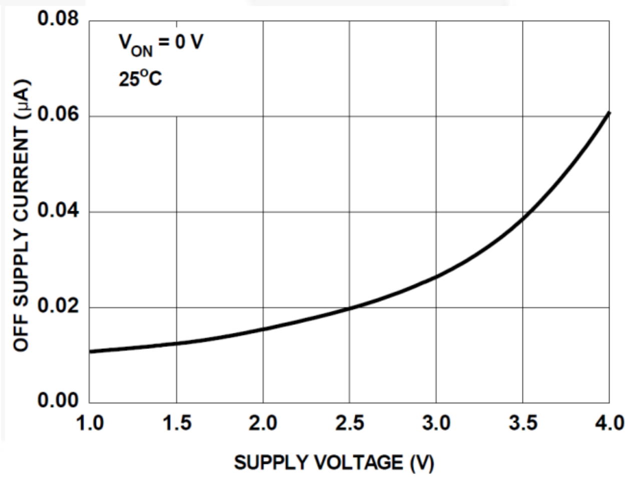


Figure 10. Off Supply Current vs. Supply Voltage

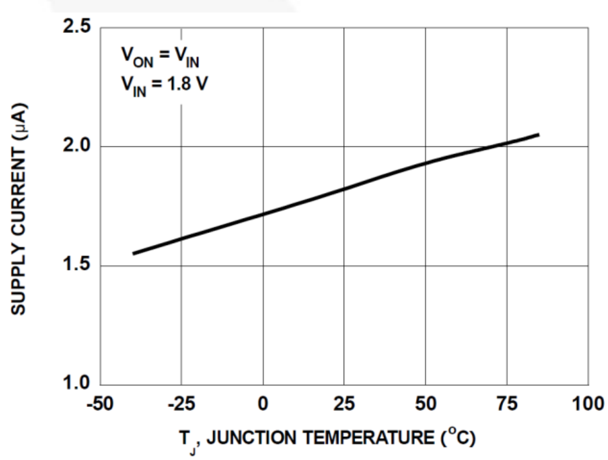


Figure 11. Quiescent Current vs. Temperature

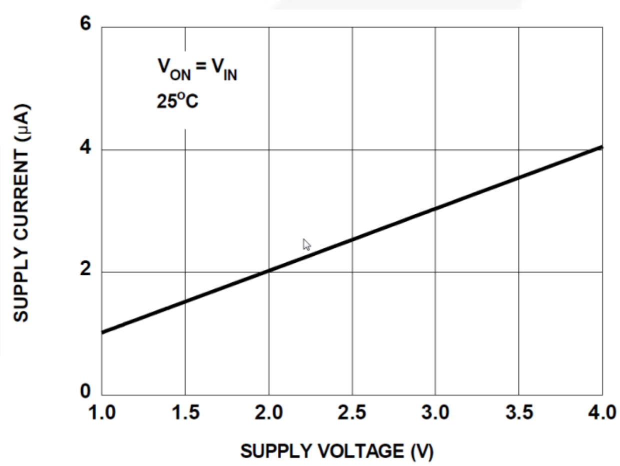


Figure 12. Quiescent Current vs. Supply Voltage

Typical Performance Characteristics

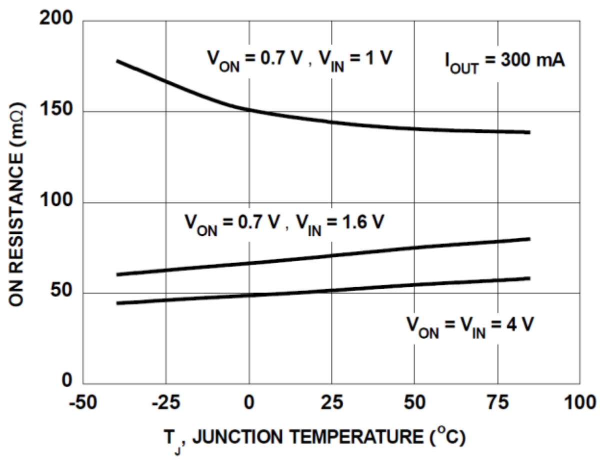


Figure 13. R_{ON} vs. Temperature

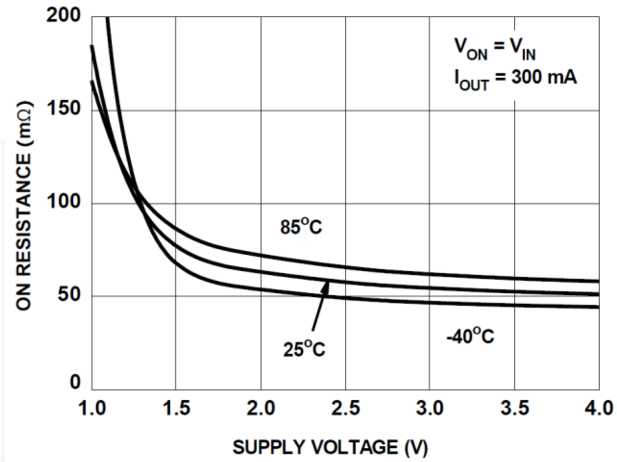


Figure 14. R_{ON} vs. Supply Voltage

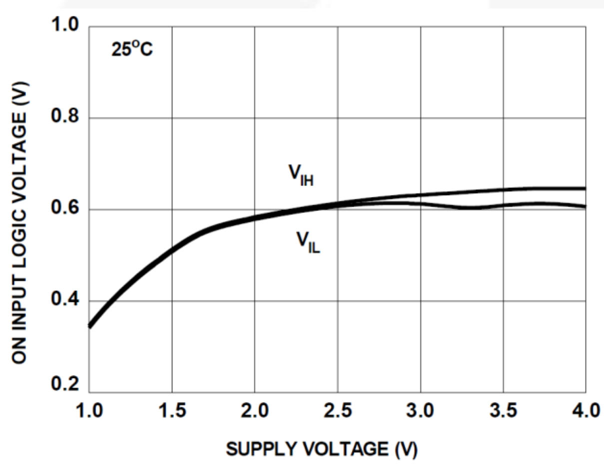


Figure 15. ON-Pin Threshold vs. V_{IN}

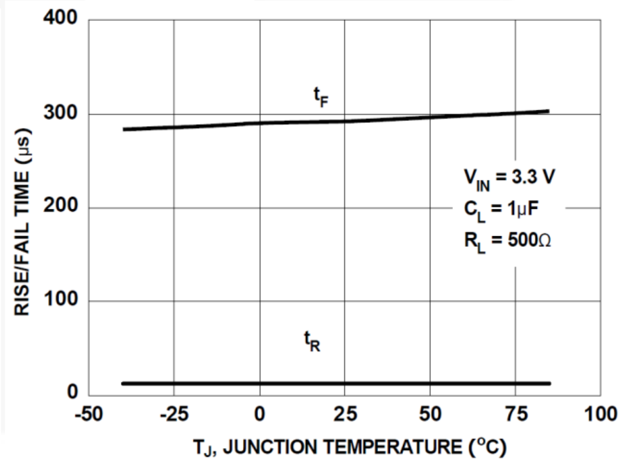


Figure 16. V_{OUT} Rise and Fall Time vs. Temperature at R_L=500Ω

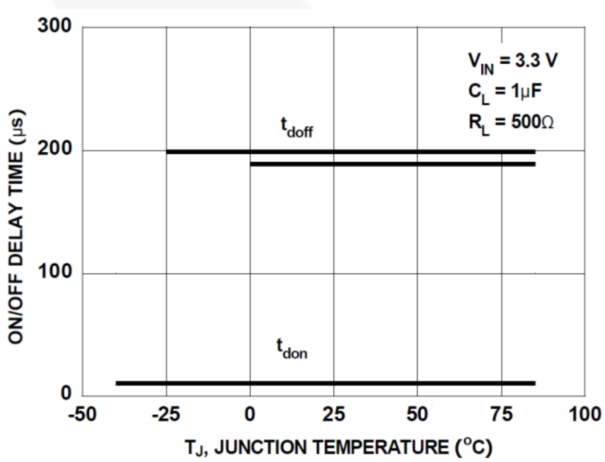


Figure 17. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at R_L=500Ω

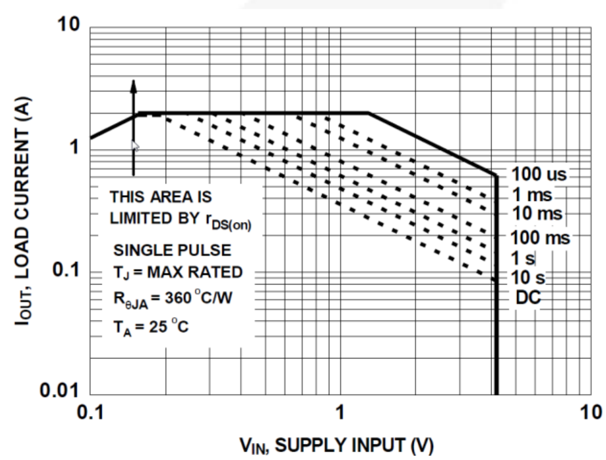


Figure 18. Forward Bias Safe Operation Area

Typical Performance Characteristics

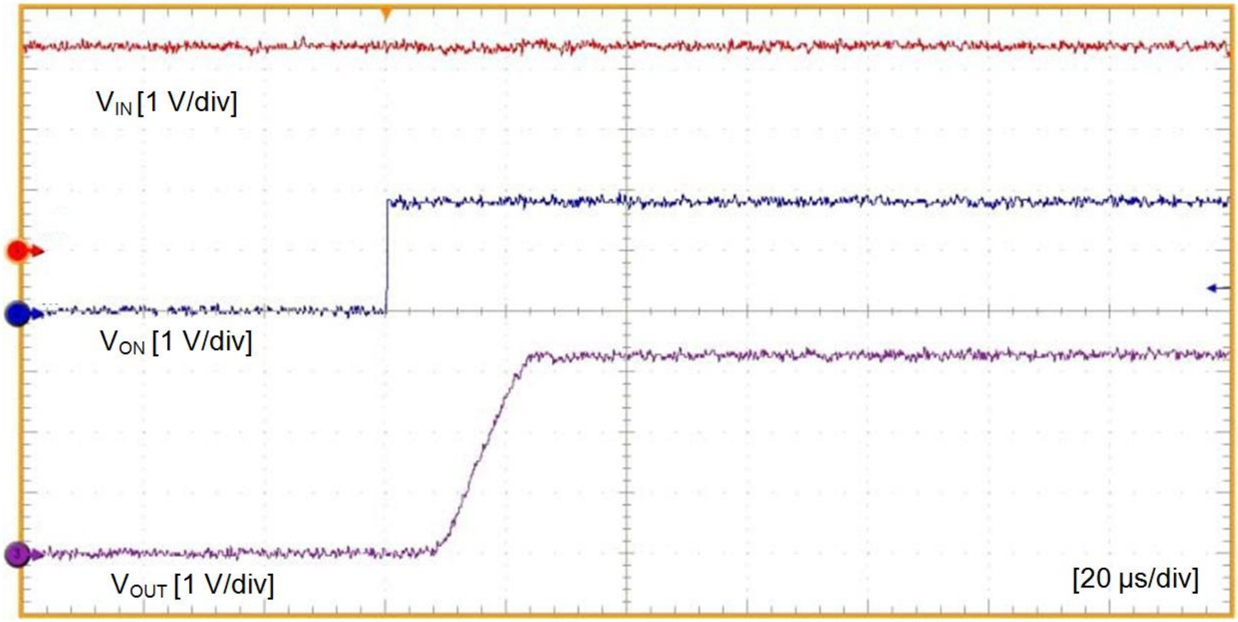


Figure 19. Turn-On Response (V_{IN} = 3.3 V, C_{OUT}=1 µF, R_L=500 Ω)

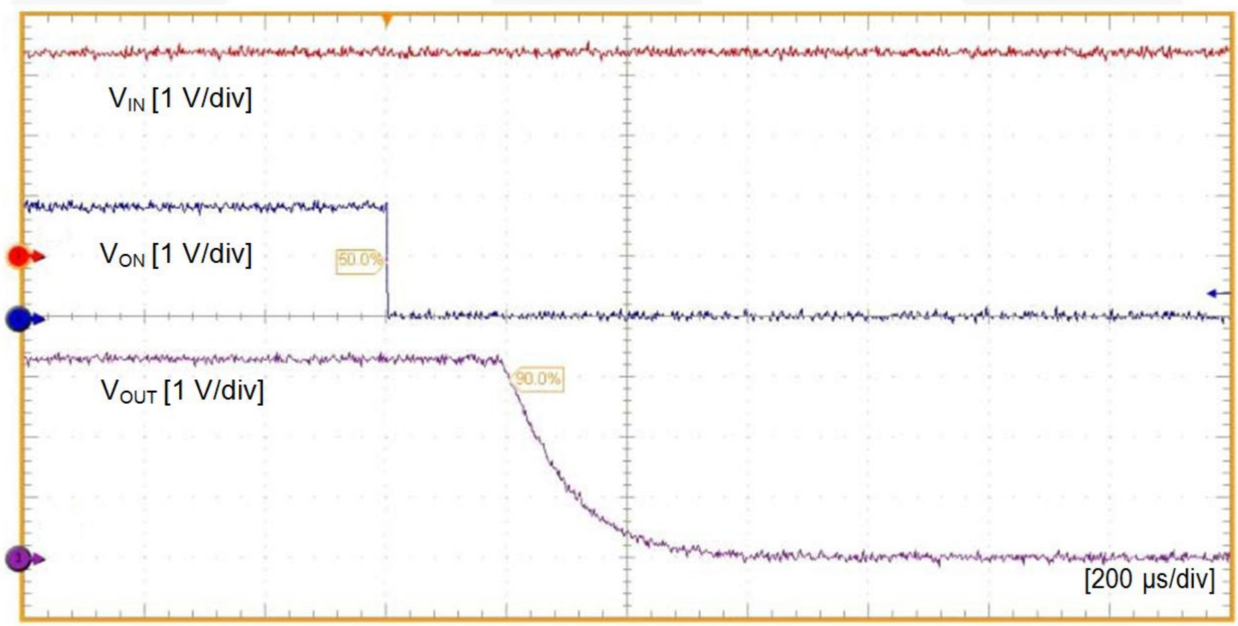


Figure 20. Turn-Off Response (V_{IN} = 3.3 V, C_{OUT}=1 µF, R_L=500 Ω)

Functional Description

The FDZ8040L is a low-$R_{DS(ON)}$ P-channel load switch packaged in space-saving 0.8 x 0.8 WLCSP.

The core of the device is an 80 mΩ P-channel MOSFET capable of functioning over a wide input operating range of 0.8-4 V. The ON pin, an active HIGH TTL-compatible input that supports input as low as 0.7 V, controls the state of the switch.

Applications Information

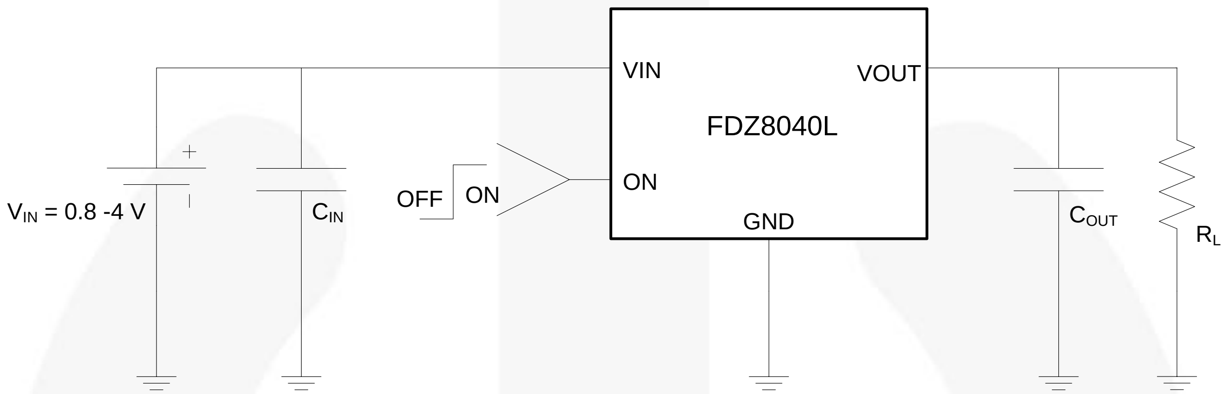


Figure 21. Typical Application

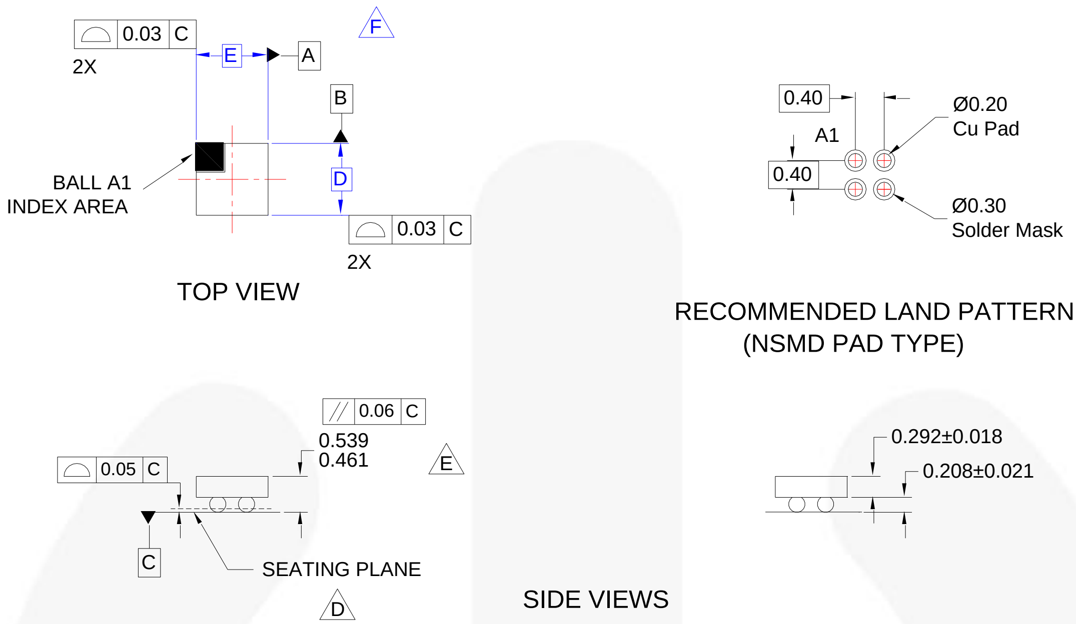
Input Capacitor

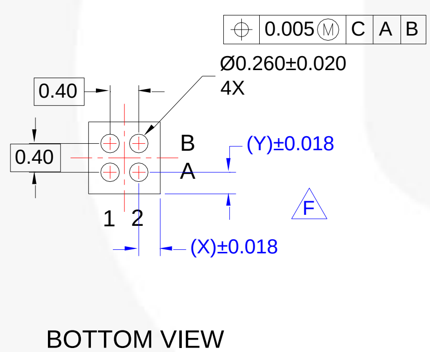
To reduce device inrush current effect, a 0.1 µF ceramic capacitor, C_{IN}, is recommended close to the VIN pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

FDZ8040L works without an output capacitor. However, if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1 µF capacitor, C_{OUT}, should be placed between the VOUT and GND pins.

Physical Dimensions





NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004AFrev1.

Figure 22. 4-Ball, WLCSP, 2 X 2 Array, 0.4 mm Pitch, 250 µm Ball

Product-Specific Dimensions

Product	D	E	X	Y
FDZ8040L	0.8 ±0.03 mm	0.8 ±0.03 mm	0.21 mm	0.21 mm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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