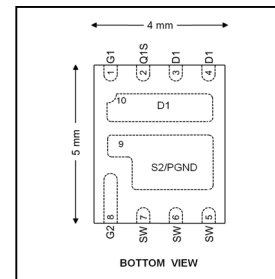
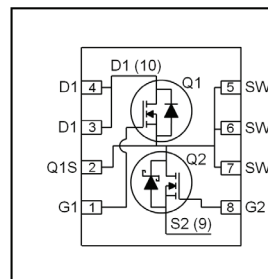


HEXFET® Power MOSFET

	Q1	Q2	
$V_{DSS}$	25	25	V
$R_{DS(on) \max}$ (@ $V_{GS} = 4.5V$ )	4.70	1.80	mΩ
$Qg$ (typical)	9.7	23	nC
$I_D$ (@ $T_C = 25^\circ C$ )	25 <sup>⑦</sup>	25 <sup>⑦</sup>	A



**Applications**

- Control and Synchronous MOSFETs for synchronous buck converters

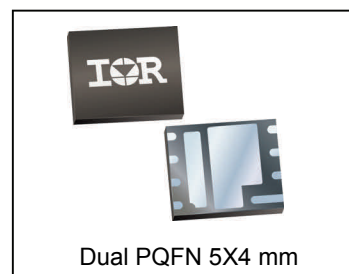
**Features**

Control and synchronous MOSFETs in one package
Low charge control MOSFET (9.7nC typical)
Low $R_{DS(on)}$ synchronous MOSFET (<1.8mΩ)
Intrinsic Schottky Diode with Low Forward Voltage on Q2
RoHS Compliant, Halogen-Free
MSL1, Industrial Qualification

results in  
⇒

**Benefits**

Increased power density
Lower switching losses
Lower conduction losses
Lower Switching Losses
Environmentally friendlier
Increased reliability



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH4257DPbF	Dual PQFN 5mm x 4mm	Tape and Reel	4000	IRFH4257DTRPbF

**Absolute Maximum Ratings**

	Parameter	Q1 Max.	Q2 Max.	Units
$V_{GS}$	Gate-to-Source Voltage	± 20		V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	68 <sup>⑥⑦</sup>	111 <sup>⑥⑦</sup>	A
$I_D @ T_C = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	54 <sup>⑥⑦</sup>	88 <sup>⑥⑦</sup>	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ (Source Bonding Technology Limited)	25 <sup>⑦</sup>	25 <sup>⑦</sup>	
$I_{DM}$	Pulsed Drain Current	120 <sup>⑧</sup>	375 <sup>⑧</sup>	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	25	28	
$P_D @ T_C = 70^\circ C$	Power Dissipation	16	18	W/°C
	Linear Derating Factor	0.20	0.22	
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150		°C

**Thermal Resistance**

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case <sup>④</sup>	5.0	4.5	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case <sup>④</sup>	33	26	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑤</sup>	45	40	
$R_{\theta JA} (<10s)$	Junction-to-Ambient <sup>⑤</sup>	30	27	

Notes ① through ⑧ are on page 12

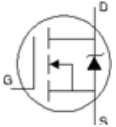
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

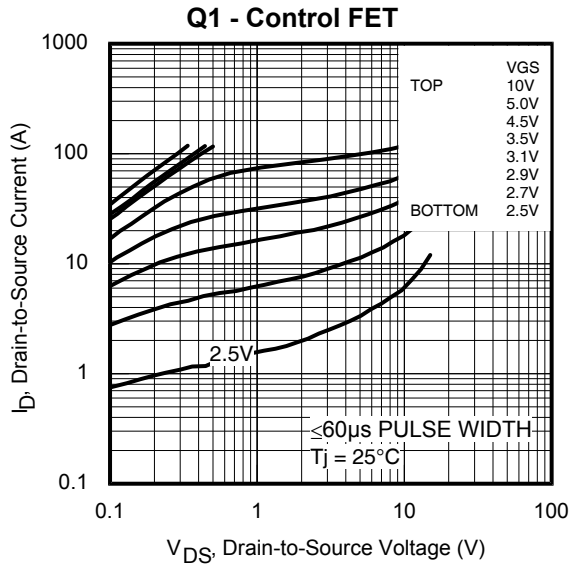
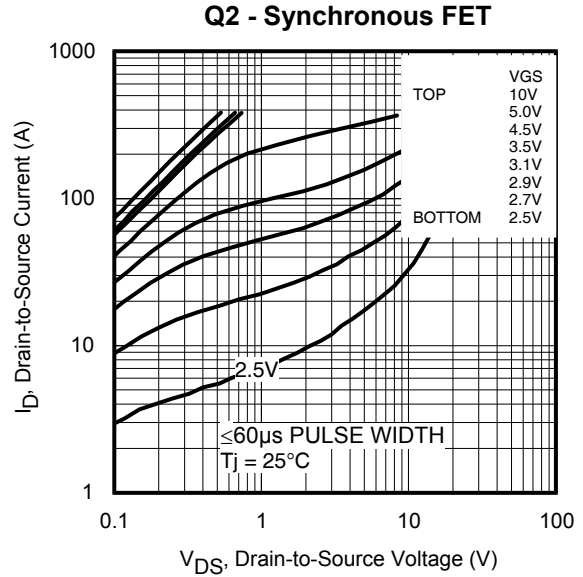
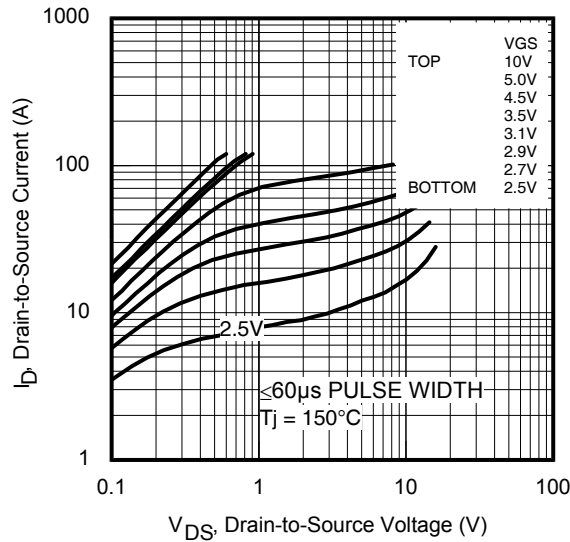
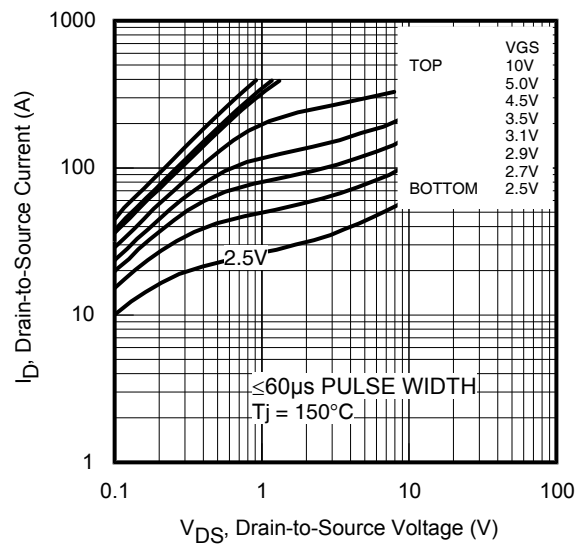
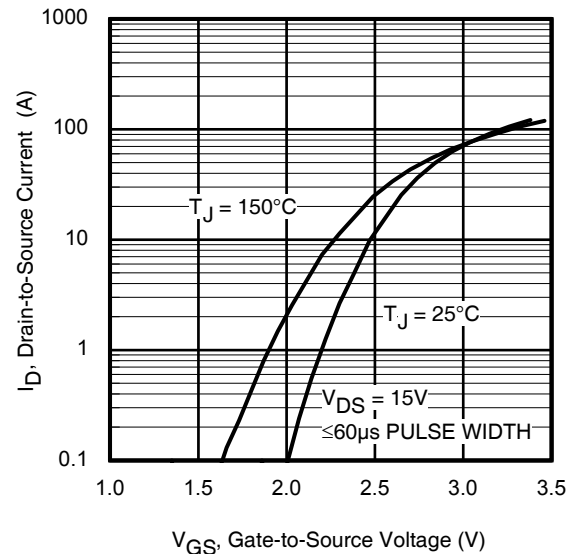
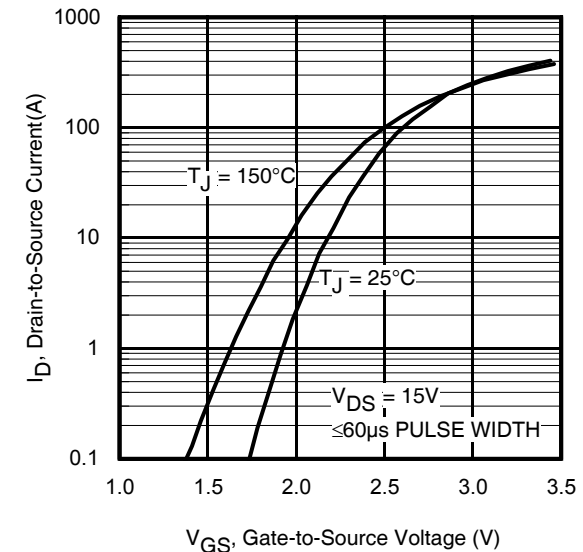
	Parameter		Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	Q1	25	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
		Q2	25	—	—		V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	Q1	—	22	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
		Q2	—	22	—		Reference to 25°C, I <sub>D</sub> = 10mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	Q1	—	2.7	3.4	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A ③
		Q2	—	1.1	1.4		V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A ③
		Q1	—	3.7	4.7		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 25A ③
		Q2	—	1.4	1.8		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 25A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	Q1	1.1	1.6	2.1	V	Q1: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 35μA
		Q2	1.1	1.6	2.1		Q2: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	Q1	—	-5.4	—	mV/°C	Q1: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 35μA
		Q2	—	-5.3	—		Q2: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1mA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	Q1	—	—	1.0	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
		Q2	—	—	250		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	Q1	—	—	100	nA	V <sub>GS</sub> = 20V
		Q2	—	—	100		V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	Q1	—	—	-100		V <sub>GS</sub> = -20V
		Q2	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	Q1	100	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 25A
		Q2	138	—	—		V <sub>DS</sub> = 10V, I <sub>D</sub> = 25A
Q <sub>g</sub>	Total Gate Charge	Q1	—	9.7	15	nC	Q1 V <sub>DS</sub> = 13V V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 25A  Q2 V <sub>DS</sub> = 13V V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 25A
		Q2	—	23	35		
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	Q1	—	2.4	—		
		Q2	—	5.1	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	Q1	—	1.2	—		
		Q2	—	2.6	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	Q1	—	3.4	—		
		Q2	—	7.6	—		
Q <sub>godr</sub>	Gate Charge Overdrive	Q1	—	2.7	—		
		Q2	—	7.7	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	Q1	—	4.6	—		
		Q2	—	10.2	—		
Q <sub>oss</sub>	Output Charge	Q1	—	10	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
		Q2	—	25	—		
R <sub>G</sub>	Gate Resistance	Q1	—	1.4	—	Ω	
		Q2	—	0.7	—		
t <sub>d(on)</sub>	Turn-On Delay Time	Q1	—	8.2	—	ns	Q1 V <sub>DS</sub> = 13V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 25A, R <sub>g</sub> = 1.8Ω  Q2 V <sub>DS</sub> = 13V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 25A, R <sub>g</sub> = 1.8Ω
		Q2	—	12	—		
t <sub>r</sub>	Rise Time	Q1	—	47	—		
		Q2	—	51	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	Q1	—	12	—		
		Q2	—	20	—		
t <sub>f</sub>	Fall Time	Q1	—	20	—		
		Q2	—	25	—		
C <sub>iss</sub>	Input Capacitance	Q1	—	1321	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 13V f = 1.0MHz
		Q2	—	3161	—		
C <sub>oss</sub>	Output Capacitance	Q1	—	365	—		
		Q2	—	965	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	Q1	—	101	—		
		Q2	—	237	—		

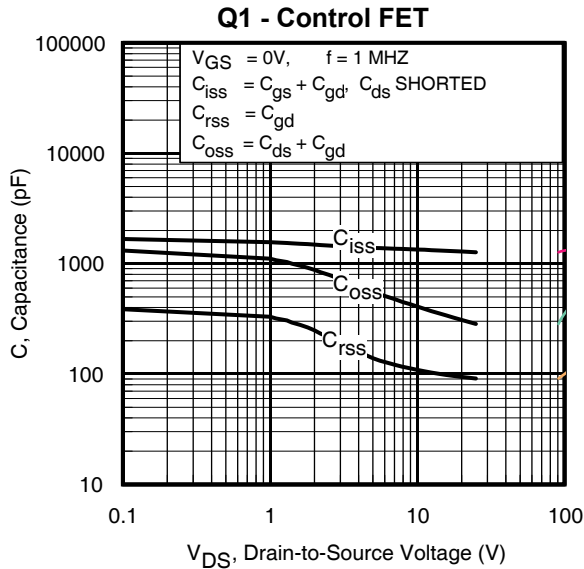
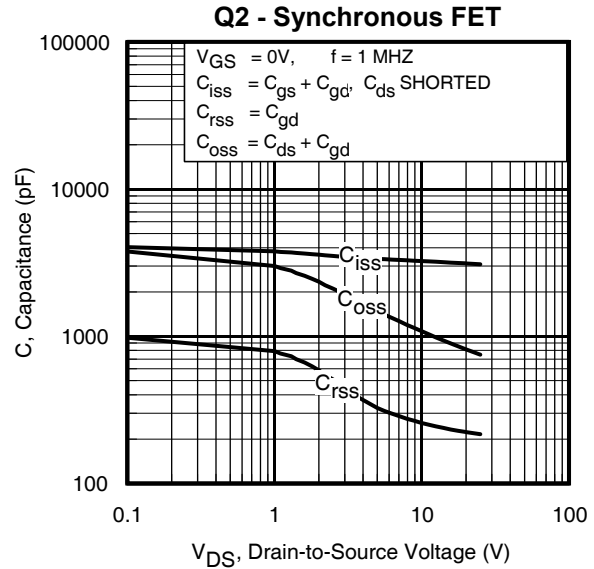
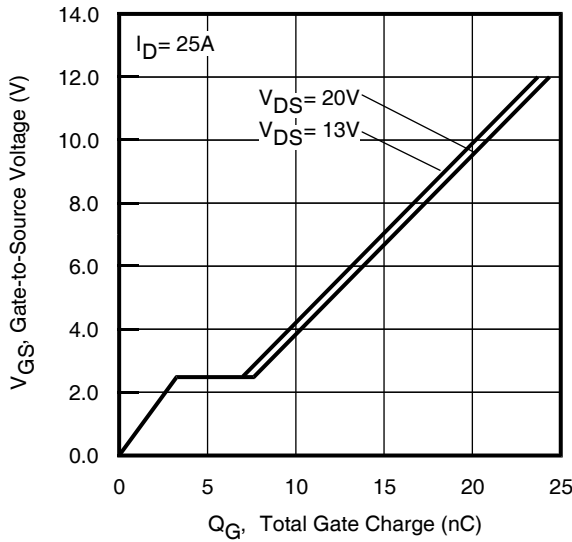
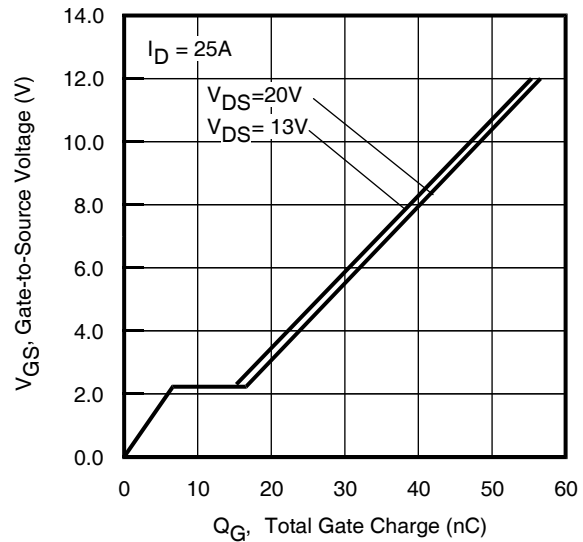
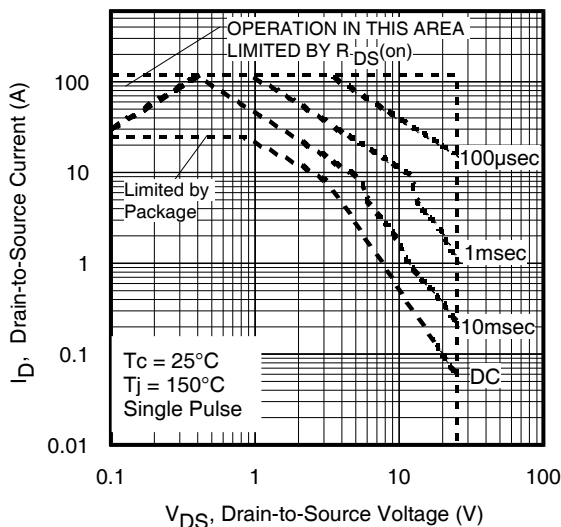
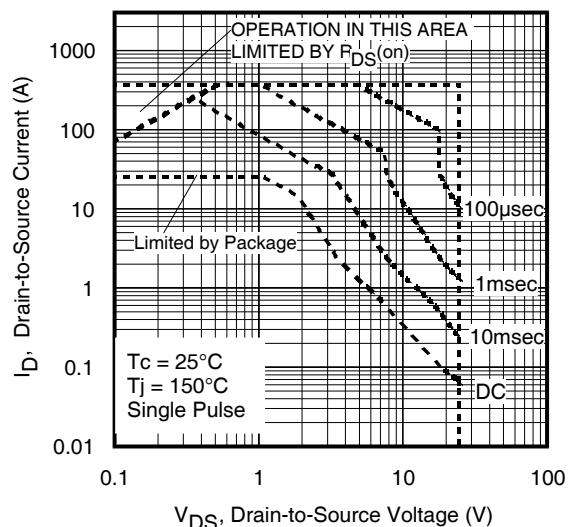
**Avalanche Characteristics**

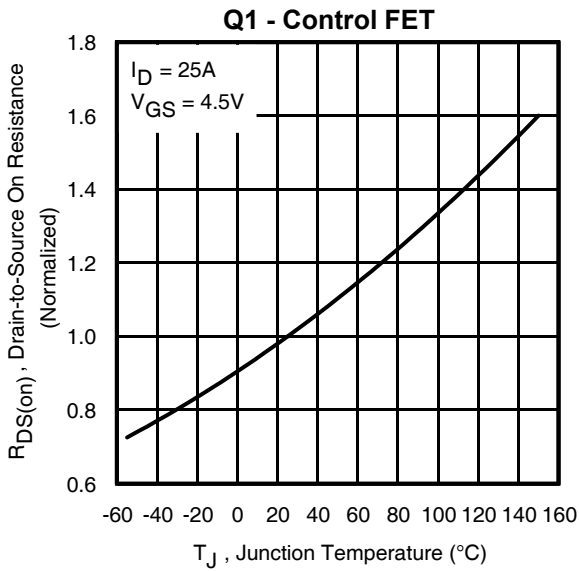
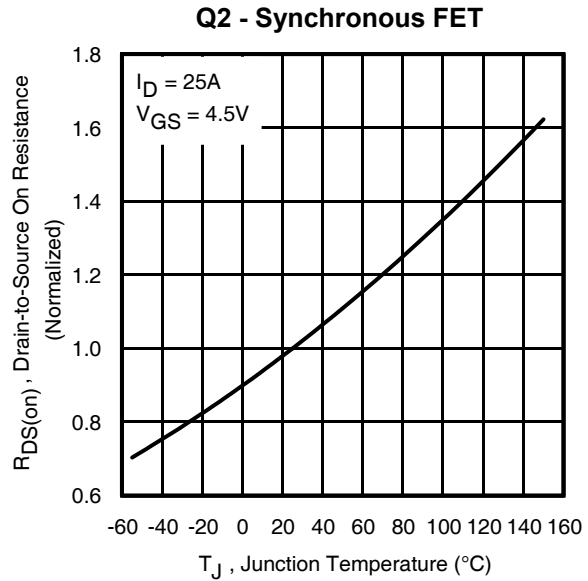
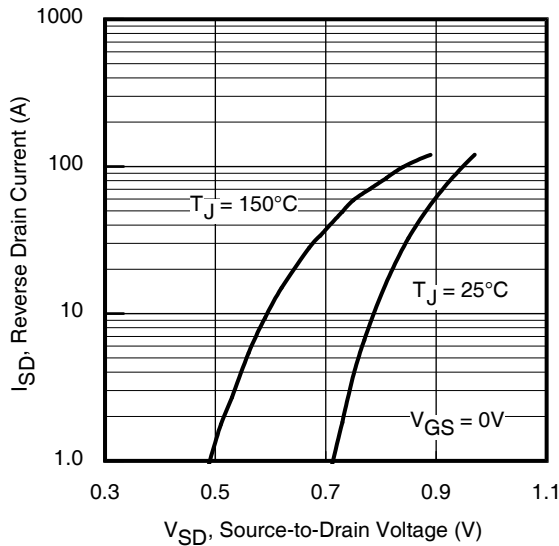
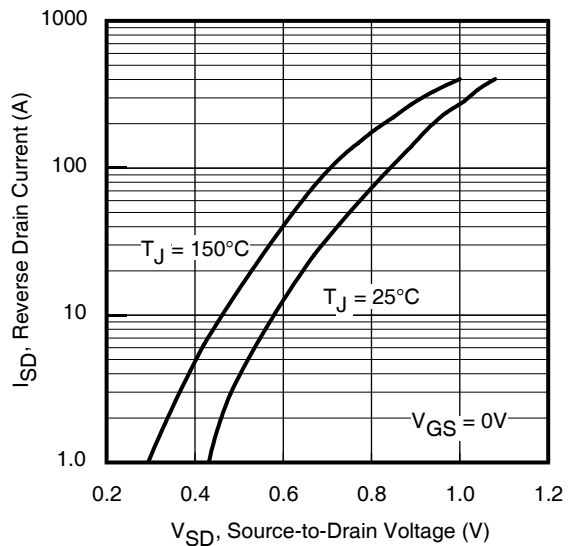
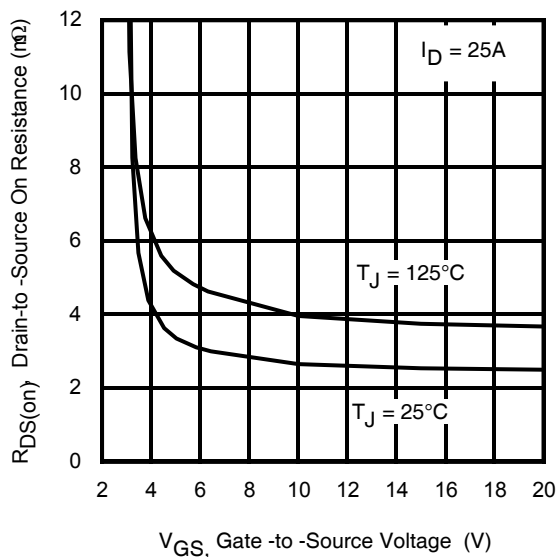
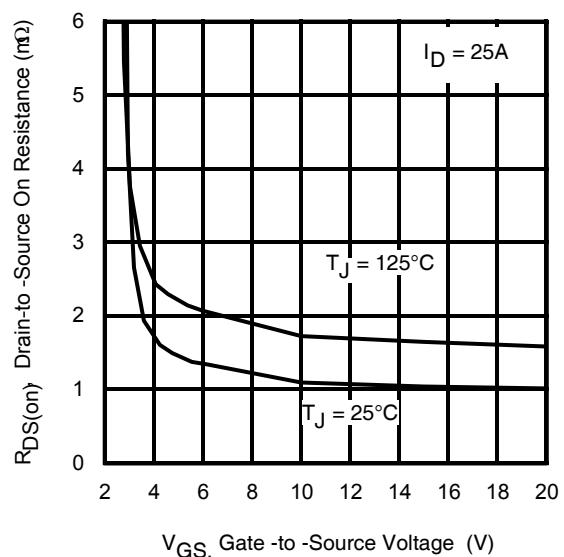
	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	42	387	mJ

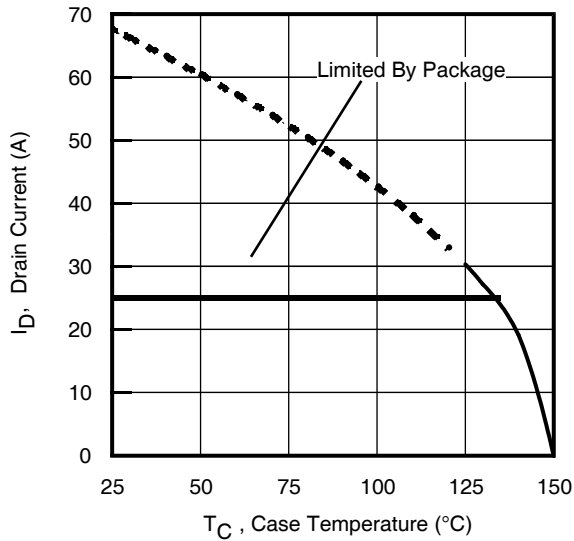
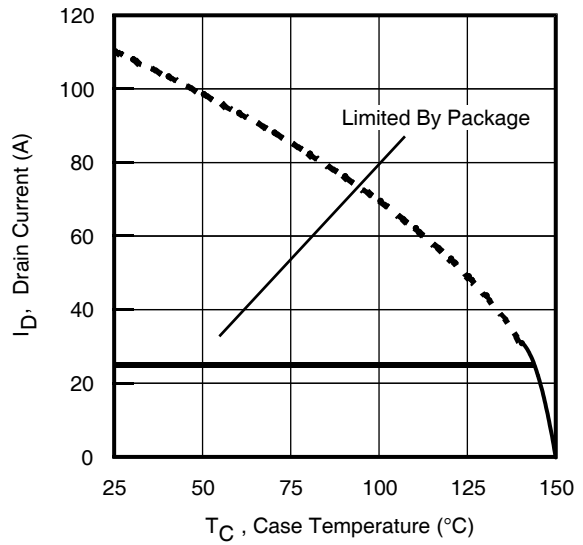
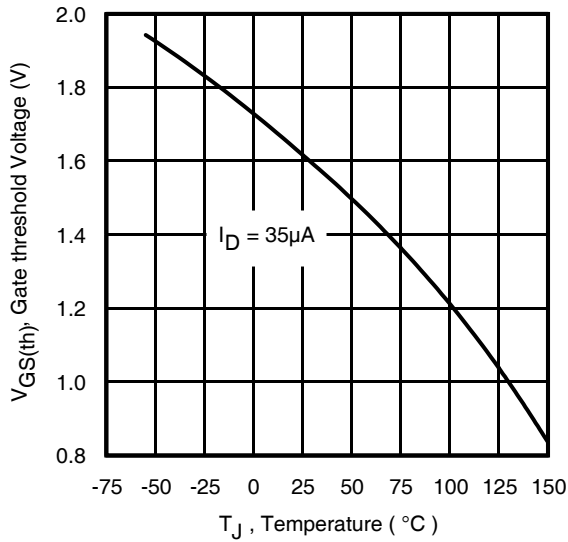
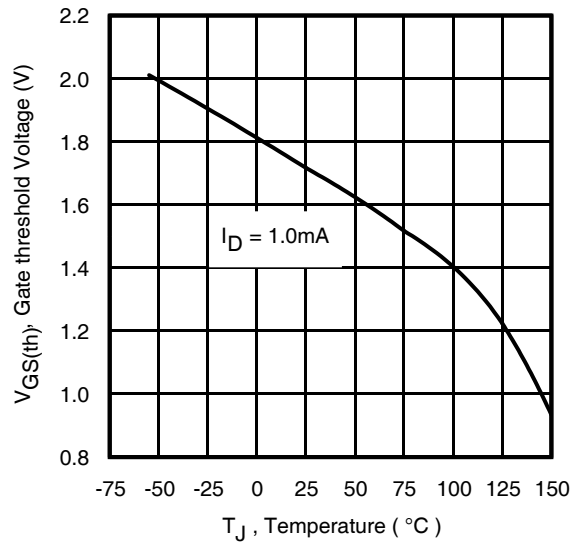
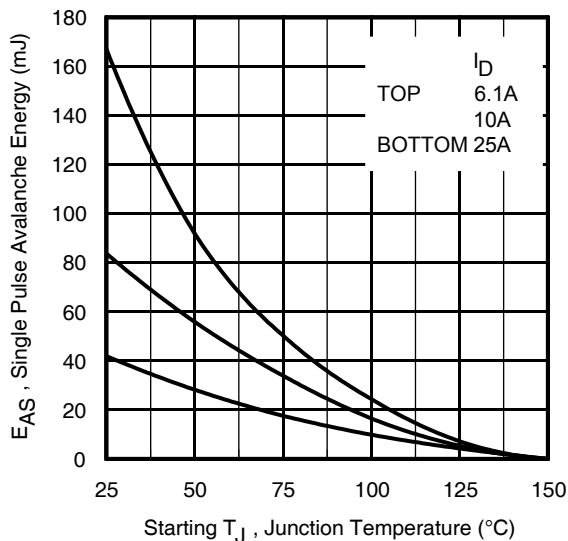
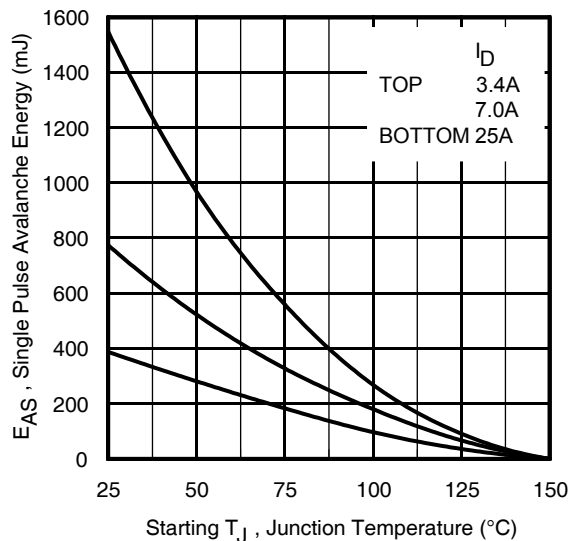
**Diode Characteristics**

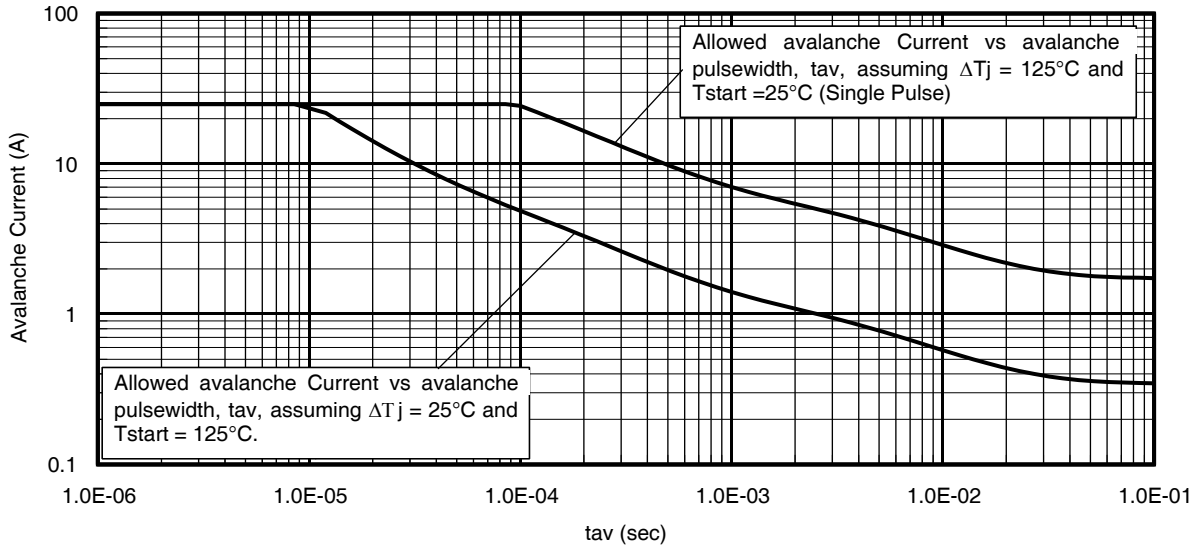
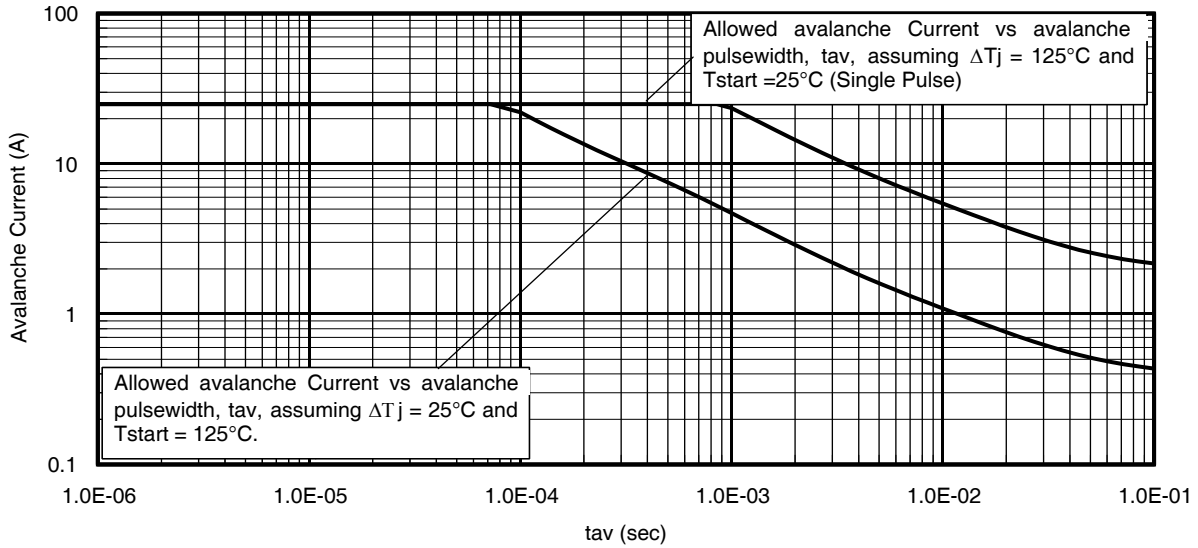
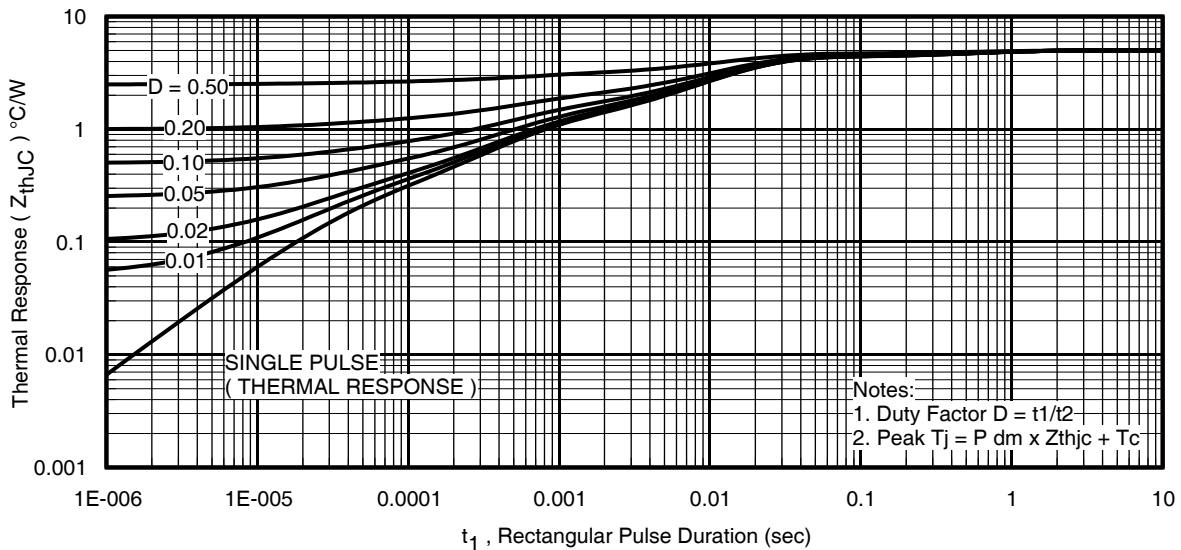
	Parameter		Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	Q1	—	—	25⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
		Q2	—	—	25⑦		
I <sub>SM</sub>	Pulsed Source Current (Body Diode)	Q1	—	—	120⑧	A	T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V③
		Q2	—	—	375⑧		
V <sub>SD</sub>	Diode Forward Voltage	Q1	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V③
		Q2	—	—	0.75		T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V③
t <sub>rr</sub>	Reverse Recovery Time	Q1	—	18	—	ns	Q1 T <sub>J</sub> = 25°C, I <sub>F</sub> = 25A V <sub>DD</sub> = 13V, di/dt = 200A/μs ③
		Q2	—	30	—		
Q <sub>rr</sub>	Reverse Recovery Charge	Q1	—	16	—	nC	Q2 T <sub>J</sub> = 25°C, I <sub>F</sub> = 25A V <sub>DD</sub> = 13V, di/dt = 200A/μs ③
		Q2	—	37	—		


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Typical Transfer Characteristics**

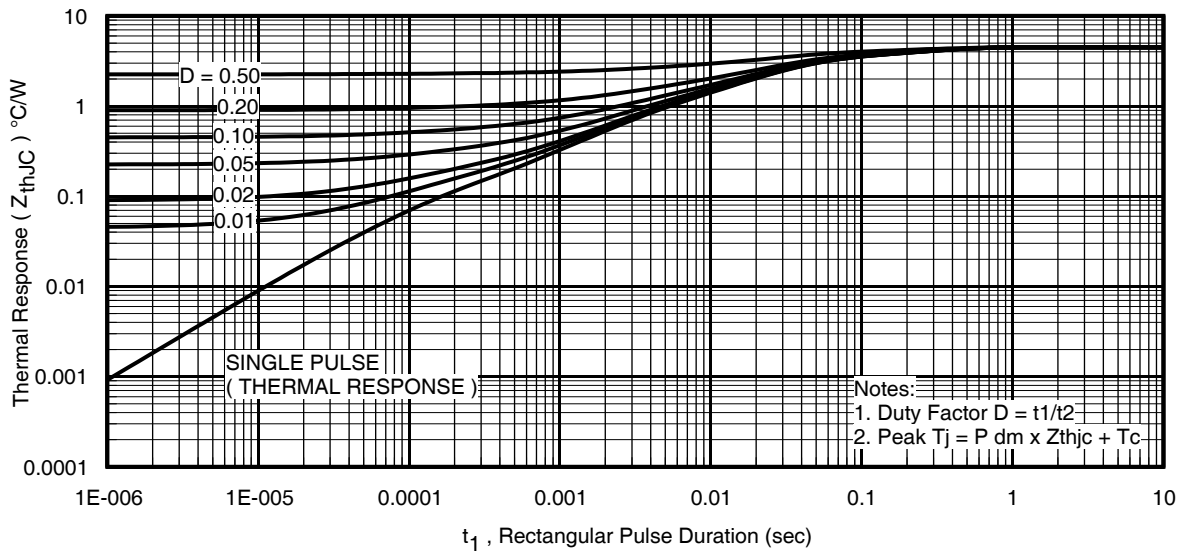

**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 8.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 9.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage

**Fig 11.** Maximum Safe Operating Area

**Fig 12.** Maximum Safe Operating Area


**Fig 13. Normalized On-Resistance vs. Temperature**

**Fig 14. Normalized On-Resistance vs. Temperature**

**Fig 15. Typical Source-Drain Diode Forward Voltage**

**Fig 16. Typical Source-Drain Diode Forward Voltage**

**Fig 17. Typical On-Resistance vs. Gate Voltage**

**Fig 18. Typical On-Resistance vs. Gate Voltage**

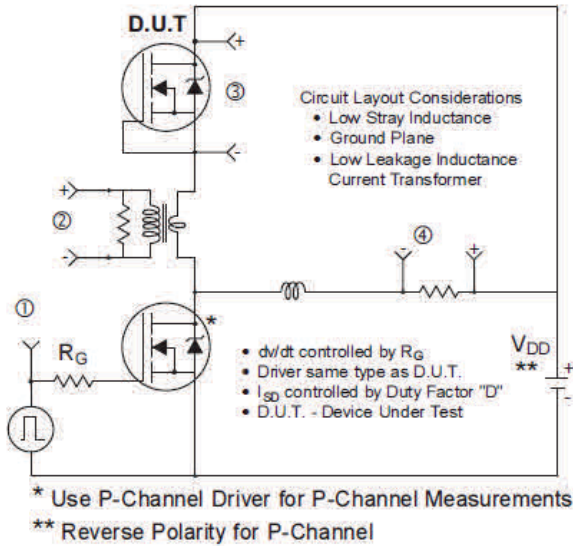
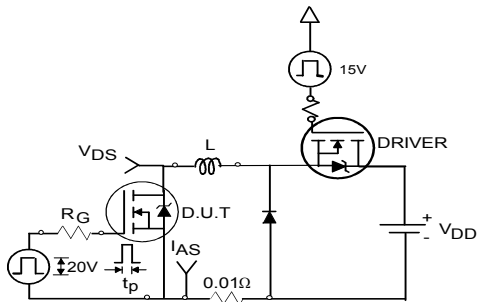
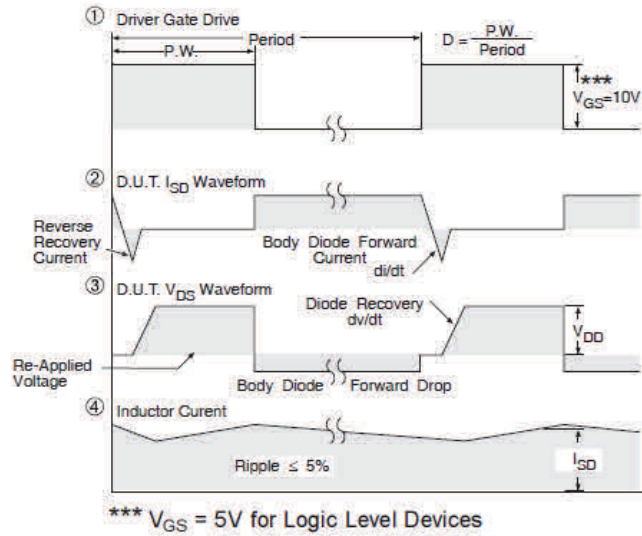
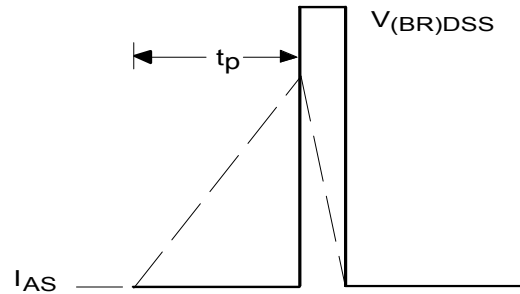
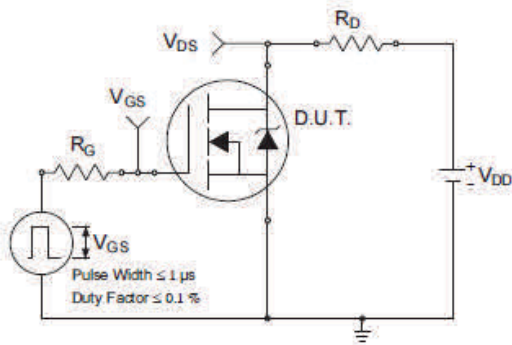
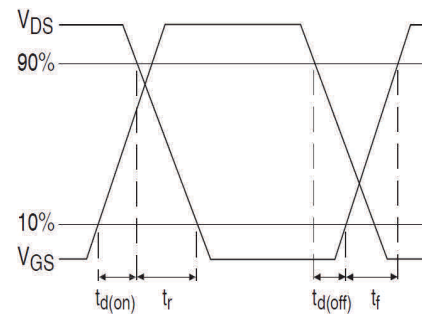
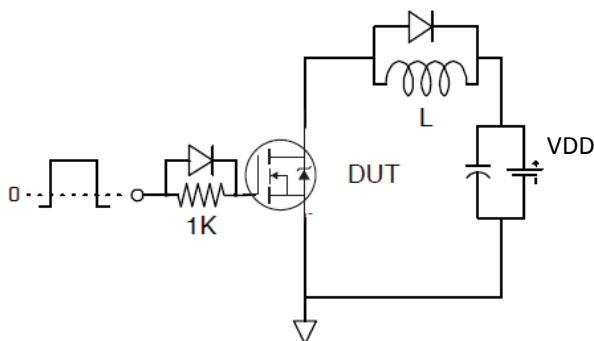
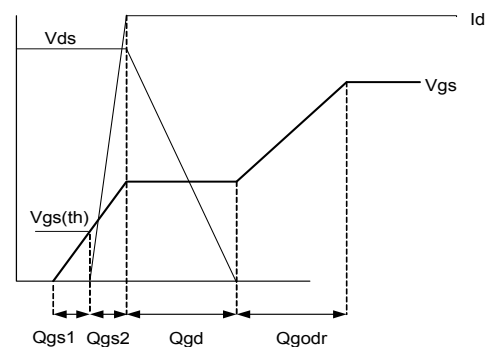
**Q1 - Control FET**

**Fig 19. Maximum Drain Current vs. Case Temperature**
**Q2 - Synchronous FET**

**Fig 20. Maximum Drain Current vs. Case Temperature**

**Fig 21. Threshold Voltage vs. Temperature**

**Fig 22. Threshold Voltage vs. Temperature**

**Fig 23. Maximum Avalanche Energy vs. Drain Current**

**Fig 24. Maximum Avalanche Energy vs. Drain Current**


**Fig 25. Typical Avalanche Current vs. Pulse Width (Q1)**

**Fig 26. Typical Avalanche Current vs. Pulse Width (Q2)**

**Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)**

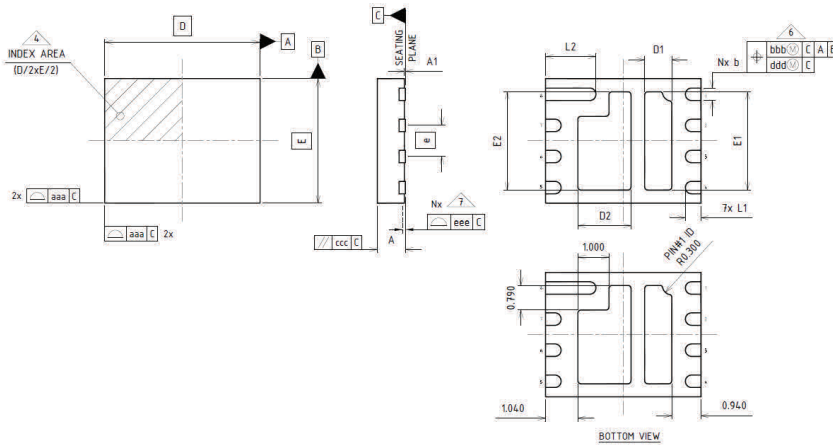




**Fig 28.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)


**Fig 29. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 30a. Unclamped Inductive Test Circuit**

**Fig 30b. Unclamped Inductive Waveforms**

**Fig 31a. Switching Time Test Circuit**

**Fig 31b. Switching Time Waveforms**

**Fig 32a. Gate Charge Test Circuit**

**Fig 32b. Gate Charge Waveform**

### Dual PQFN 5x4 Package Details

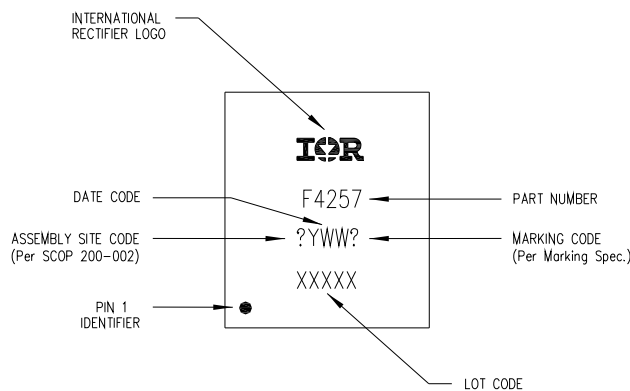


Thickness Symbol	Dimension Table			NOTE
	V-Very Thin			
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.30	0.40	0.45	6
D	5.00 BSC			
E	4.00 BSC			
e	1.00 BSC			
D1	0.72	0.87	0.97	
E1	3.01	3.16	3.26	
D2	1.56	1.71	1.81	
E2	3.01	3.16	3.26	
L1	0.40	0.50	0.60	
L2	1.562	1.662	1.762	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	8			3
NE	4			5
NOTES	1, 2			
LF DWG NO.	B-3664			
REV.	5			

**NOTE:**

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of marked terminal #1 identifier is within the hatched area.
5. NE refers to the maximum number of terminals on E side.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

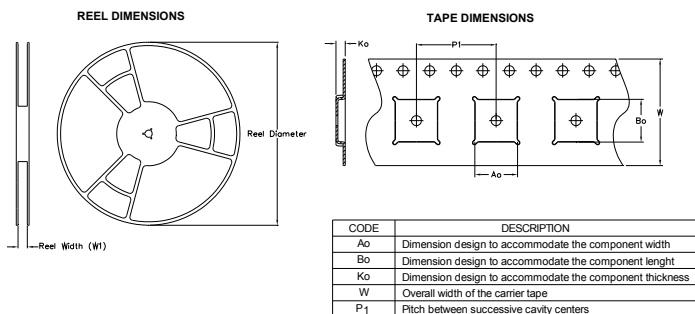
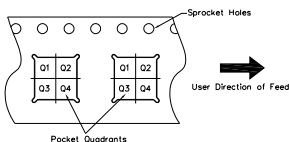
### Dual PQFN 5x4 Part Marking



For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Dual PQFN 5x4 Outline Tape and Reel**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 4 PQFN	13	4000	12.4	5.300	4.300	1.20	8.00	12	Q1

 Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
**Qualification Information†**

<b>Qualification level</b>	Industrial (per JEDEC JESD47F †† guidelines )	
<b>Moisture Sensitivity Level</b>	DUAL PQFN 5mm x 4mm	MSL1 (per JEDEC J-STD-020D††)
<b>RoHS Compliant</b>	Yes	

 † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  
 Q1:  $L = 0.13\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 25\text{A}$ ;  
 Q2:  $L = 1.24\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 25\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:  
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to  $Q1 = 25\text{A}$  &  $Q2 = 25\text{A}$  by source bonding technology.
- ⑧ Pulsed drain current is limited to 100A by source bonding technology.

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