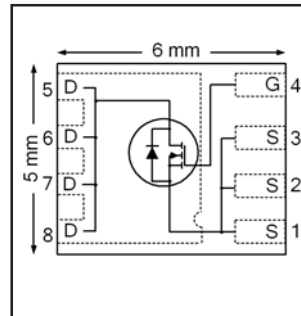


HEXFET® Power MOSFET

$V_{DS}$	<b>30</b>	<b>V</b>
$R_{DS(on) max}$ (@ $V_{GS} = 10V$ )	<b>1.85</b>	<b>mΩ</b>
$Q_g$ (typical)	<b>37</b>	<b>nC</b>
$R_G$ (typical)	<b>1.5</b>	<b>Ω</b>
$I_D$ (@ $T_{c(Bottom)} = 25^\circ C$ )	<b>100</b> Ⓞ	<b>A</b>



**Applications**

- OR-ing MOSFET for 12V (typical) Bus in-Rush Current
- Synchronous MOSFET for Buck Converters
- Battery Operated DC Motor Inverter MOSFET

**Features and Benefits**

**Features**

Low $R_{DS(on)}$ (<1.85mΩ)
Low Thermal Resistance to PCB (<1.1°C/W)
100% $R_g$ tested
Low Profile (<0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in  
⇒

**Benefits**

Lower Conduction Losses
Increased Power Density
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH5301TRPbF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRFH5301TR2PbF	PQFN 5mm x 6mm	Tape and Reel	400	EOL notice # 259

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	± 20	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	35	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	28	
$I_D @ T_{c(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	100Ⓞ	
$I_D @ T_{c(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	100Ⓞ	
$I_{DM}$	Pulsed Drain Current ①	400	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑤	3.6	W
$P_D @ T_{c(Bottom)} = 25^\circ C$	Power Dissipation ⑤	110	
	Linear Derating Factor ⑤	0.029	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑤ are on page 9

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

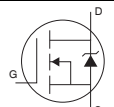
	Parameter	Min.	Typ.	Max.	Units	Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA	
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.55	1.85	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A ③	
		—	2.4	2.9		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 50A ③	
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.80	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA	
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-6.9	—	mV/°C		
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	5.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V	
		—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C	
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V	
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V	
g <sub>fs</sub>	Forward Transconductance	218	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 50A	
Q <sub>g</sub>	Total Gate Charge	—	77	—	nC	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 50A	
Q <sub>g</sub>	Total Gate Charge	—	37	56	nC	V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 50A See Fig.6, 17 & 18	
	Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	9.8			—
	Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	5			—
	Q <sub>gd</sub>	Gate-to-Drain Charge	—	12			—
	Q <sub>godr</sub>	Gate Charge Overdrive	—	10			—
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	17	—	nC		
Q <sub>oss</sub>	Output Charge	—	22	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V	
R <sub>G</sub>	Gate Resistance	—	1.5	2.3	Ω		
t <sub>d(on)</sub>	Turn-On Delay Time	—	21	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 15A R <sub>G</sub> = 1.0Ω See Fig.15	
t <sub>r</sub>	Rise Time	—	78	—			
t <sub>d(off)</sub>	Turn-Off Delay Time	—	22	—			
t <sub>f</sub>	Fall Time	—	23	—			
C <sub>iss</sub>	Input Capacitance	—	5114	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz	
C <sub>oss</sub>	Output Capacitance	—	1017	—			
C <sub>rss</sub>	Reverse Transfer Capacitance	—	406	—			

**Avalanche Characteristics**

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	150	mJ
I <sub>AR</sub>	Avalanche Current ①	—	50	A

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	100	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 50A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	24	36	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 50A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	53	80	nC	di/dt = 300A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic Inductance				


**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	1.1	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	15	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	35	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	22	

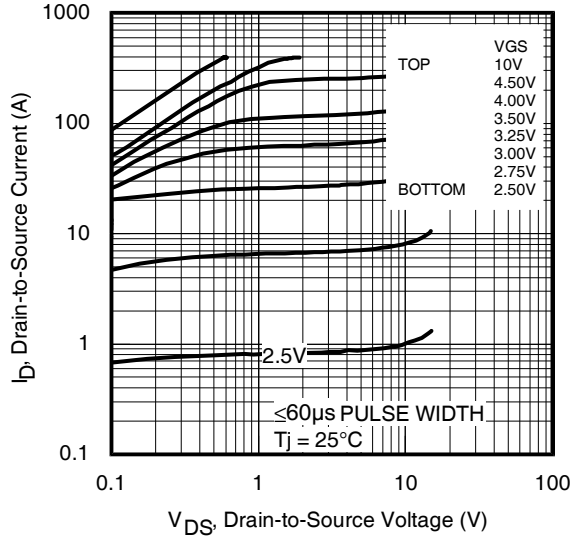


Fig 1. Typical Output Characteristics

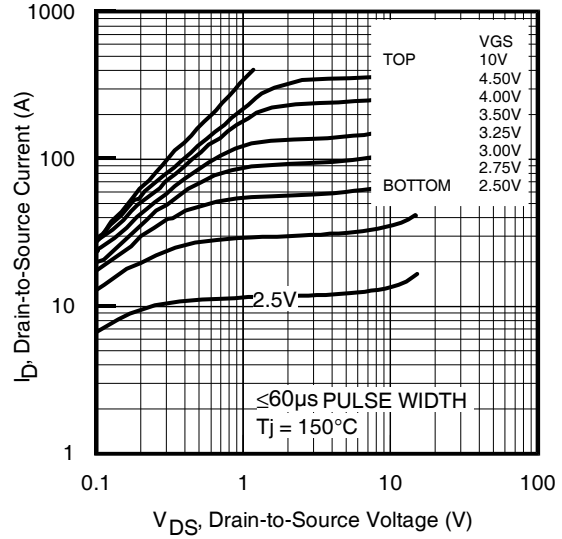


Fig 2. Typical Output Characteristics

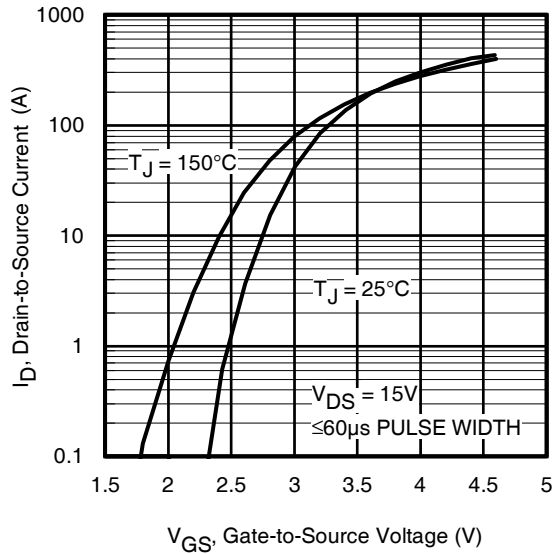


Fig 3. Typical Transfer Characteristics

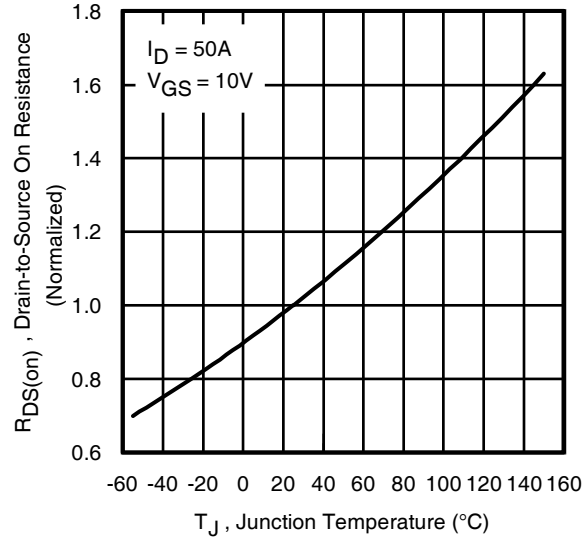


Fig 4. Normalized On-Resistance Vs. Temperature

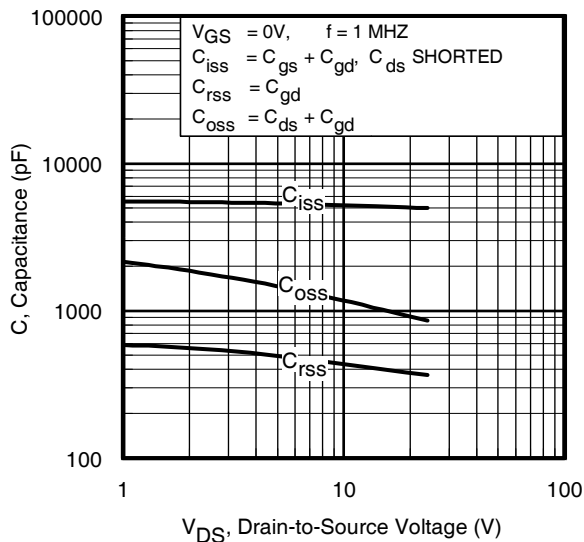


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

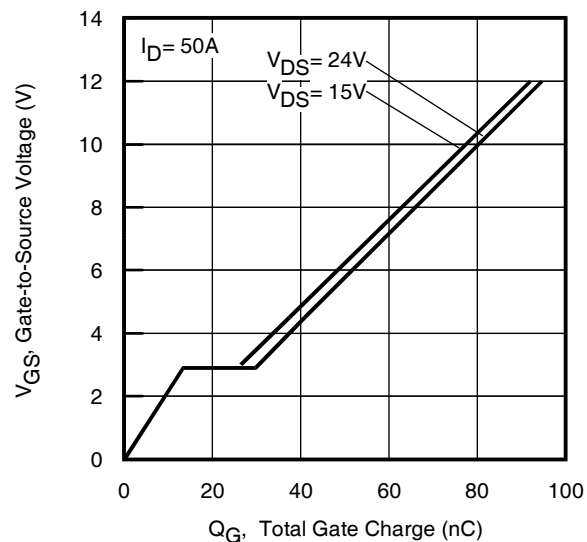
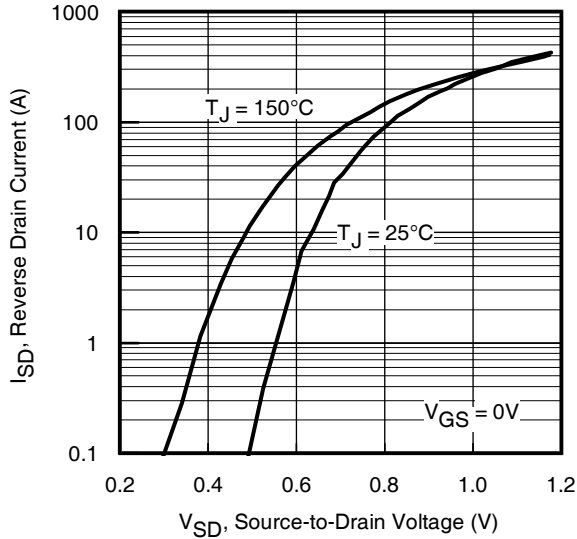
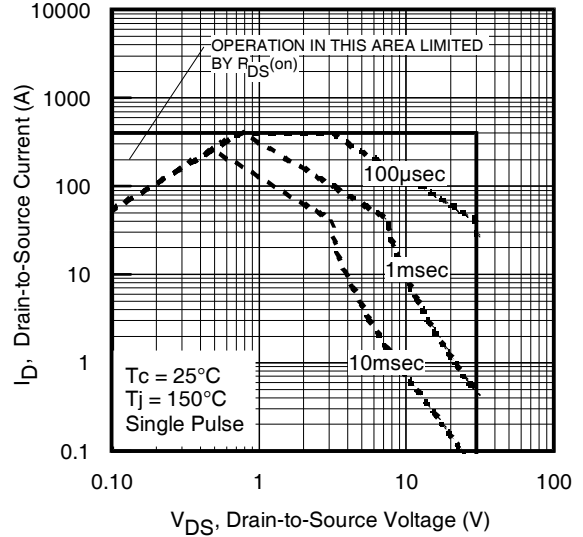


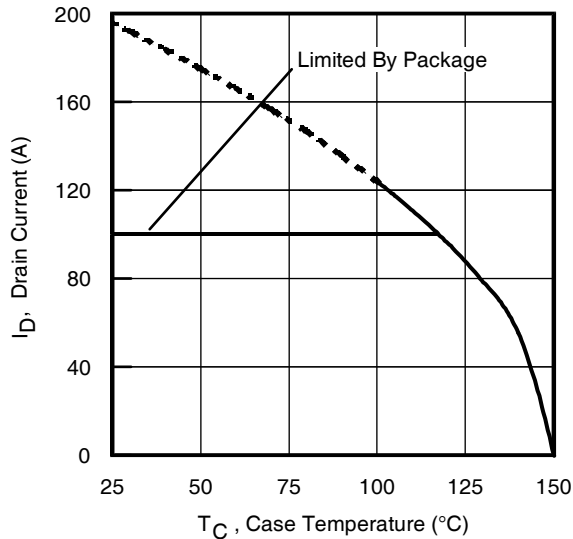
Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



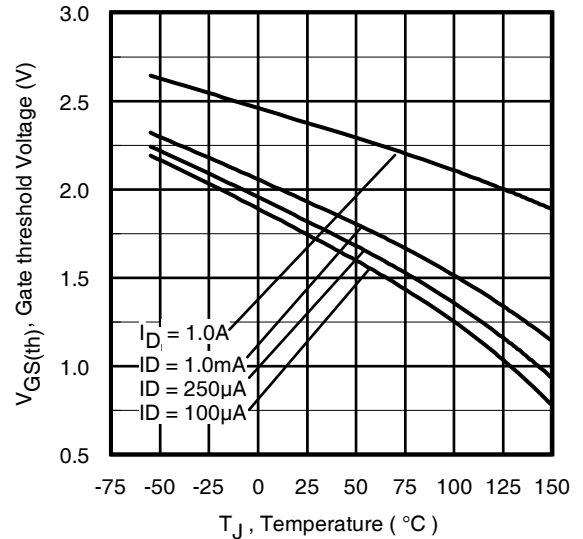
**Fig 7.** Typical Source-Drain Diode Forward Voltage



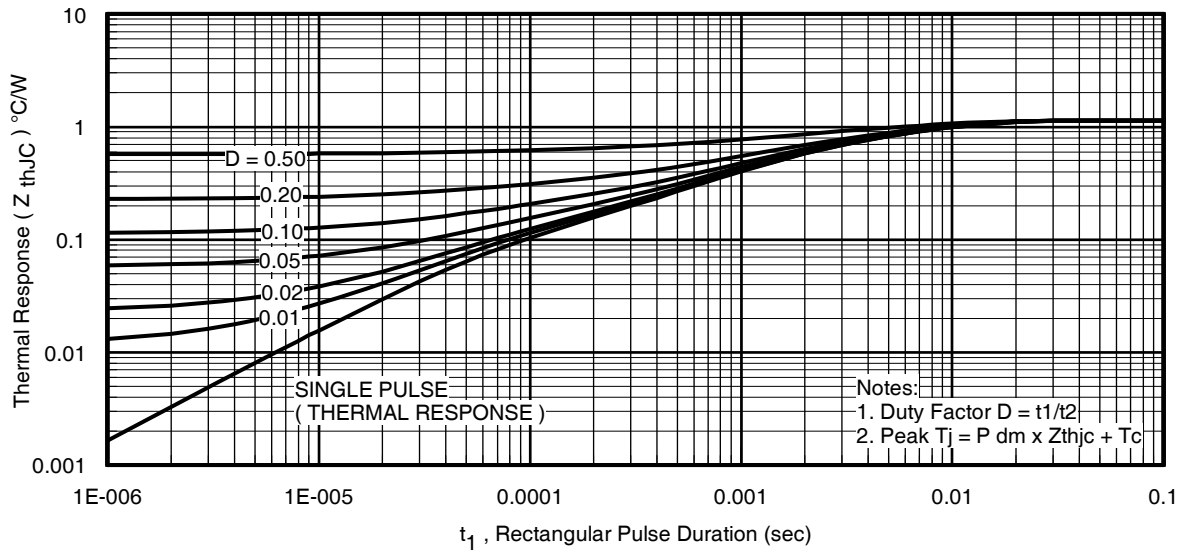
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case (Bottom) Temperature



**Fig 10.** Threshold Voltage Vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

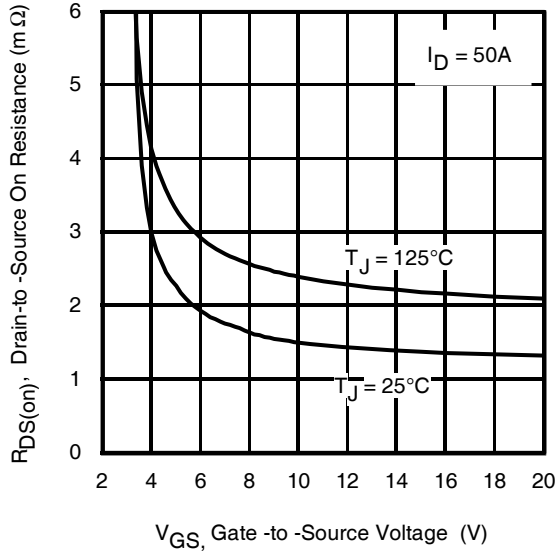


Fig 12. On-Resistance vs. Gate Voltage

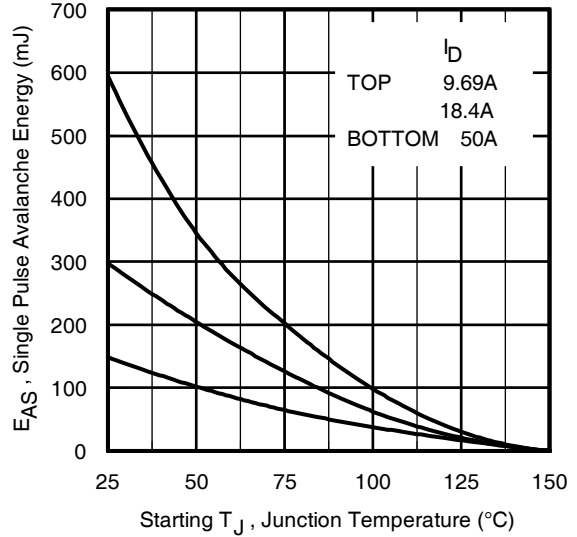


Fig 13. Maximum Avalanche Energy vs. Drain Current

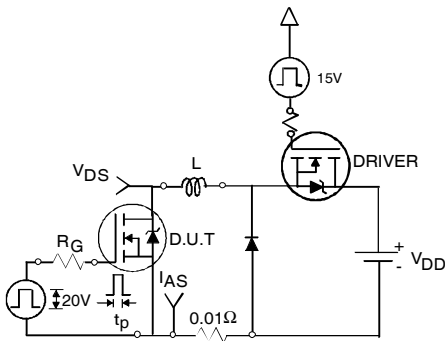


Fig 14a. Unclamped Inductive Test Circuit



Fig 14b. Unclamped Inductive Waveforms



Fig 15a. Switching Time Test Circuit

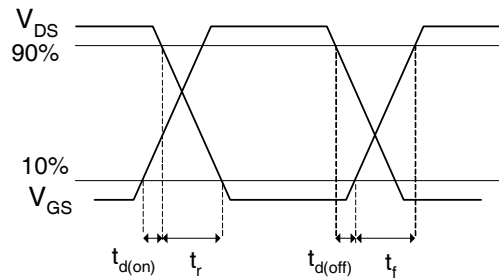
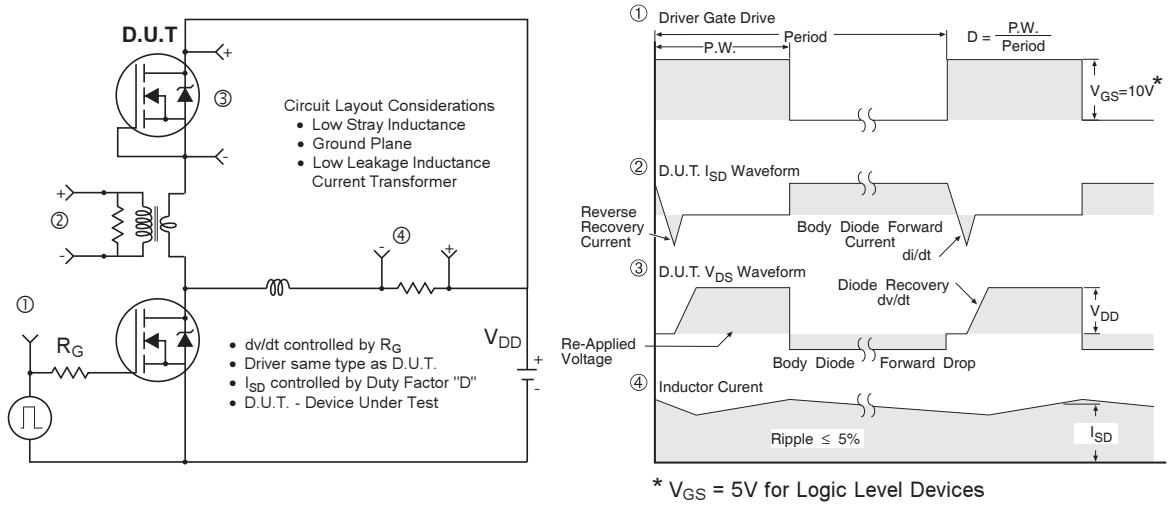
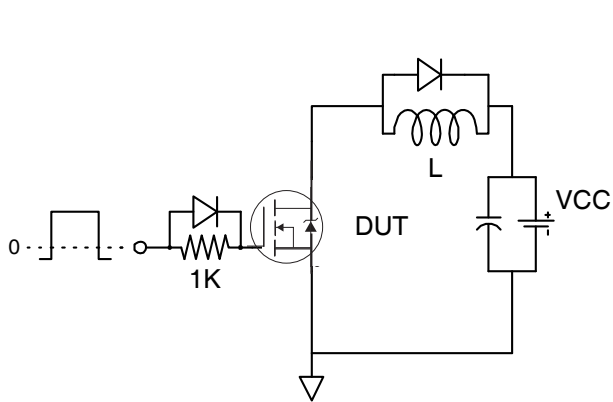


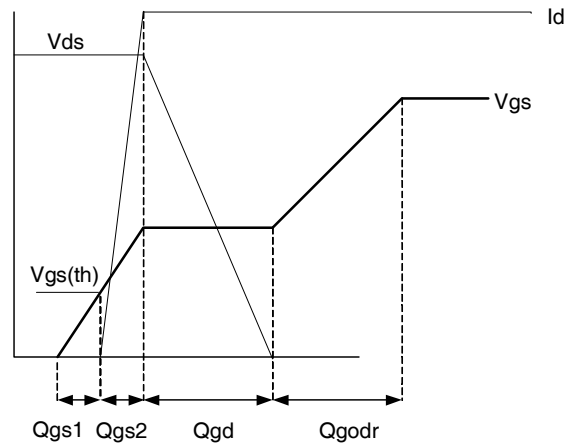
Fig 15b. Switching Time Waveforms



**Fig 16. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**

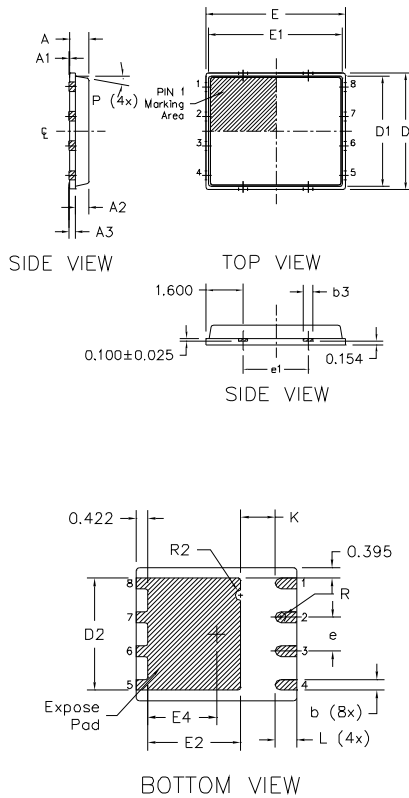


**Fig 17. Gate Charge Test Circuit**



**Fig 18. Gate Charge Waveform**

## PQFN 5x6 Outline "B" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

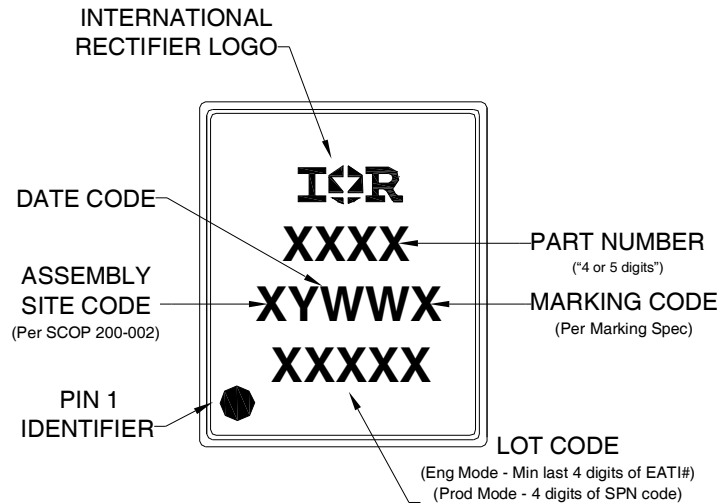
**Note:**

- Dimensions and tolerancing confirm to ASME Y14.5M-1994
- Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
- Caplanarity applies to the expose Heat Slug as well as the terminal
- Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

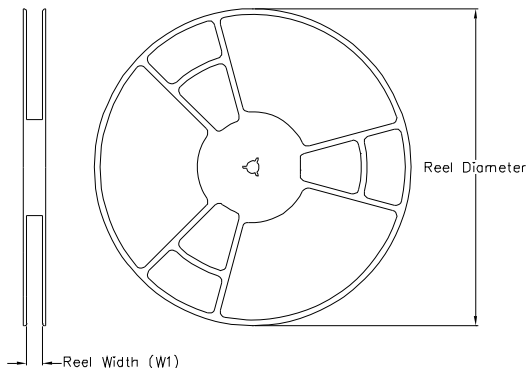
## PQFN 5x6 Part Marking



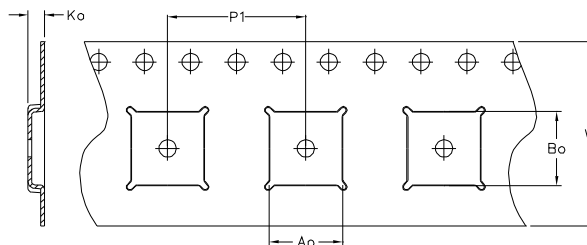
**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

# PQFN 5x6 Tape and Reel

## REEL DIMENSIONS

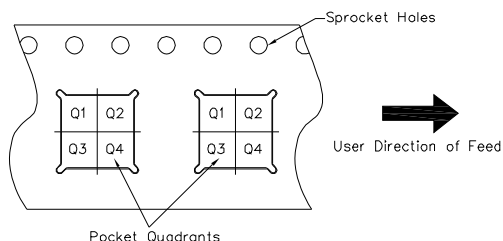


## TAPE DIMENSIONS



CODE	DESCRIPTION
$Ao$	Dimension design to accommodate the component width
$Bo$	Dimension design to accommodate the component length
$Ko$	Dimension design to accommodate the component thickness
$W$	Overall width of the carrier tape
$P1$	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	$Ao$ (mm)	$Bo$ (mm)	$Ko$ (mm)	$P1$ (mm)	$W$ (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup> (per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site  
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.119\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 50\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability

**Revision History**

Date	Comments
12/16/2013	<ul style="list-style-type: none"> <li>• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259)</li> <li>• Updated data sheet with new IR corporate template</li> </ul>
3/12/2015	<ul style="list-style-type: none"> <li>• Updated package outline and tape and reel on pages 7 and 8.</li> </ul>

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