

# IRFI4110GPbF

HEXFET® Power MOSFET

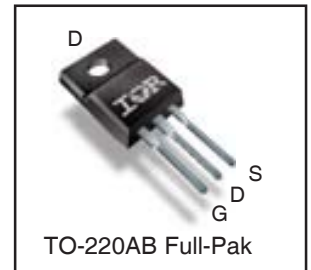
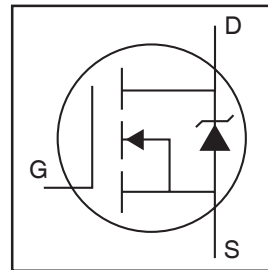
## Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

$V_{DSS}$	<b>100V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>3.7mΩ</b>
	<b>4.5mΩ</b>
$I_D$ (Silicon Limited)	<b>72A</b>

## Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	72	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	51	
$I_{DM}$	Pulsed Drain Current ①	290	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	61	W
	Linear Derating Factor	0.41	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	27	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

## Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	71	mJ
$I_{AR}$	Avalanche Current	43	A
$E_{AR}$	Repetitive Avalanche Energy ④	6.1	mJ

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	2.46	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	65	

Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.7	4.5	m $\Omega$	$V_{GS} = 10V, I_D = 43A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions	
gfs	Forward Transconductance	260	—	—	S	$V_{DS} = 50V, I_D = 43A$	
$Q_g$	Total Gate Charge	—	190	290	nC	$I_D = 43A$ $V_{DS} = 50V$ $V_{GS} = 10V$ ④	
$Q_{gs}$	Gate-to-Source Charge	—	40	—			
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	49	—			
$R_G$	Gate Resistance	—	1.3	—			$\Omega$
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 65V$ $I_D = 43A$ $R_G = 2.6\Omega$ $V_{GS} = 10V$ ④	
$t_r$	Rise Time	—	58	—			
$t_{d(off)}$	Turn-Off Delay Time	—	81	—			
$t_f$	Fall Time	—	71	—			
$C_{iss}$	Input Capacitance	—	9540	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz$	
$C_{oss}$	Output Capacitance	—	680	—			
$C_{rss}$	Reverse Transfer Capacitance	—	300	—			
$C_{oss\ eff. (ER)}$	Effective Output Capacitance (Energy Related)⑥	—	760	—			$V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑥
$C_{oss\ eff. (TR)}$	Effective Output Capacitance (Time Related)⑤	—	1120	—			$V_{GS} = 0V, V_{DS} = 0V$ to $80V$ ⑤

## Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	72	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ②⑦	—	—	290		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 43A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}$ $V_R = 85V,$ $T_J = 125^\circ\text{C}$ $I_F = 43A$
		—	60	90		
$Q_{rr}$	Reverse Recovery Charge	—	100	150	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $di/dt = 100A/\mu s$ ④
		—	140	210		
$I_{RRM}$	Reverse Recovery Current	—	3.5	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.077mH$   
 $R_G = 25\Omega, I_{AS} = 43A, V_{GS} = 10V$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 43A, di/dt \leq 1600A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

- ⑤  $C_{oss\ eff. (TR)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to  $80\% V_{DSS}$ .
- ⑥  $C_{oss\ eff. (ER)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to  $80\% V_{DSS}$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

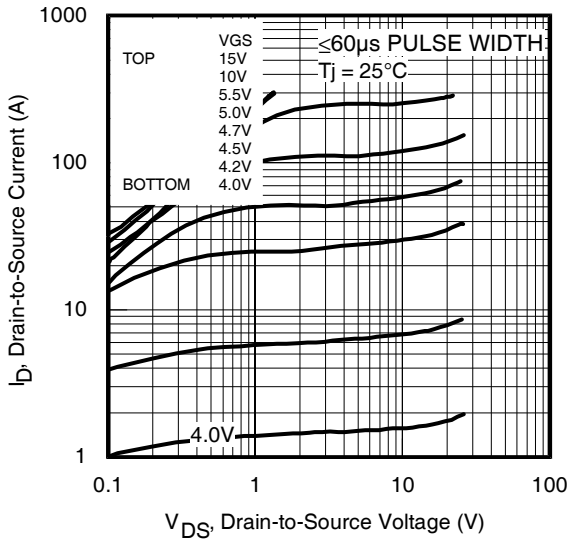


Fig 1. Typical Output Characteristics

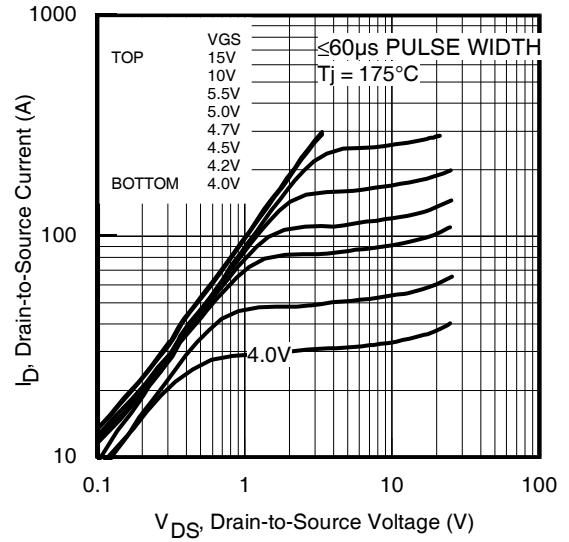


Fig 2. Typical Output Characteristics

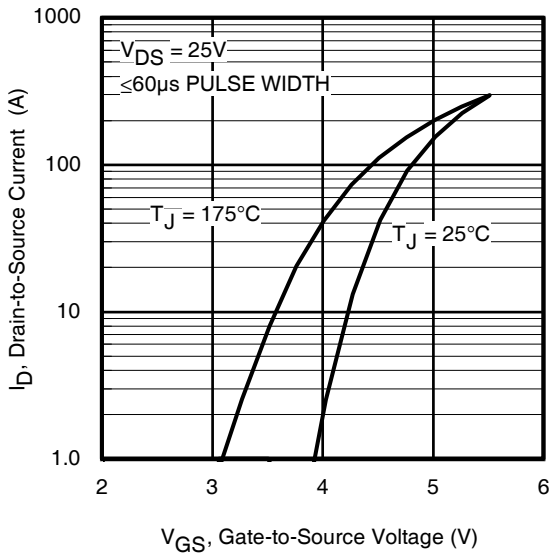


Fig 3. Typical Transfer Characteristics

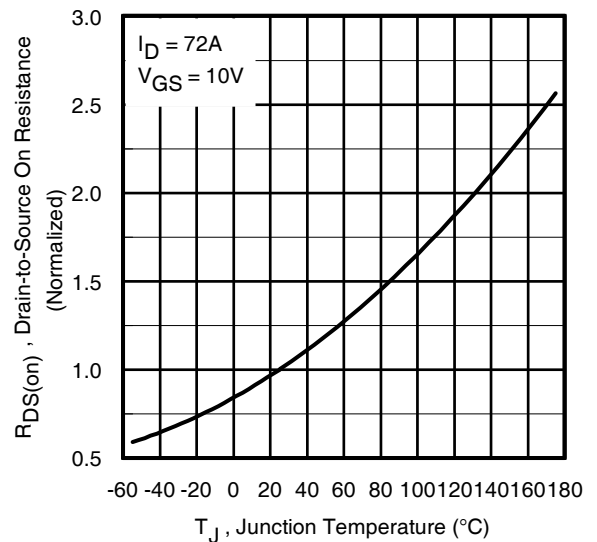


Fig 4. Normalized On-Resistance vs. Temperature

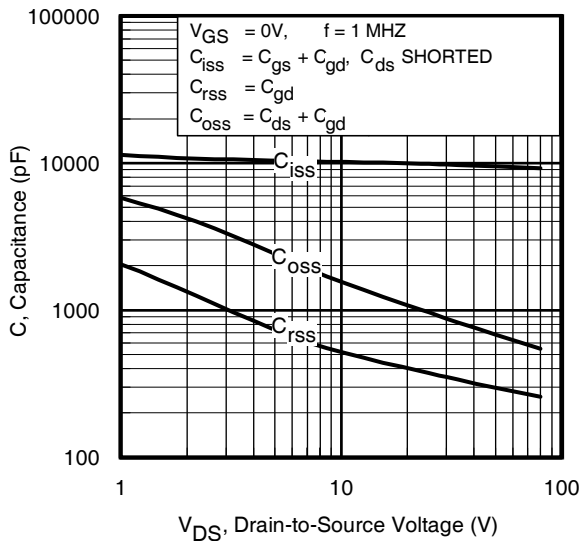


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

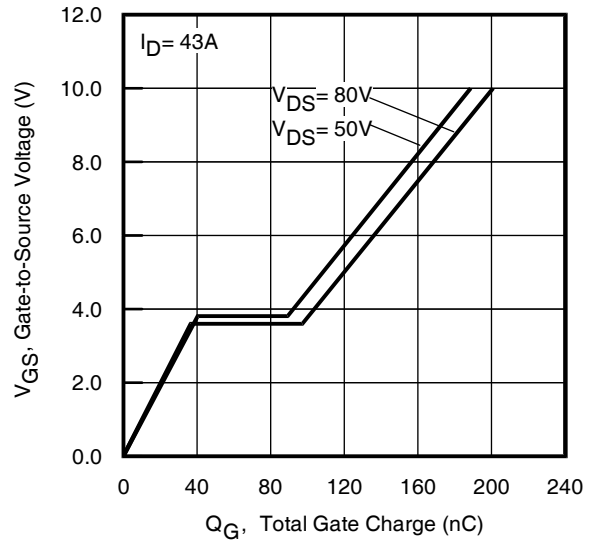


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

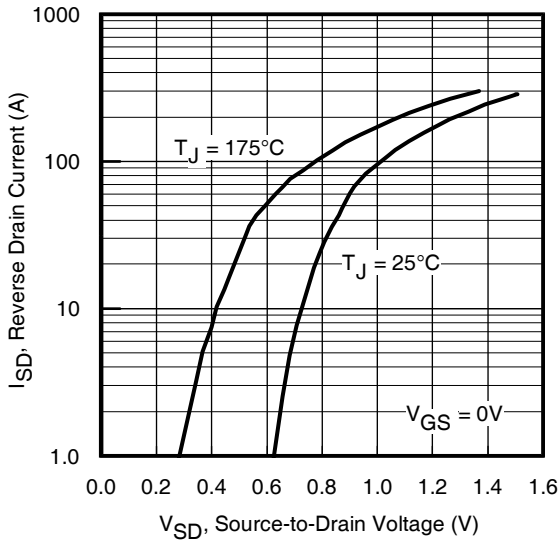


Fig 7. Typical Source-Drain Diode Forward Voltage

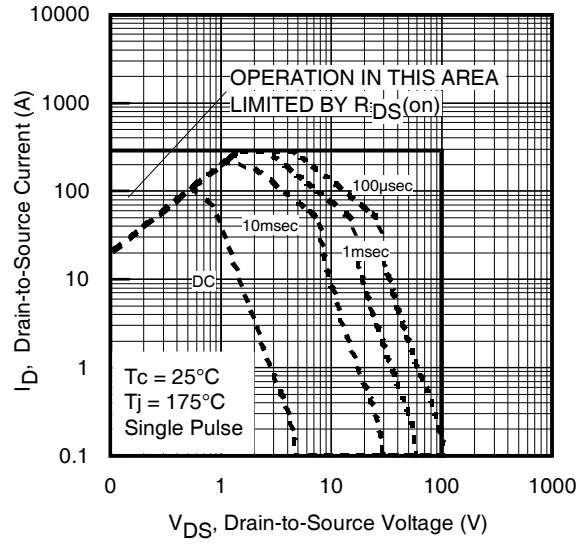


Fig 8. Maximum Safe Operating Area

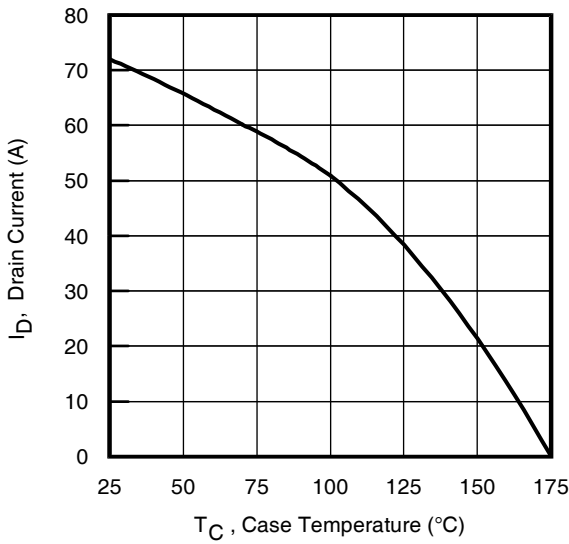


Fig 9. Maximum Drain Current vs. Case Temperature

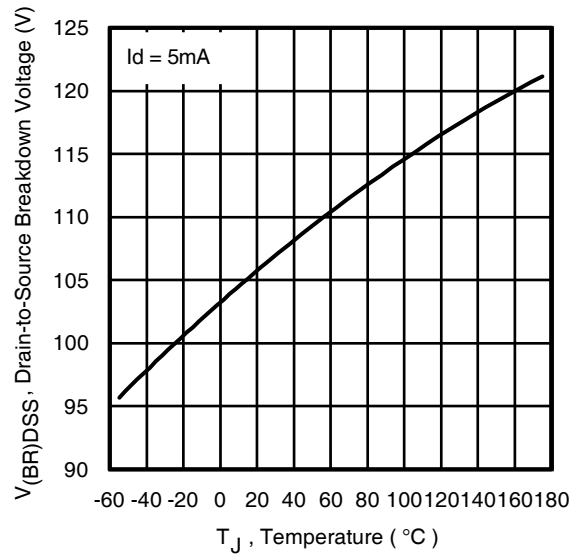


Fig 10. Drain-to-Source Breakdown Voltage

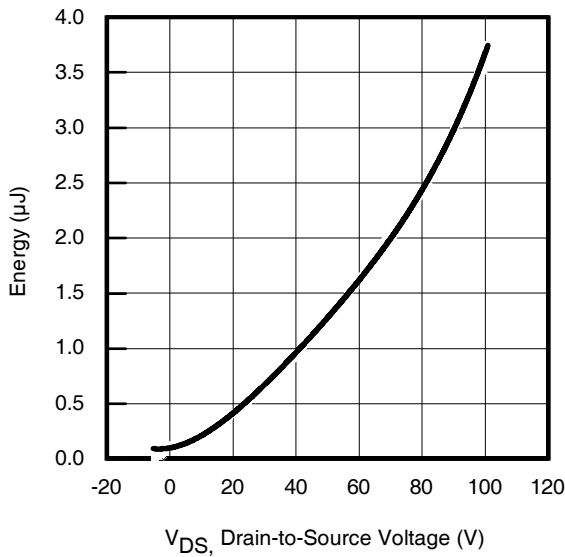


Fig 11. Typical  $C_{OSS}$  Stored Energy

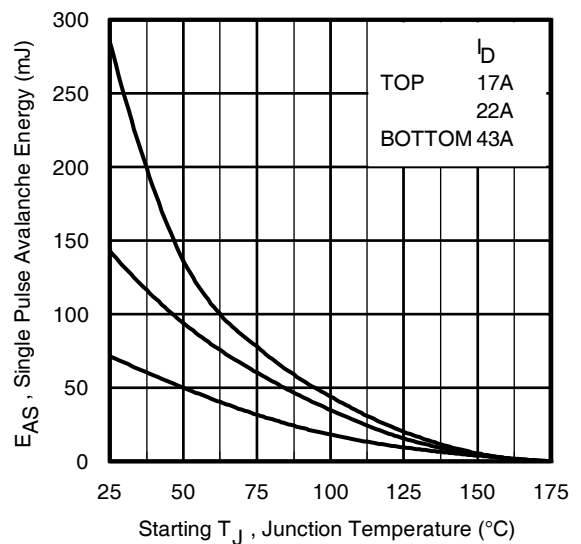


Fig 12. Maximum Avalanche Energy vs. Drain Current

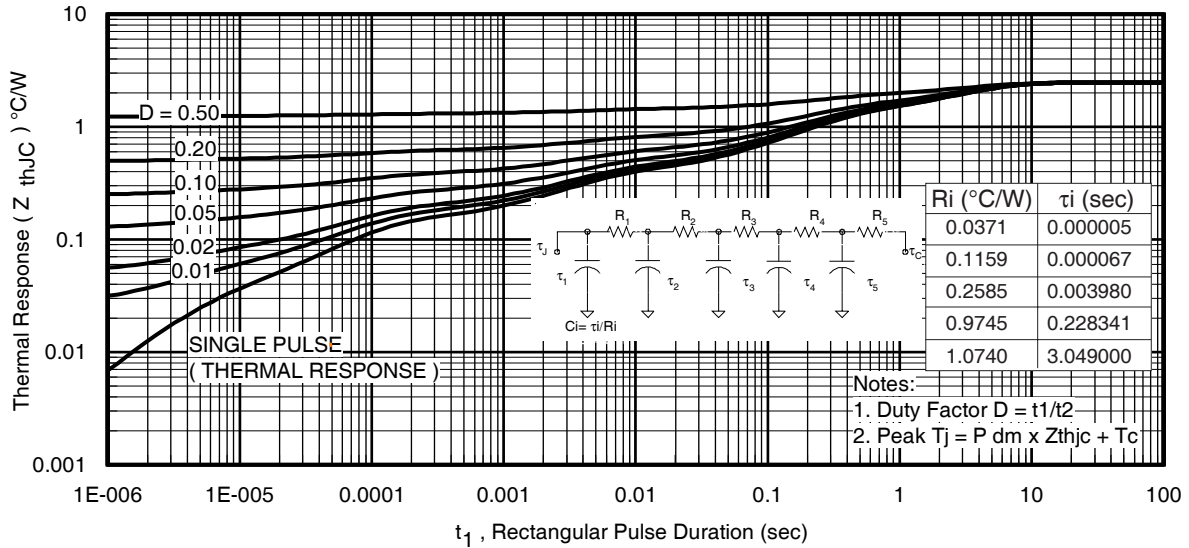


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

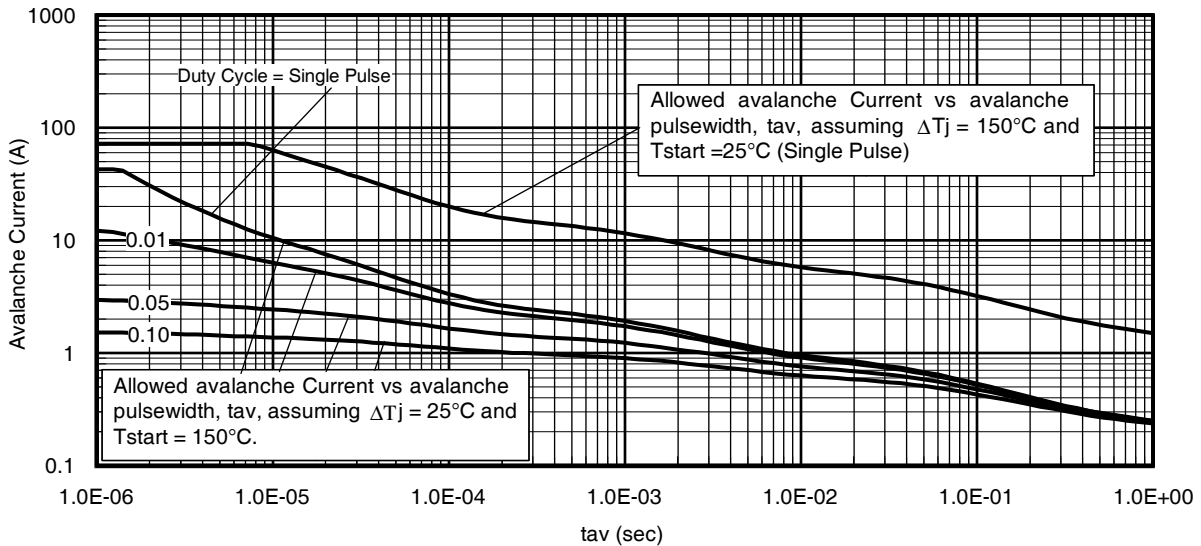


Fig 14. Typical Avalanche Current vs. Pulsewidth

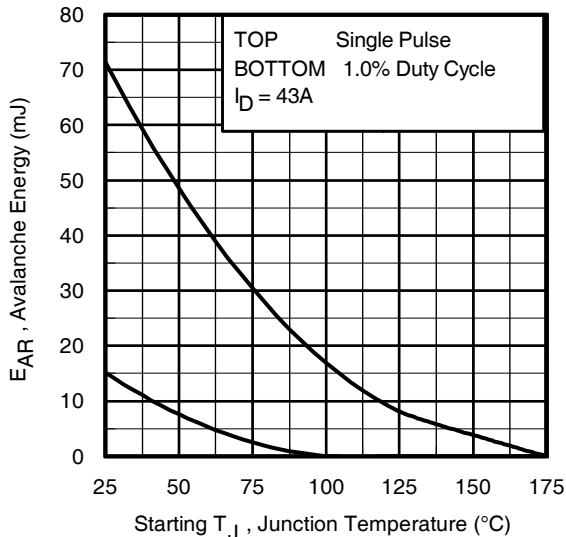


Fig 15. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thjc}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thjc}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

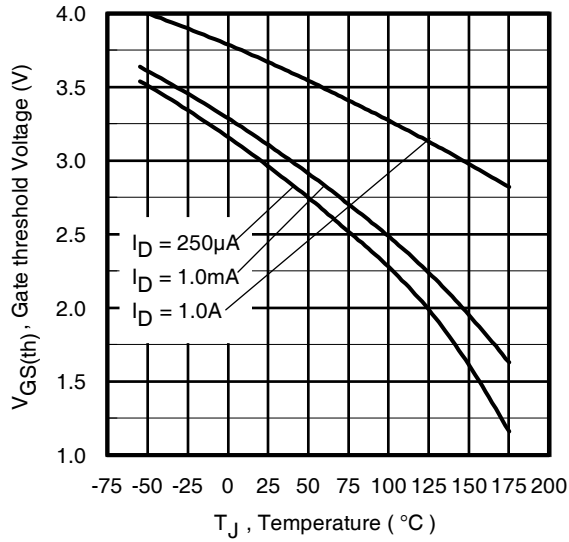


Fig 16. Threshold Voltage vs. Temperature

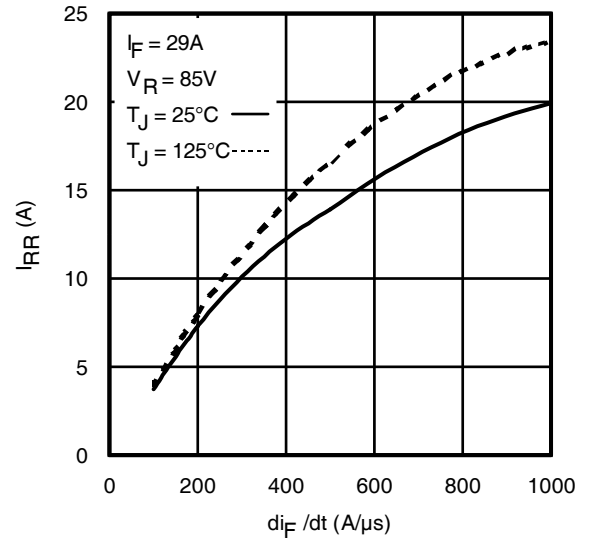


Fig. 17 - Typical Recovery Current vs.  $di_f/dt$

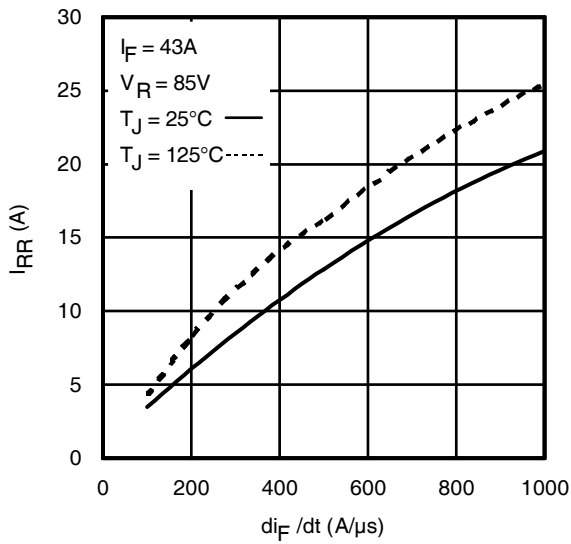


Fig. 18 - Typical Recovery Current vs.  $di_f/dt$

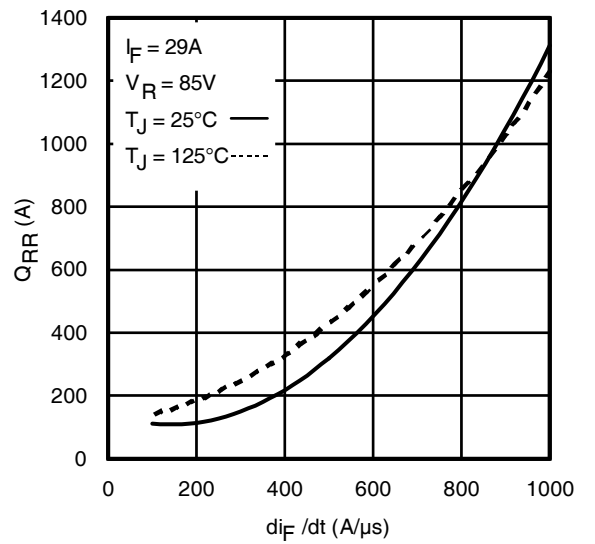


Fig. 19 - Typical Stored Charge vs.  $di_f/dt$

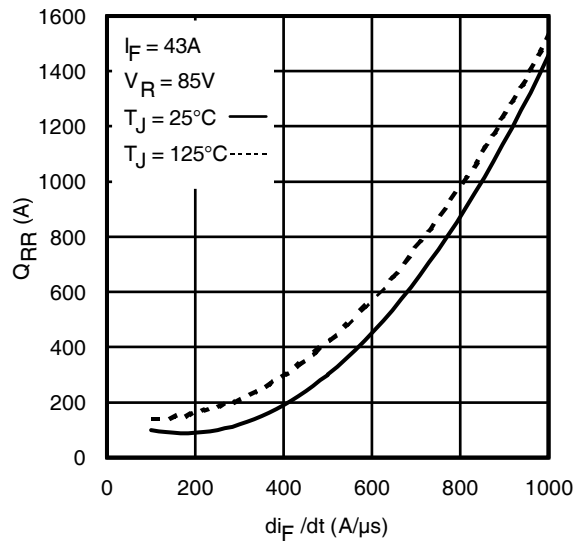
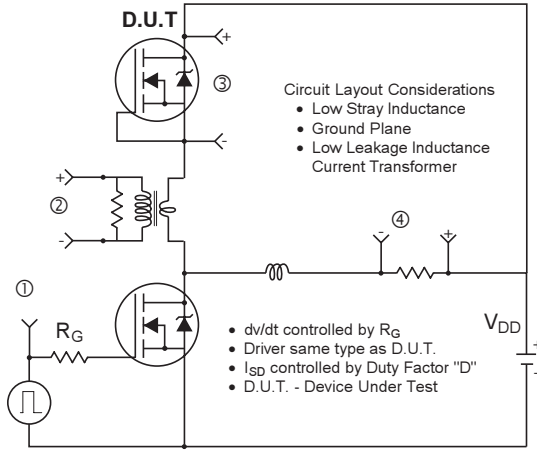
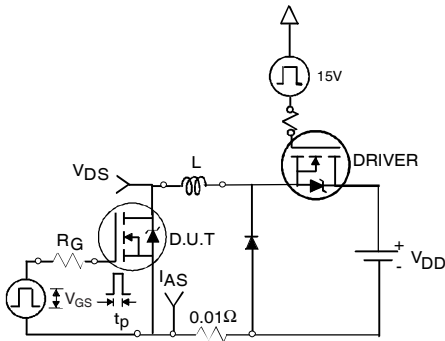


Fig. 20 - Typical Stored Charge vs.  $di_f/dt$



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 21a. Unclamped Inductive Test Circuit**



**Fig 21b. Unclamped Inductive Waveforms**



**Fig 22a. Switching Time Test Circuit**



**Fig 22b. Switching Time Waveforms**



**Fig 23a. Gate Charge Test Circuit**

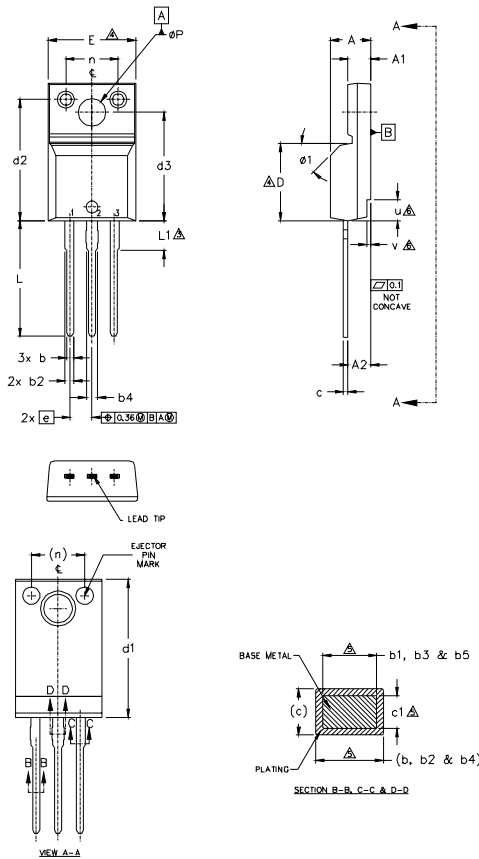


**Fig 23b. Gate Charge Waveform**

# IRFI4110GPbF

## TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	5
A1	2.57	2.83	.101	.111	
A2	2.51	2.93	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	
d	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	4
d3	12.30	12.93	.484	.509	
E	9.63	10.75	.379	.423	4
e	2.54	BSC	.100	BSC	
L	13.20	13.72	.520	.540	3
L1	3.37	3.67	.122	.145	
n	6.05	6.60	.238	.260	6
phi P	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	6
v	0.40	0.50	.016	.020	
phi 1	-	45*	-	45*	

- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
  - 5.0 DIMENSION b1, b5, b5 & c1 APPLY TO BASE METAL ONLY.
  - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
  - 7.0 CONTROLLING DIMENSION : INCHES.

**LEAD ASSIGNMENTS**

- HEXFET**
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE

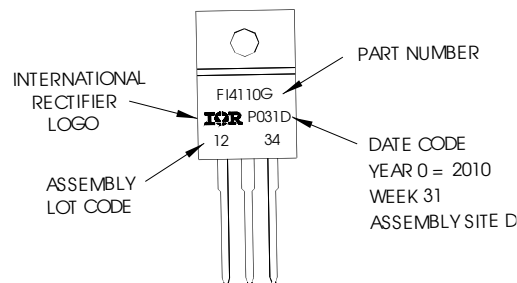
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI4110G  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW31, 2010

Notes: - "P" in assembly line position indicates "Lead-Free"  
- "G" suffix in part number indicates "Halogen-Free"



TO-220AB Full-Pak package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.



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