MAX1415/MAX1416

16-Bit, Low-Power, 2-Channel, Sigma-Delta ADCs

General Description

The MAX1415/MAX1416 low-power, 2-channel, serial-output analog-to-digital converters (ADCs) use a sigma-delta modulator with a digital filter to achieve 16-bit resolution with no missing codes. These ADCs are pin-compatible upgrades to the MX7705/AD7705. The MAX1415/MAX1416 feature an internal oscillator (1MHz or 2.4576MHz), an on-chip input buffer, and a programmable gain amplifier (PGA). The devices offer an SPI-/QSPI™-/MICROWIRE®-compatible serial interface.

The MAX1415/MAX1416 are available in 16-pin PDIP, SO, and TSSOP packages.

Applications

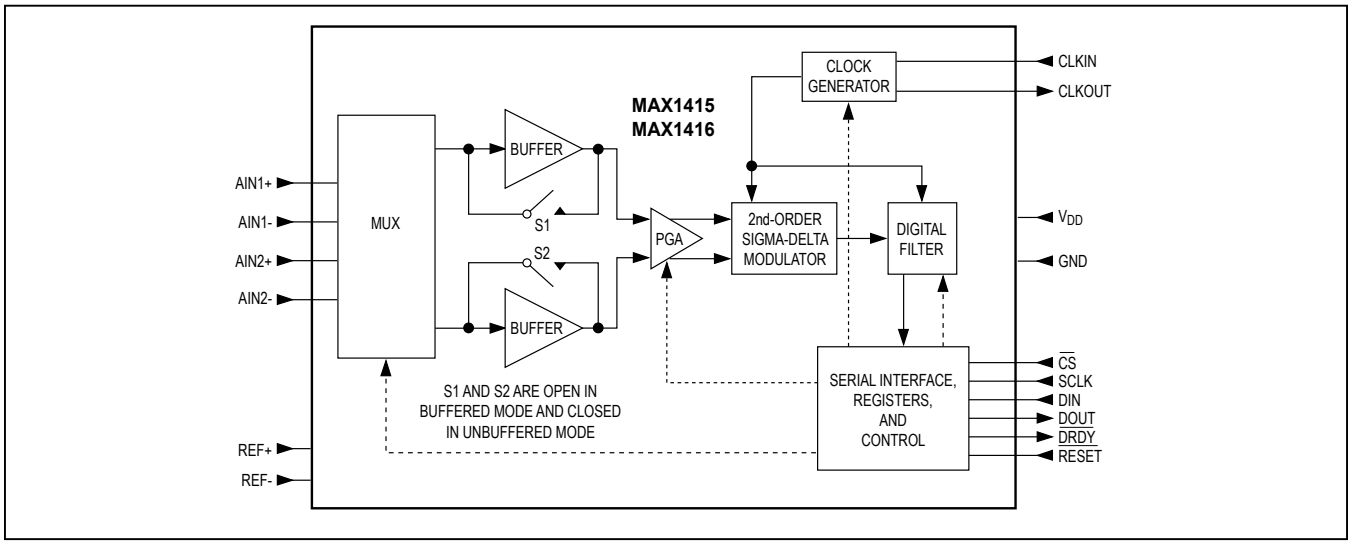
- Industrial Instruments
- Weigh Scales
- Strain-Gauge Measurements
- Loop-Powered Systems
- Flow and Gas Meters
- Medical Instrumentation
- Pressure Transducers
- Thermocouple Measurements
- RTD Measurements

Ordering Information ***continued at end of data sheet.***

Benefits and Features

- Improve Measurement Quality with Excellent DC Accuracy
  - 16-Bit Sigma-Delta ADC with Two Fully-Differential Input Channels
  - 0.0015% INL (max) with No Missing Codes
- Minimize Power Consumption with Low-Power Dissipation
  - 1.2mW (max) 3V supply
  - 2µA (typ) Power-Down Current
- Lower System Cost with Integrated Functionality
  - PGA with 1 to 128 Programmable Gain
  - Optional Input Buffers
  - > 98dB 50Hz/60Hz Rejection
- Increase System Accuracy with Built-in Self Calibration
  - On-Demand Offset and Gain Self-Calibration and System Calibration
  - User-Programmable Offset and Gain Registers
- Flexible Single-Supply Options
  - 2.7V to 3.6V (MAX1415)
  - 4.75V to 5.25V (MAX1416)
- Pin Compatible Upgrades for MX7705/AD7705

Functional Diagram



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maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
All Other Pins to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current Input into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin PDIP (derate 10.5mW/°C above +70°C) 842mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C).....755mW
16-Pin Wide SO (derate 9.5mW/°C above +70°C) 762mW
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -60°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics—MAX1415

(V_{DD} = 3V, V_{GND} = 0V, V_{REF+} = 1.225V, V_{REF-} = GND, external f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution (No Missing Codes)			16			Bits
Output Noise				(Tables 1, 3)		µV
Integral Nonlinearity	INL	Gain = 1, bipolar mode, unbuffered			±0.0015	%FSR
Unipolar Offset Error		After calibration		(Note 1)		µV
Unipolar Offset Drift		(Note 2)		0.5		µV/°C
Bipolar Zero Error		After calibration		(Note 1)		µV
Bipolar Zero Drift (Note 2)		Gain = 1 to 4		0.5		µV/°C
		Gain = 8 to 128		0.1		
Positive Full-Scale Error		After calibration		(Notes 1, 3)		µV
Full-Scale Drift		(Notes 2, 4)		0.5		µV/°C
Gain Error		After calibration		(Notes 1, 5)		µV
Gain Drift		(Notes 2, 6)		0.5		ppm of FSR/°C
Bipolar Negative Full-Scale Error		After calibration		±0.003		%FSR
Bipolar Negative Full-Scale Drift (Note 2)		Gain = 1 to 4		1		µV/°C
		Gain = 8 to 128		0.6		
ANALOG INPUTS (AIN1+, AIN1-, AIN2+, AIN2-)						
AIN Differential Input Voltage Range (Note 7)		Unipolar input range	0		V_{REF} / GAIN	V
		Bipolar input range	-V_{REF} / GAIN		V_{REF} / GAIN	
AIN Absolute Input Voltage Range (Note 8)		Unbuffered	GND - 30mV		V_{DD} + 30mV	V
		Buffered	GND + 50mV		V_{DD} - 1.5V	
AIN DC Leakage Current		Unselected input channel			1	nA

Electrical Characteristics—MAX1415 (continued)

(V_{DD} = 3V, V_{GND} = 0V, V_{REF+} = 1.225V, V_{REF-} = GND, external f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN Input Capacitance		Gain = 1		34		pF
		Gain = 2		38		
		Gain = 4		45		
		Gain = 8 to 128		60		
AIN Input Sampling Rate	f_S	Gain = 1 to 128			f_{CLKIN} / 64	MHz
Input Common-Mode Rejection	CMR	Gain = 1		105		dB
		Gain = 2		110		
		Gain = 4		120		
		Gain = 8 to 128		130		
Normal-Mode 50Hz Rejection		For filter notches of 25Hz, 50Hz, ±0.02 x f_{NOTCH}		98		dB
Normal-Mode 60Hz Rejection		For filter notches of 20Hz, 60Hz, ±0.02 x f_{NOTCH}		98		dB
Common-Mode 50Hz Rejection		For filter notches of 25Hz, 50Hz, ±0.02 x f_{NOTCH}		150		dB
Common-Mode 60Hz Rejection		For filter notches of 20Hz, 60Hz, ±0.02 x f_{NOTCH}		150		dB
EXTERNAL REFERENCE (REF+, REF-)						
REF Differential Input Range	V_{REF}	(Note 9)	1.00		1.75	V
REF Absolute Input Voltage Range			GND		V_{DD}	V
REF Input Capacitance		Gain = 1 to 128		10		pF
REF Input Sampling Rate	f_S				f_{CLKIN} / 64	MHz
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.4	V
Input Hysteresis	V_{HYST}	DIN, $\overline{CS}$, $\overline{RESET}$		250		mV
		SCLK		500		
Input Current	I_{IN}				±1	µA
Input Capacitance				5		pF
CLKIN INPUT						
CLKIN Input High Voltage	V_{CLKINH}		2.5			V
CLKIN Input Low Voltage	V_{CLKINL}				0.4	V
CLKIN Input Current	I_{CLKIN}				±10	µA
DIGITAL OUTPUTS (DOUT, $\overline{DRDY}$, CLKOUT)						
Output-Voltage Low	V_{OL}	DOUT and $\overline{DRDY}$, I_{SINK} = 100µA			0.4	V
		CLKOUT, I_{SINK} = 10µA			0.4	

Electrical Characteristics—MAX1415 (continued)

(V_{DD} = 3V, V_{GND} = 0V, V_{REF+} = 1.225V, V_{REF-} = GND, external f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output-Voltage High	V_{OH}	DOUT and $\overline{DRDY}$, I_{SOURCE} = 100µA		V_{DD} -0.6V			V
		CLKOUT, I_{SOURCE} = 10µA		V_{DD} -0.6V			
Tri-State Leakage Current	I_L	DOUT only				±10	µA
Tri-State Output Capacitance	C_{OUT}	DOUT only			9		pF
SYSTEM CALIBRATION							
Full-Scale Calibration Range		GAIN = selected PGA gain (1 to 128) (Note 10)		-1.05 x V_{REF} / GAIN		1.05 x V_{REF} / GAIN	V
Offset Calibration Range		GAIN = selected PGA gain (1 to 128) (Note 10)		-1.05 x V_{REF} / GAIN		1.05 x V_{REF} / GAIN	V
Input Span		GAIN = selected PGA gain (1 to 128) (Notes 10, 11)		0.8 x V_{REF} / GAIN		2.1 x V_{REF} / GAIN	V
POWER REQUIREMENTS							
Power-Supply Voltage	V_{DD}			2.7		3.6	V
Power-Supply Current (Note 12)	I_{DD}	Unbuffered, f_{CLKIN} = 1MHz, gain = 1 to 128				0.40	mA
		Buffered, f_{CLKIN} = 1MHz, gain = 1 to 128				0.725	
		Unbuffered, f_{CLKIN} = 2.4576MHz	Gain = 1 to 4			0.55	
			Gain = 8 to 128			0.55	
		Buffered, f_{CLKIN} = 2.4576MHz	Gain = 1 to 4			0.825	
			Gain = 8 to 128			1.0	
		Power-down mode (Note 13)				8	µA
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 3.6V			(Note 14)		dB
EXTERNAL-CLOCK TIMING SPECIFICATIONS							
CLKIN Frequency	f_{CLKIN}	(Note 15)		400		2500	kHz
Duty Cycle				40		60	%
INTERNAL-CLOCK TIMING SPECIFICATIONS							
Internal-Clock Frequency	f_{CLK}	MAX1415AE__, f_{CLK} = 1MHz (CLK = 0) or 2.4576MHz (CLK = 1)	T_A = -40°C to +85°C			±4	%
		MAX1415C__, f_{CLK} = 1MHz (CLK = 0) or 2.4576MHz (CLK = 1)	T_A = 0°C to +70°C			±4	
		MAX1415E__, f_{CLK} = 1MHz (CLK = 0) or 2.4576MHz (CLK = 1)	T_A = -40°C to 0°C			±7	
			T_A = 0°C to +85°C			±4	

Electrical Characteristics—MAX1415 (continued)

(V_{DD} = 3V, V_{GND} = 0V, V_{REF+} = 1.225V, V_{REF-} = GND, external f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Typical Conversion-Time Variation	Δt_{CONV}	t_{CONV} = 1/ODR		±0.5		%

Timing Characteristics—MAX1415

(Note 16) (Figures 8, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{DRDY}$ High Time			500/ f_{CLKIN}			s
Reset Pulse-Width Low			100			ns
$\overline{DRDY}$ Fall to $\overline{CS}$ Fall Setup Time	t_1		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_2		120			ns
SCLK Fall to DOUT Valid Delay	t_3		0		100	ns
SCLK Pulse-Width High	t_4		100			ns
SCLK Pulse-Width Low	t_5		100			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_6		0			ns
Bus Relinquish Time After SCLK Rising Edge	t_7				100	ns
SCLK Fall to $\overline{DRDY}$ Rise Delay	t_8				100	ns
DIN to SCLK Setup Time	t_9		30			ns
DIN to SCLK Hold Time	t_{10}		20			ns

Electrical Characteristics—MAX1416

(V_{DD} = 5V, V_{GND} = 0V, V_{REF+} = 2.5V, V_{REF-} = GND, f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution (No Missing Codes)			16			Bits
Output Noise				(Tables 1, 3)		µV
Integral Nonlinearity	INL	Gain = 1, bipolar mode, unbuffered			±0.0015	%FSR
Unipolar Offset Error		After calibration		(Note 1)		µV
Unipolar Offset Drift		(Note 2)		0.5		µV/°C
Bipolar Zero Error		After calibration		(Note 1)		µV
Bipolar Zero Drift (Note 2)		Gain = 1 to 4		0.5		µV/°C
		Gain = 8 to 128		0.1		

Electrical Characteristics—MAX1416 (continued)

(V_{DD} = 5V, V_{GND} = 0V, V_{REF+} = 2.5V, V_{REF-} = GND, f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Full-Scale Error		After calibration		(Notes 1, 3)		µV
Full-Scale Drift		(Notes 2, 4)		0.5		µV/°C
Gain Error		After calibration		(Notes 1, 5)		µV
Gain Drift		(Notes 2, 6)		0.5		ppm of FSR/°C
Bipolar Negative Full-Scale Error		After calibration		±0.003		%FSR
Bipolar Negative Full-Scale Drift (Note 2)		Gain = 1 to 4		1		µV/°C
		Gain = 8 to 128		0.6		
ANALOG INPUTS (AIN1+, AIN1-, AIN2+, AIN2-)						
AIN Differential Input Voltage Range (Note 7)		Unipolar input range	0		V_{REF} / GAIN	V
		Bipolar input range	-V_{REF} / GAIN		V_{REF} / GAIN	
AIN Absolute Input Voltage Range (Note 8)		Unbuffered	GND - 30mV		V_{DD} + 30mV	V
		Buffered	GND + 50mV		V_{DD} - 1.5V	
AIN DC Leakage Current		Unselected input channel			1	nA
AIN Input Capacitance		Gain = 1		34		pF
		Gain = 2		38		
		Gain = 4		45		
		Gain = 8 to 128		60		
AIN Input Sampling Rate	f_S	Gain = 1 to 128			f_{CLKIN} / 64	MHz
Input Common-Mode Rejection	CMR	Gain = 1		96		dB
		Gain = 2		105		
		Gain = 4		110		
		Gain = 8 to 128		130		
Normal-Mode 50Hz Rejection		For filter notches of 25Hz, 50Hz, ±0.02 x f_{NOTCH}		98		dB
Normal-Mode 60Hz Rejection		For filter notches of 20Hz, 60Hz, ±0.02 x f_{NOTCH}		98		dB
Common-Mode 50Hz Rejection		For filter notches of 25Hz, 50Hz, ±0.02 x f_{NOTCH}		150		dB
Common-Mode 60Hz Rejection		For filter notches of 20Hz, 60Hz, ±0.02 x f_{NOTCH}		150		dB

Electrical Characteristics—MAX1416 (continued)

(V_{DD} = 5V, V_{GND} = 0V, V_{REF+} = 2.5V, V_{REF-} = GND, f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE (REF+, REF-)						
REF Differential Input Range	V_{REF}	(Note 9)	1		3.5	V
REF Absolute Input Voltage Range			GND		V_{DD}	V
REF Input Capacitance		Gain = 1 to 128		10		pF
REF Input Sampling Rate	f_s				f_{CLKIN} / 64	MHz
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{RESET}$)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYST}	DIN, $\overline{CS}$, $\overline{RESET}$		250		mV
		SCLK		500		
Input Current	I_{IN}				±1	µA
Input Capacitance				5		pF
CLKIN INPUT						
CLKIN Input High Voltage	V_{CLKINH}		3.5			V
CLKIN Input Low Voltage	V_{CLKINL}				0.8	V
CLKIN Input Current	I_{CLKIN}				±10	µA
DIGITAL OUTPUTS (DOUT, $\overline{DRDY}$, CLKOUT)						
Output-Voltage Low	V_{OL}	DOUT and $\overline{DRDY}$, I_{SINK} = 800µA			0.4	V
		CLKOUT, I_{SINK} = 10µA			0.4	
Output-Voltage High	V_{OH}	DOUT and $\overline{DRDY}$, I_{SOURCE} = 200µA	4.0			V
		CLKOUT, I_{SOURCE} = 10µA	4.0			
Tri-State Leakage Current	I_L	DOUT only			±10	µA
Tri-State Output Capacitance	C_{OUT}	DOUT only		9		pF
SYSTEM CALIBRATION						
Full-Scale Calibration Range		GAIN = selected PGA gain (1 to 128) (Note 10)	-1.05 x V_{REF} / GAIN		+1.05 x V_{REF} / GAIN	V
Offset Calibration Range		GAIN = selected PGA gain (1 to 128) (Note 10)	-1.05 x V_{REF} / GAIN		+1.05 x V_{REF} / GAIN	V
Input Span		GAIN = selected PGA gain (1 to 128) (Notes 10, 11)	0.8 x V_{REF} / GAIN		2.1 x V_{REF} / GAIN	V
POWER REQUIREMENTS						
Power-Supply Voltage	V_{DD}		4.75		5.25	V

Electrical Characteristics—MAX1416 (continued)

(V_{DD} = 5V, V_{GND} = 0V, V_{REF+} = 2.5V, V_{REF-} = GND, f_{CLKIN} = 2.4576MHz, CLKDIV bit = 0, C_{REF+} to GND = 0.1µF, C_{REF-} to GND = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Current (Note 12)	I_{DD}	Unbuffered, f_{CLKIN} = 1MHz, gain = 1 to 128				0.45	mA
		Buffered, f_{CLKIN} = 1MHz, gain = 1 to 128				0.78	
		Unbuffered, f_{CLKIN} = 2.4576MHz	Gain = 1 to 4			0.6	
			Gain = 8 to 128			0.6	
		Buffered, f_{CLKIN} = 2.4576MHz	Gain = 1 to 4			0.95	
			Gain = 8 to 128			1.1	
		Power-down mode (Note 13)				16	µA
Power-Supply Rejection Ratio	PSRR	V_{DD} = 4.75V to 5.25V			(Note 14)		dB
EXTERNAL-CLOCK SPECIFICATIONS							
CLKIN Frequency	f_{CLKIN}	(Note 15)		400		2500	kHz
Duty Cycle				40		60	%
INTERNAL-CLOCK TIMING SPECIFICATIONS							
Internal-Clock Frequency	f_{CLK}	MAX1416AE__, f_{CLK} = 1MHz (CLK = 0) or 2.4576MHz (CLK = 1)	T_A = -40°C to +85°C			±4	%
		MAX1416C__, f_{CLK} = 1MHz (CLK = 0) or 2.4576MHz (CLK = 1)	T_A = 0°C to +70°C			±4	
		MAX1416E__, f_{CLK} = 1MHz (CLK = 0) or 2.4576MHz (CLK = 1)	T_A = -40°C to 0°C			±7	
			T_A = 0°C to +85°C			±4	
Typical Conversion-Time Variation	Δt_{CONV}	t_{CONV} = 1/ODR, CLK = 0 (1MHz), INTCLK = 1			±0.5		%

Timing Characteristics—MAX1416

(Note 16) (Figures 8, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{DRDY}$ High Time			500 / f_{CLKIN}			s
Reset Pulse-Width Low			100			ns
$\overline{DRDY}$ Fall to $\overline{CS}$ Fall Setup Time	t_1		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_2		120			ns
SCLK Fall to DOUT Valid Delay	t_3		0		80	ns
SCLK Pulse-Width High	t_4		100			ns
SCLK Pulse-Width Low	t_5		100			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_6		0			ns
Bus Relinquish Time After SCLK Rising Edge	t_7				60	ns

Timing Characteristics—MAX1416 (continued)

(Note 16) (Figures 8, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Fall to $\overline{DRDY}$ Rise Delay	t_8				100	ns
DIN to SCLK Setup Time	t_9		30			ns
DIN to SCLK Hold Time	t_{10}		20			ns

Note 1: These errors are in the order of the conversion noise shown in Tables 1 and 3. This applies after calibration at the given temperature.

Note 2: Recalibration at any temperature removes these drift errors.

Note 3: Positive full-scale error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges.

Note 4: Full-scale drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and applies to both unipolar and bipolar input ranges.

Note 5: Gain error does not include zero-scale errors. It is calculated as (full-scale error – unipolar offset error) for unipolar ranges, and (full-scale error – bipolar zero error) for bipolar ranges.

Note 6: Gain-error drift does not include unipolar offset drift or bipolar zero drift. Effectively, it is the drift of the part if only zero-scale calibrations are performed.

Note 7: The analog input voltage range on AIN+ is given here with respect to the voltage on AIN- on the MAX1415/MAX1416.

Note 8: This common-mode voltage range is allowed, provided that the input voltage on the analog inputs does not go more positive than (V_{DD} + 30mV) or more negative than (GND - 30mV). Parts are functional with voltages down to (GND - 200mV), but with increased leakage at high temperature.

Note 9: The REF differential voltage, V_{REF}, is the voltage on REF+ referenced to REF- ($V_{REF} = V_{REF+} - V_{REF-}$).

Note 10: Guaranteed by design.

Note 11: These calibration and span limits apply, provided that the absolute voltage on the analog inputs does not exceed (V_{DD} + 30mV) or go more negative than (GND - 30mV). The offset-calibration limit applies to both the unipolar zero point and the bipolar zero point.

Note 12: When using a crystal or ceramic resonator across the CLKIN and CLKOUT as the clock source for the device, the supply current and power dissipation varies depending on the crystal or resonator type. Supply current is measured with the digital inputs connected to 0 or V_{DD}, CLKIN connected to an external clock source, and CLKDIS = 1.

Note 13: If the external master clock continues to run in power-down mode, the power-down current typically increases to 67µA at 3V. When using a crystal or ceramic resonator across the CLKIN and CLKOUT as the clock source for the device, the clock generator continues to run in power-down mode and the power dissipation depends on the crystal or resonator type (see the *Power-Down Modes* section).

Note 14: Measured at DC and applied in the selected passband. PSRR at 50Hz exceeds 120dB with filter notches of 25Hz or 50Hz. PSRR at 60Hz exceeds 120dB with filter notches of 20Hz or 60Hz.

PSRR depends on both gain and V_{DD}.

GAIN	PSRR (V_{DD} = 5V)	PSRR (V_{DD} = 3V) (dB)
1	90	86
2	78	78
4	84	85
8 to 128	91	93

Note 15: Provide f_{CLKIN} whenever the MAX1415/MAX1416 are not in power-down mode. If no clock is present, the device can draw higher-than-specified current and can possibly become uncalibrated.

Note 16: All input signals are specified with $t_r = t_f$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6V.

Table 1. MAX1415—Output RMS Noise vs. Gain and Output Data Rate (3V)

FILTER FIRST NOTCH AND OUTPUT DATA RATE (Hz)	-3dB FREQUENCY (Hz)	TYPICAL OUTPUT RMS NOISE (µV)							
		GAIN							
		1	2	4	8	16	32	64	128
BUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	2.85	1.63	2.16	0.70	0.67	0.63	0.64	0.62
25	6.55	3.46	1.92	1.13	6.05	0.75	0.73	0.70	0.70
100	26.2	48.94	26.98	11.99	0.85	3.44	2.27	1.66	1.72
200	52.4	270.91	161.33	66.19	32.64	16.89	8.34	4.98	4.86
UNBUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	3.09	1.70	1.05	0.72	0.66	0.64	0.60	0.60
25	6.55	3.58	1.94	1.23	0.80	0.77	0.73	0.70	0.70
100	26.2	51.92	24.54	11.47	6.14	3.26	2.16	1.67	1.64
200	52.4	263.86	136.78	65.40	34.51	16.64	8.97	4.96	4.80
BUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	3.03	1.97	1.34	1.01	0.95	0.93	0.96	0.95
60	15.72	3.62	2.14	1.52	1.05	0.98	1.03	1.04	1.00
250	65.5	51.02	25.44	12.95	6.19	3.84	2.70	2.35	2.23
500	131	280.58	138.29	70.21	34.60	18.44	9.45	5.40	5.34
UNBUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	3.76	1.63	0.96	0.69	0.66	0.64	0.59	0.61
60	15.72	3.11	1.86	1.12	0.78	0.75	0.71	0.71	0.69
250	65.5	48.28	25.13	12.75	6.18	3.32	2.12	1.59	1.62
500	131	280.67	143.15	75.84	34.70	17.88	9.19	4.90	4.98

Table 2. MAX1415—Peak-to-Peak Resolution vs. Gain and Output Data Rate

FILTER FIRST NOTCH AND OUTPUT DATA RATE (Hz)	-3dB FREQUENCY (Hz)	TYPICAL PEAK-TO-PEAK RESOLUTION (BITS)							
		GAIN							
		1	2	4	8	16	32	64	128
BUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	16	16	16	16	15	14	13	12
25	6.55	16	16	16	12	15	14	13	12
100	26.2	12	12	12	16	12	12	11	11
200	52.4	10	10	10	10	10	10	10	9
UNBUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	16	16	16	16	15	14	13	12
25	6.55	16	16	16	16	15	14	13	12
100	26.2	12	12	12	12	12	12	12	11
200	52.4	10	10	10	10	10	10	10	9
BUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	16	16	16	15	15	14	13	12
60	15.72	16	16	16	15	14	13	12	11
250	65.5	12	12	12	12	12	12	11	10
500	131	10	10	10	10	10	10	10	9
UNBUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	16	16	16	16	15	14	13	12
60	15.72	16	16	16	16	15	14	13	12
250	65.5	12	12	12	12	12	12	12	11
500	131	10	10	10	10	10	10	10	9

Table 3. MAX1416—Output RMS Noise vs. Gain and Output Data Rate (5V)

FILTER FIRST NOTCH AND OUTPUT DATA RATE (Hz)	-3dB FREQUENCY (Hz)	TYPICAL OUTPUT RMS NOISE (µV)							
		GAIN							
		1	2	4	8	16	32	64	128
BUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	3.51	1.87	1.11	0.75	0.70	0.71	0.67	0.65
25	6.55	4.46	2.39	1.32	0.90	0.83	0.81	0.75	0.74
100	26.2	92.29	47.60	28.62	11.60	6.40	3.70	2.34	2.30
200	52.4	552.57	295.67	105.50	69.01	35.15	17.37	9.04	9.05
UNBUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	3.88	1.92	1.17	0.76	0.72	0.70	0.65	0.65
25	6.55	5.00	2.60	1.41	0.87	0.83	0.81	0.73	0.74
100	26.2	98.13	48.60	24.35	11.89	6.00	3.66	2.51	2.46
200	52.4	551.95	275.15	134.65	69.82	33.34	16.77	9.04	9.36
BUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	4.10	2.56	1.68	1.23	1.19	1.21	1.15	1.19
60	15.72	4.52	2.96	1.89	1.32	1.32	1.27	1.28	1.31
250	65.5	96.62	47.35	26.33	12.42	7.10	4.30	3.16	3.19
500	131	568.80	292.49	151.10	71.96	36.61	19.18	9.95	10.23
UNBUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	3.21	1.84	1.14	0.76	0.73	0.72	0.64	0.65
60	15.72	3.93	2.21	1.37	0.87	0.81	0.77	0.74	0.73
250	65.5	99.77	52.91	26.56	12.31	5.95	3.50	2.37	2.38
500	131	520.55	302.42	136.54	68.66	36.94	18.64	9.34	9.49

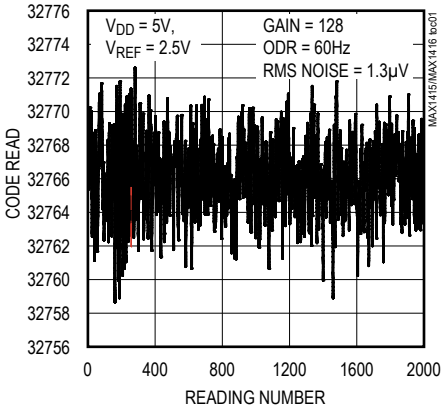
Table 4. MAX1416—Peak-to-Peak Resolution vs. Gain and Output Data Rate

FILTER FIRST NOTCH AND OUTPUT DATA RATE (Hz)	-3dB FREQUENCY (Hz)	TYPICAL PEAK-TO-PEAK RESOLUTION (BITS)							
		GAIN							
		1	2	4	8	16	32	64	128
BUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	16	16	16	16	16	15	14	13
25	6.55	16	16	16	16	16	15	14	13
100	26.2	12	12	12	12	12	12	12	11
200	52.4	10	10	11	10	10	10	10	9
UNBUFFERED (f_{CLKIN} = 1MHz)									
20	5.24	16	16	16	16	16	15	14	13
25	6.55	16	16	16	16	16	15	14	13
100	26.2	12	12	12	12	12	12	12	11
200	52.4	10	10	10	10	10	10	10	9
BUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	16	16	16	16	15	14	13	12
60	15.72	16	16	16	16	15	14	13	12
250	65.5	12	12	12	12	12	12	12	10
500	131	10	10	10	10	10	10	10	9
UNBUFFERED (f_{CLKIN} = 2.4576MHz)									
50	13.1	16	16	16	16	16	15	14	13
60	15.72	16	16	16	16	16	15	14	13
250	65.5	12	12	12	12	12	12	12	11
500	131	10	10	10	10	10	10	10	9

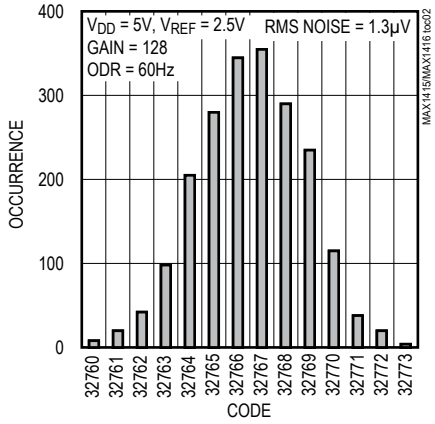
Typical Operating Characteristics

(MAX1415: V_{DD} = 5V, V_{REF+} = 2.5V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.) (MAX1416: V_{DD} = 3V, V_{REF+} = 1.225V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.)

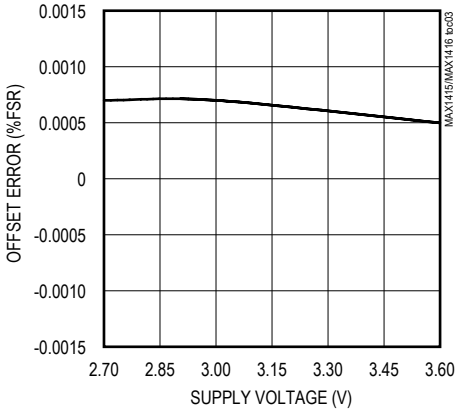
TYPICAL OUTPUT NOISE (MAX1416, BUFFERED MODE)



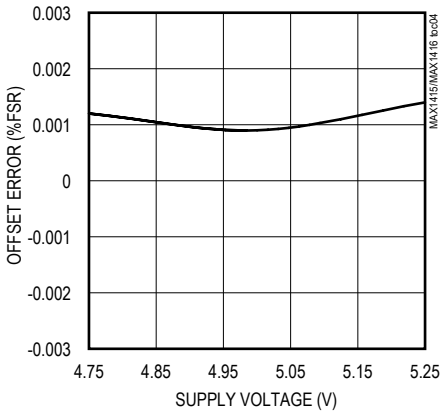
HISTOGRAM OF TYPICAL OUTPUT NOISE (MAX1416, BUFFERED MODE)



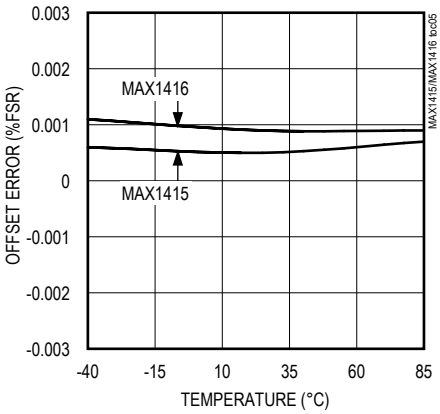
OFFSET ERROR vs. SUPPLY VOLTAGE (MAX1415)



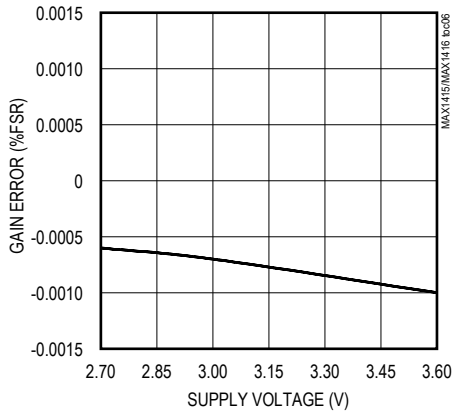
OFFSET ERROR vs. SUPPLY VOLTAGE (MAX1416)



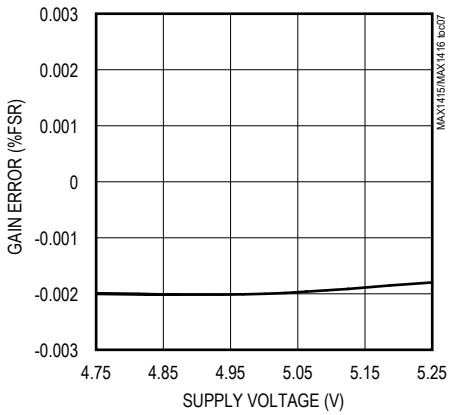
OFFSET ERROR vs. TEMPERATURE



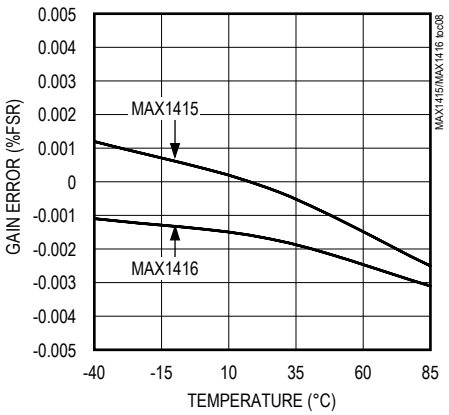
GAIN ERROR vs. SUPPLY VOLTAGE (MAX1415)



GAIN ERROR vs. SUPPLY VOLTAGE (MAX1416)



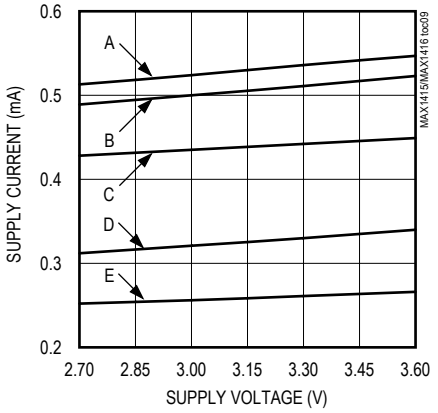
GAIN ERROR vs. TEMPERATURE



Typical Operating Characteristics (continued)

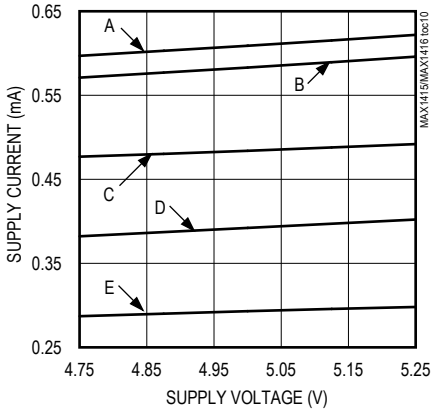
(MAX1415: V_{DD} = 5V, V_{REF+} = 2.5V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.) (MAX1416: V_{DD} = 3V, V_{REF+} = 1.225V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1415)



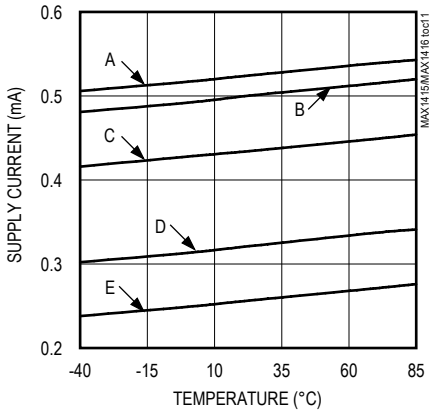
A: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 8 TO 128
B: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 4
C: BUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128
D: UNBUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 128
E: UNBUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128

SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1416)



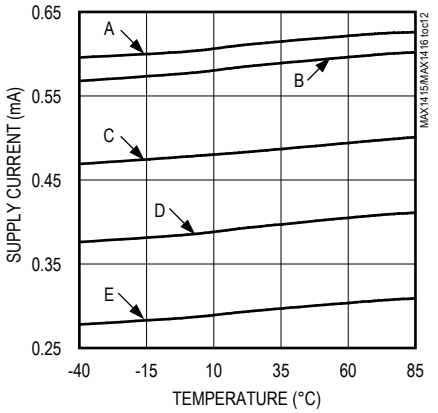
A: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 8 TO 128
B: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 4
C: BUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128
D: UNBUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 128
E: UNBUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128

SUPPLY CURRENT vs. TEMPERATURE (MAX1415)



A: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 8 TO 128
B: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 4
C: BUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128
D: UNBUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 128
E: UNBUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128

SUPPLY CURRENT vs. TEMPERATURE (MAX1416)

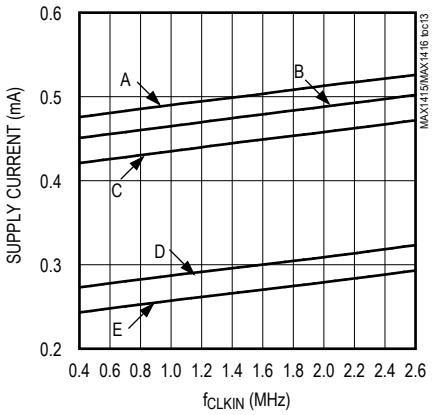


A: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 8 TO 128
B: BUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 4
C: BUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128
D: UNBUFFERED MODE f_{CLKIN} = 2.4576MHz, GAIN = 1 TO 128
E: UNBUFFERED MODE f_{CLKIN} = 1MHz, GAIN = 1 TO 128

Typical Operating Characteristics (continued)

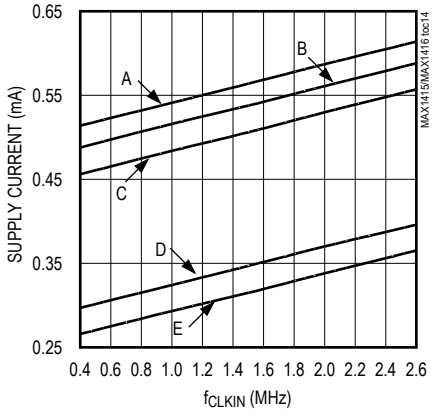
(MAX1415: V_{DD} = 5V, V_{REF+} = 2.5V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.) (MAX1416: V_{DD} = 3V, V_{REF+} = 1.225V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. f_{CLKIN} (MAX1415)



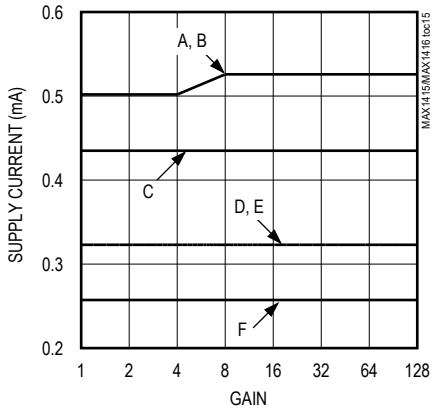
A: BUFFERED MODE CLK = 1, GAIN = 128
B: BUFFERED MODE CLK = 1, GAIN = 1
C: BUFFERED MODE CLK = 0, GAIN = 1, 128
D: UNBUFFERED MODE CLK = 1, GAIN = 1, 128
E: UNBUFFERED MODE CLK = 0, GAIN = 1, 128

SUPPLY CURRENT vs. f_{CLKIN} (MAX1416)



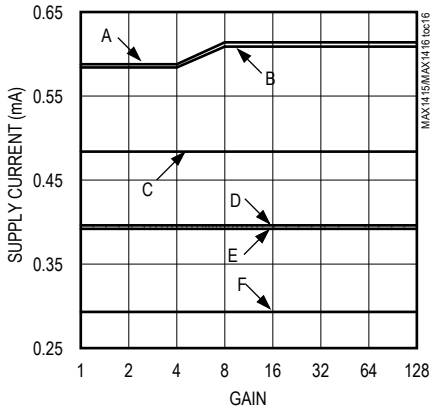
A: BUFFERED MODE CLK = 1, GAIN = 128
B: BUFFERED MODE CLK = 1, GAIN = 1
C: BUFFERED MODE CLK = 0, GAIN = 1, 128
D: UNBUFFERED MODE CLK = 1, GAIN = 1, 128
E: UNBUFFERED MODE CLK = 0, GAIN = 1, 128

SUPPLY CURRENT vs. GAIN (MAX1415)



A: BUFFERED MODE CLK = 1, CLKDIV = 1, f_{CLKIN} = 4.9152MHz
B: BUFFERED MODE CLK = 1, CLKDIV = 0, f_{CLKIN} = 2.4576MHz
C: BUFFERED MODE CLK = 0, CLKDIV = 0, f_{CLKIN} = 1MHz
D: UNBUFFERED MODE CLK = 1, CLKDIV = 1, f_{CLKIN} = 4.9152MHz
E: UNBUFFERED MODE CLK = 1, CLKDIV = 0, f_{CLKIN} = 2.4576MHz
F: UNBUFFERED MODE CLK = 0, CLKDIV = 0, f_{CLKIN} = 1MHz

SUPPLY CURRENT vs. GAIN (MAX1416)

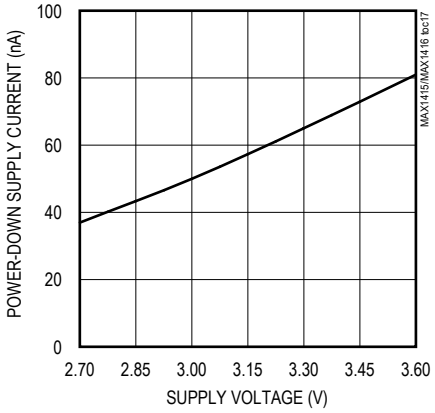


A: BUFFERED MODE CLK = 1, CLKDIV = 1, f_{CLKIN} = 4.9152MHz
B: BUFFERED MODE CLK = 1, CLKDIV = 0, f_{CLKIN} = 2.4576MHz
C: BUFFERED MODE CLK = 0, CLKDIV = 0, f_{CLKIN} = 1MHz
D: UNBUFFERED MODE CLK = 1, CLKDIV = 1, f_{CLKIN} = 4.9152MHz
E: UNBUFFERED MODE CLK = 1, CLKDIV = 0, f_{CLKIN} = 2.4576MHz
F: UNBUFFERED MODE CLK = 0, CLKDIV = 0, f_{CLKIN} = 1MHz

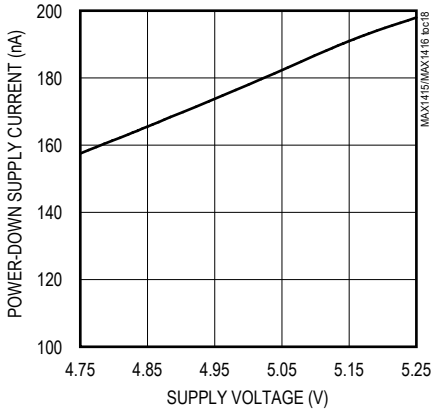
Typical Operating Characteristics (continued)

(MAX1415: V_{DD} = 5V, V_{REF+} = 2.5V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.) (MAX1416: V_{DD} = 3V, V_{REF+} = 1.225V, V_{REF-} = GND, T_A = +25°C, unless otherwise noted.)

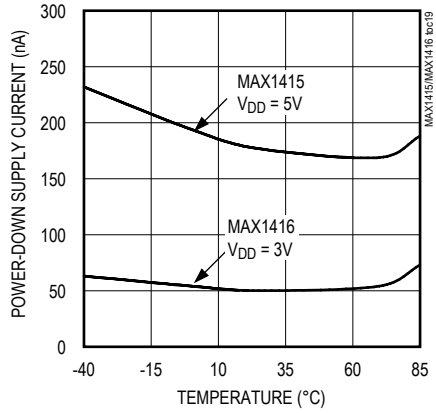
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1415)



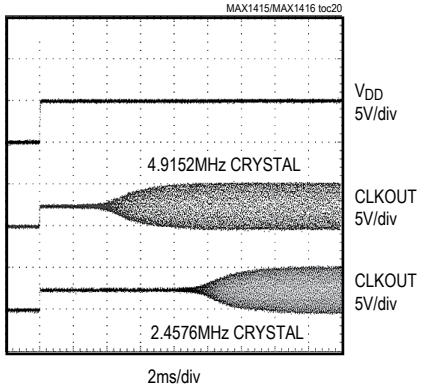
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX1416)



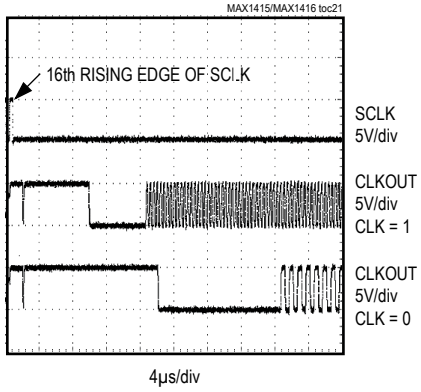
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



EXTERNAL OSCILLATOR STARTUP TIME



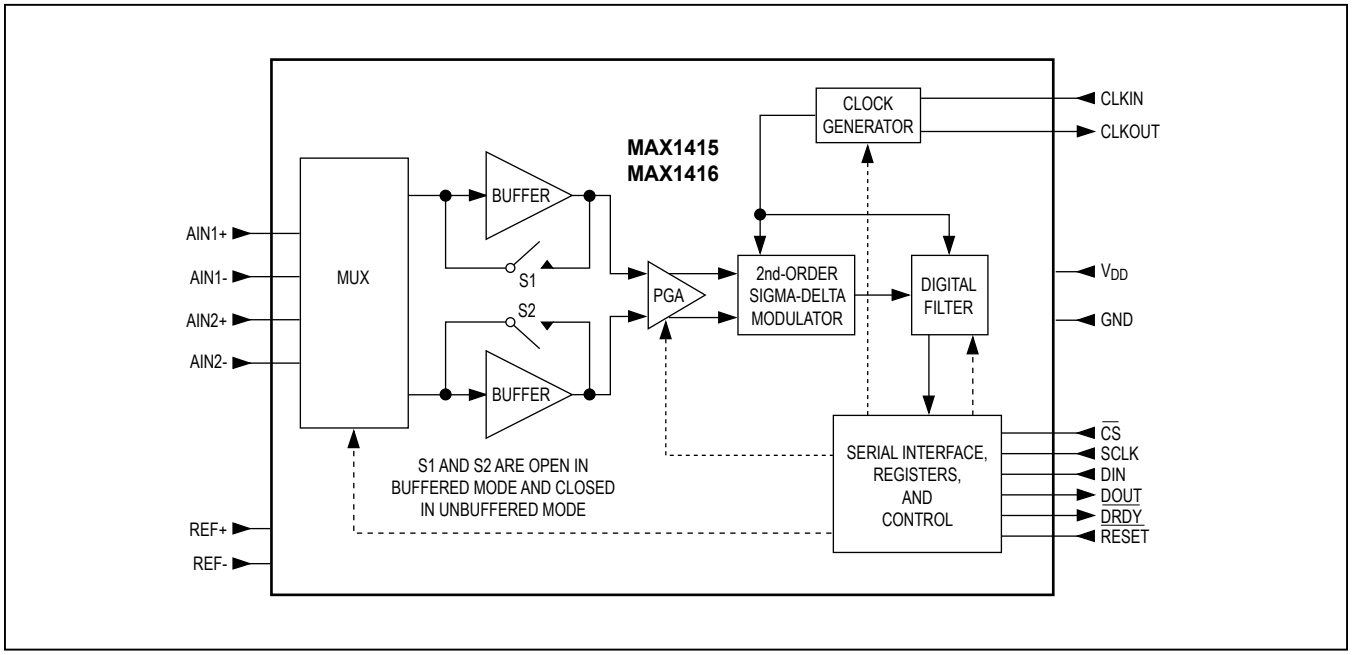
INTERNAL OSCILLATOR STARTUP TIME



Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial Clock Input. Apply an external serial clock to transfer data to and from the device at data rates up to 5MHz.
2	CLKIN	Clock Input. Connect a crystal/resonator between CLKIN and CLKOUT, or drive CLKIN externally with a CMOS-compatible clock source. Connect CLKIN to GND when using the internal oscillator.
3	CLKOUT	Clock Output. Connect a crystal/resonator between CLKIN and CLKOUT. When enabled, CLKOUT provides a CMOS-compatible, inverted clock output. CLKOUT can drive one CMOS load. Set CLKDIS = 0 in the clock register to enable CLKOUT. Set CLKDIS = 1 in the clock register to disable CLKOUT.
4	$\overline{CS}$	Active-Low Chip-Select Input. $\overline{CS}$ selects the active device in systems with more than one device on the serial bus. Drive $\overline{CS}$ low to clock data in on DIN and to clock data out on DOUT. When $\overline{CS}$ is high, DOUT is high impedance. Connect $\overline{CS}$ to GND for 3-wire operation.
5	$\overline{RESET}$	Active-Low Reset Input. Drive $\overline{RESET}$ low to reset the MAX1415/MAX1416 to power-on reset status.
6	AIN2+	Channel 2 Positive Analog Input
7	AIN1+	Channel 1 Positive Analog Input
8	AIN1-	Channel 1 Negative Analog Input
9	REF+	Positive Reference Input
10	REF-	Negative Reference Input
11	AIN2-	Channel 2 Negative Analog Input
12	$\overline{DRDY}$	Active-Low Data Ready Output. $\overline{DRDY}$ goes low when a new conversion result is available in the data register. When a read operation of a full output word completes, $\overline{DRDY}$ returns high.
13	DOUT	Serial Data Output. DOUT outputs serial data from the data register. DOUT changes on the falling edge of SCLK and is valid on the rising edge of SCLK. When $\overline{CS}$ is high, DOUT is high impedance.
14	DIN	Serial Data Input. Data on DIN is clocked in on the rising edge of SCLK when $\overline{CS}$ is low.
15	V_{DD}	Power Input. Connect V_{DD} to a 2.7V to 3.6V power supply for the MAX1415, and connect V_{DD} to a 4.75V to 5.25V power supply for the MAX1416.
16	GND	Ground

Functional Diagram



Detailed Description

The MAX1415/MAX1416 low-power, 2-channel serial output ADCs use a sigma-delta modulator with a digital filter to achieve 16-bit resolution with no missing codes. Each device includes a PGA, an on-chip input buffer, an internal oscillator, and a bidirectional communications port. The MAX1415 operates with a 2.7V to 3.6V single supply, and the MAX1416 operates with a 4.75V to 5.25V single supply.

Fully differential inputs, an internal input buffer, and an on-chip PGA (gain = 1 to 128) allow low-level signals to be directly measured, minimizing the requirements for external signal conditioning. Self-calibration corrects for gain and offset errors. A programmable digital filter allows for the selection of the output data rate and first notch frequency from 20Hz to 500Hz.

The bidirectional serial SPI-/QSPI-/MICROWIRE-compatible interface consists of four digital control lines (SCLK, $\overline{CS}$, DOUT, and DIN) and provides an easy interface to microcontrollers (µCs). Connect $\overline{CS}$ to GND to configure the MAX1415/MAX1416 for 3-wire operation.

Analog Inputs

The MAX1415/MAX1416 accept four analog inputs (AIN1+, AIN1-, AIN2+, and AIN2-) in buffered or unbuffered mode. Use Table 8 to select the positive and negative input pair for a fully differential channel. The input buffer isolates the inputs from the capacitive load presented by the PGA/modulator, allowing for high source-impedance analog transducers. The value of the BUF bit in the setup register (see the *Setup Register* section) determines whether the input buffer is enabled or disabled.

Internal protection diodes, which clamp the analog input to V_{DD} and/or GND, allow the input to swing from (GND - 0.3V) to (V_{DD} + 0.3V), without damaging the device. If the analog input exceeds 300mV beyond the supplies, limit the input current to 10mA.

Input Buffers

When the analog input buffer is disabled, the analog input drives a typical 7pF (gain = 1) capacitor, C_{TOTAL}, in series with the 7kΩ typical on-resistance of the track and hold (T/H) switch (Figure 1). C_{TOTAL} is comprised of the sampling capacitor, C_{SAMP}, and the stray capacitance, C_{STRAY}. During the conversion, C_{SAMP} charges to (AIN+ - AIN-). The gain determines the value of C_{SAMP} (see Table 5).

To minimize gain errors in unbuffered mode, select a source impedance less than the maximum values shown in Figures 2 and 3. These are the maximum external resistance/capacitance combinations allowed before gain errors greater than 1 LSB are introduced in unbuffered mode.

Enable the internal input buffer for a high source impedance. This isolates the inputs from the sampling capacitor and reduces the sampling-related gain error. When using the internal buffer, limit the absolute input voltage range to (V_{GND} + 50mV) to (V_{DD} - 1.5V). Properly set up the gain and common-mode voltage range to minimize linearity errors.

Input Voltage Range

In unbuffered mode, the absolute analog input voltage range is from (GND - 30mV) to (V_{DD} + 30mV) (see the *Electrical Characteristics* section). In buffered mode, the analog input voltage range is reduced to (GND + 50mV) to (V_{DD} - 1.5V). In both buffered and unbuffered modes, the differential analog input range (V_{AIN+} - V_{AIN-}) decreases at higher gains (see the *Programmable Gain Amplifier* and *Unipolar and Bipolar Modes* sections).

Reference

The MAX1415/MAX1416 provide differential inputs, REF+ and REF-, for an external reference voltage. Connect the external reference directly across REF+ and REF- to obtain the differential reference voltage, V_{REF}. The common-mode voltage range for V_{REF+} and V_{REF-} is between GND and V_{DD}. For specified operation, the nominal voltage, V_{REF} is 1.225V for the MAX1415 and 2.5V for the MAX1416.

The MAX1415/MAX1416 sample REF+ and REF- at f_{CLKIN}/64 (CLKDIV = 0) or f_{CLKIN}/128 (CLKDIV = 1) with an internal 10pF (typ for gain = 1) sampling capacitor in series with a 7kΩ (typ) switch on-resistance.

Programmable Gain Amplifier

A PGA provides selectable levels of gain: 1, 2, 4, 8, 16, 32, 64, and 128. Bits G0, G1, and G2 in the setup register control the gain (see Table 9). As the gain increases, the value of the input sampling capacitor, C_{SAMP}, also increases (see Table 5). The dynamic load presented to the analog inputs increases with clock frequency and gain in unbuffered mode (see the *Input Buffers* section and Figure 1).

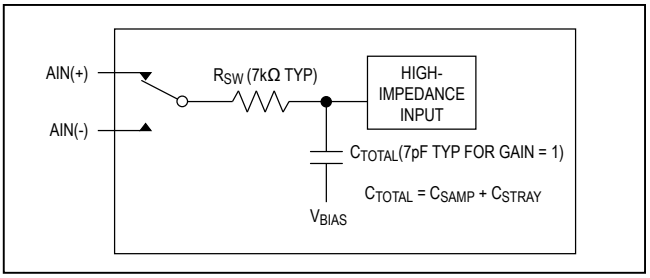


Figure 1. Unbuffered Analog Input Structure

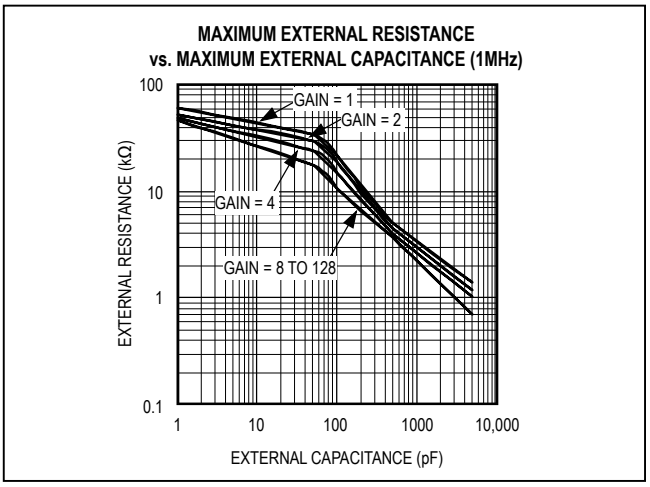


Figure 2. Maximum External Resistance vs. Maximum External Capacitance for Unbuffered Mode (1MHz)

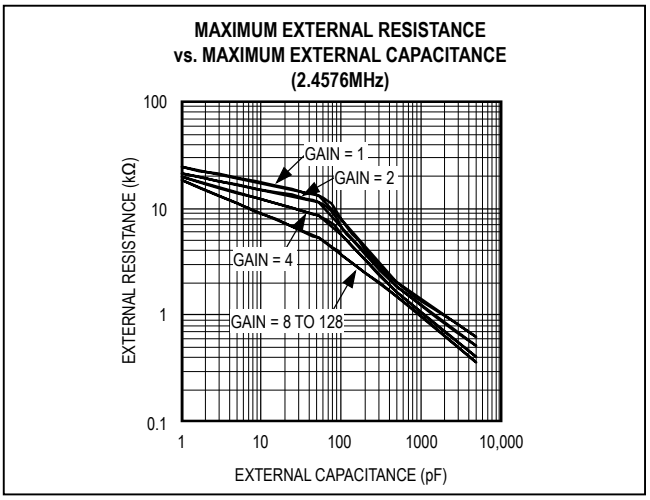


Figure 3. Maximum External Resistance vs. Maximum External Capacitance for Unbuffered Mode (2.4576MHz)

Table 5. Input Sampling Capacitor

GAIN	INPUT SAMPLING CAPACITOR (C_{SAMP}) (pF)
1	3.75
2	7.5
4	15
8–128	30

Increasing the gain increases the resolution of the ADC (LSB size decreases), but reduces the differential input voltage range. Calculate 1 LSB in unipolar mode using the following equation:

$$1\ LSB = \frac{V_{REF}}{GAIN\ (\ 65,536\ )}$$

where: $V_{REF} = V_{REF+} - V_{REF-}$.

For a gain of 1 and V_{REF} = 2.5V, the full-scale voltage in unipolar mode is 2.5V and 1 LSB ≈ 38.1µV. For a gain of 4, the full-scale voltage in unipolar mode is 0.625V (V_{REF}/GAIN) and 1 LSB ≈ 9.5µV. The differential input voltage range in this example reduces from 2.5V to 0.625V, and the resolution increases since the LSB size decreases from 38.1µV to 9.5µV.

Calculate 1 LSB in bipolar mode using the following equation:

$$1\ LSB = \frac{V_{REF}}{GAIN\ (\ 65,536\ )} \times 2$$

where: $V_{REF} = V_{REF+} - V_{REF-}$.

Unipolar and Bipolar Modes

The $\overline{B}$/U bit in the setup register (Table 9) configures the MAX1415/MAX1416 for unipolar or bipolar transfer functions. Figures 4 and 5 illustrate the unipolar and bipolar transfer functions, respectively.

In unipolar mode, the digital output code is straight binary. When AIN+ = AIN-, the outputs are at zero scale, which is the lower endpoint of the transfer function. The full-scale endpoint is given by AIN+ - AIN- = V_{REF} / GAIN, where $V_{REF} = V_{REF+} - V_{REF-}$.

In bipolar mode, the digital output code is in offset binary. Positive full scale is given by AIN+ - AIN- = +V_{REF} / GAIN and negative full scale is given by AIN+ - AIN- = -V_{REF} / GAIN. When AIN+ = AIN-, the outputs are at zero scale, which is the midpoint of the bipolar transfer function.

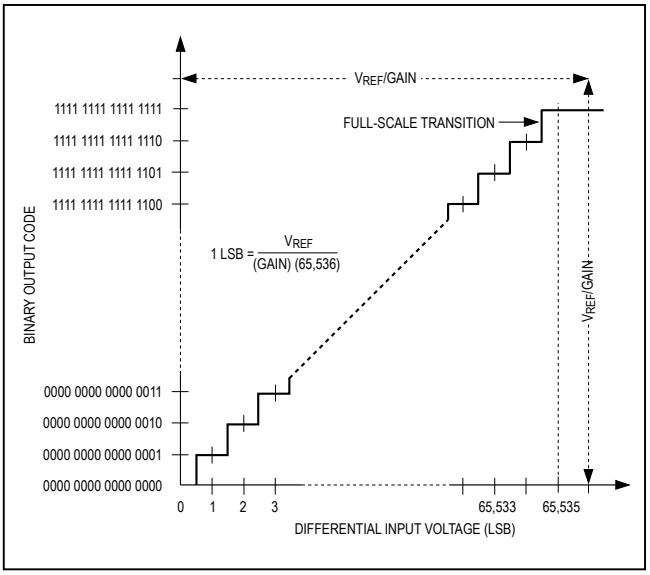


Figure 4. MAX1415/MAX1416 Unipolar Transfer Function

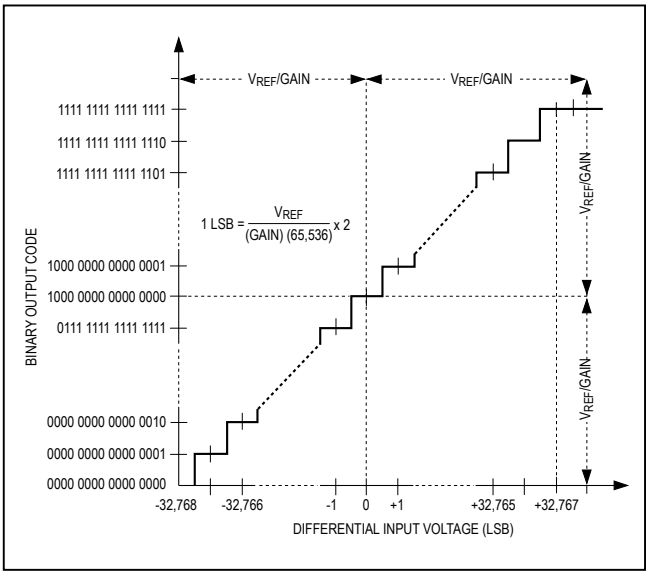


Figure 5. MAX1415/MAX1416 Bipolar Transfer Function

When the MAX1415/MAX1416 are in buffered mode, the absolute and common-mode analog input voltage ranges reduce to between (GND + 50mV) and (V_{DD} - 1.5V). The differential input voltage range is not affected in buffered mode.

Modulator

The MAX1415/MAX1416 perform analog-to-digital conversions using a single-bit, 2nd-order, switched-capacitor, sigma-delta modulator. The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. A single comparator within the modulator quantizes the input signal at a much higher sample rate than the bandwidth of the input.

The MAX1415/MAX1416 modulator provides 2nd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply and common-mode noise. A single-bit data stream is then presented to the digital filter for processing to remove the frequency-shaped quantization noise.

The modulator sampling frequency is f_{CLKIN} / 128, regardless of gain, where f_{CLKIN} (CLKDIV = 0) is the frequency of the signal at CLKIN.

Digital Filtering

The MAX1415/MAX1416 contain an on-chip, digital low-pass filter that processes the 1-bit data stream from the modulator using a $SINC^3$ $(sinx/x)^3$ response. The $SINC^3$ filter has a settling time of three output data periods.

Filter Characteristics

Figure 6 shows the filter frequency response. The SINC3 characteristic -3dB cutoff frequency is 0.262 times the first notch frequency. This results in a cutoff frequency of 15.72Hz for a first filter notch frequency of 60Hz (output data rate of 60Hz). The response shown in Figure 5 is repeated at either side of the digital filter's sample frequency, f_M (f_M = 19.2kHz for 60Hz output data rate), and at either side of the related harmonics ($2f_M$, $3f_M$, and so on).

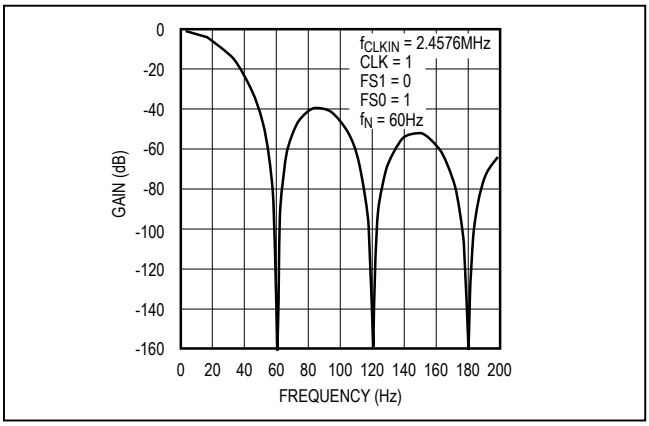


Figure 6. Frequency Response of the $SINC^3$ Filter (Notch at 60Hz)

The output data rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Therefore, for the plot in Figure 6, where the first notch of the filter is 60Hz, the output data rate is 60Hz. The notches of the $SINC^3$ filter are repeated at multiples of the first notch frequency. The $SINC^3$ filter provides an attenuation of better than 100dB at these notches.

Determine the cutoff frequency of the digital filter by loading the appropriate values into the CLK, FS0, and FS1 bits in the clock register (see Table 13). Programming a different cutoff frequency with FS0 and FS1 changes the frequency of the notches, but it does not alter the profile of the frequency response.

For step changes at the input, allow a settling time before valid data is read. The settling time depends on the output data rate chosen for the filter. The worst-case settling time of a $SINC^3$ filter for a full-scale step input is four times the output data period. By synchronizing the step input using FSYNC, the settling time reduces to three times the output data period. If FSYNC is high during the step input, the filter settles in three times the data output period after FSYNC falls low.

Analog Filtering

The digital filter does not provide any rejection close to the harmonics of the modulator sample frequency. Due to the high oversampling ratio of the MAX1415/MAX1416, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. The analog filtering requirements in front of the MAX1415/MAX1416 are reduced compared to a conventional converter with no on-chip filtering. In addition, the devices provide excellent common-mode rejection to reduce the common-mode noise susceptibility.

Additional filtering prior to the MAX1415/MAX1416 eliminates unwanted frequencies the digital filter does not reject. Use additional filtering to ensure that differential noise signals outside the frequency band of interest do not saturate the analog modulator.

If passive components are in the path of the analog inputs when the device is in unbuffered mode, ensure the source impedance is low enough (Figure 2) not to introduce gain errors in the system. This significantly limits the amount of passive anti-aliasing filtering that can be applied in front of the MAX1415/MAX1416 in unbuffered mode. In buffered mode, large source impedance causes a small DC-offset error, which can be removed by calibration.

Internal Oscillator Mode

In internal oscillator mode (INTCLK = 1), set the CLK bit in the clock register (Table 12) to 0 to operate at a clock frequency of 1MHz, or set CLK to 1 for a frequency of 2.4576MHz. The CLKDIV bit is not used in this mode.

Internal-Clock Startup Time

The internal clock requires time to stabilize during power-on reset. This startup time is dependent on the internal-clock frequency (see the T*ypical Operating Characteristics* section). The typical startup time for the internal oscillator is less than 35µs, while the external oscillator startup time when using a crystal or resonator is in the order of milliseconds.

External Oscillator

The oscillator requires time to stabilize when enabled. Startup time for the oscillator depends on supply voltage, temperature, load capacitances, and center frequency. Depending on the load capacitance, a 1MΩ feedback resistor across the crystal can reduce the startup time (Figure 7). The MAX1415/MAX1416 were tested with an ECS-24-32-1 (2.4576MHz crystal) and an ECS-49-20-1 (4.9152MHz crystal) (see the *Typical Operating Characteristics* section). When the external oscillator is enabled, the supply current is typically 67µA with a 3V supply and 227µA with a 5V supply.

Serial Digital Interface

The MAX1415/MAX1416 interface is fully compatible with SPI-, QSPI-, and MICROWIRE-standard serial interfaces. The serial interface provides access to seven on-chip registers. The registers are 8, 16, and 24 bits in size.

Drive $\overline{CS}$ low to transfer data in and out of the MAX1415/MAX1416. Clock in data at DIN on the rising edge of SCLK. Data at DOUT changes on the falling edge of SCLK and is valid on the rising edge of SCLK. DIN and DOUT are transferred MSB first. Drive $\overline{CS}$ high to force DOUT high impedance and cause the MAX1415/MAX1416 to ignore any signals on SCLK and DIN. Connect $\overline{CS}$ low for 3-wire operation. Figures 8 and 9 show the timings for write and read operations, respectively.

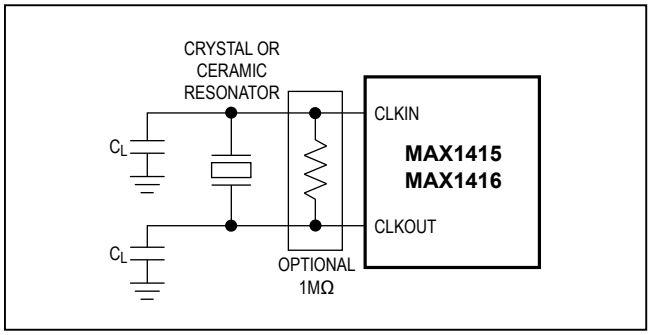


Figure 7. Using a Crystal or Ceramic Oscillator

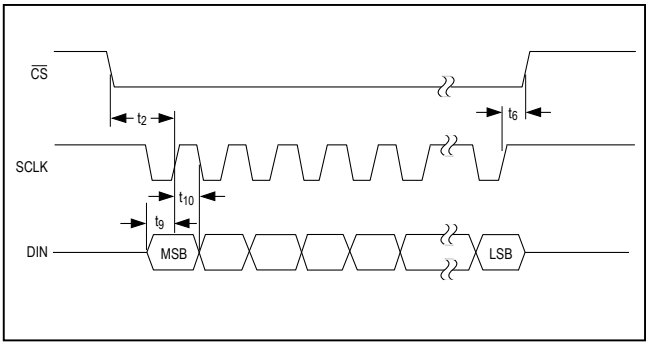


Figure 8. Write Timing Diagram

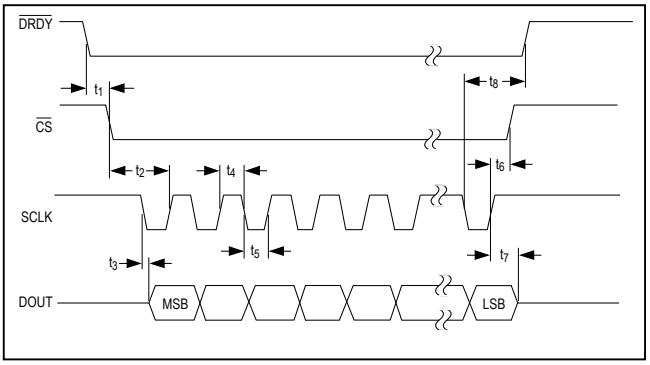


Figure 9. Read Timing Diagram

On-Chip Registers

The MAX1415/MAX1416 contain seven internal registers (Figure 10), which are accessed by the serial interface. These registers control the various functions of the device and allow the results to be read. Table 7 lists the address, power-on default value, and size of each register.

The first of these registers is the communications register. The 8-bit communications register controls the acquisition-channel selection, whether the next data transfer is a read or write operation, and which register is to be accessed. The second register is the 8-bit setup register, which controls calibration modes, gain setting, unipolar/bipolar inputs, and buffered/unbuffered modes. The third register is the 8-bit clock register, which sets the digital filter characteristics and the clock control bits. The fourth register is the 16-bit data register, which holds the output result. The 24-bit offset and gain registers store the calibration coefficients for the MAX1415/MAX1416. The 8-bit test register is used for factory testing only.

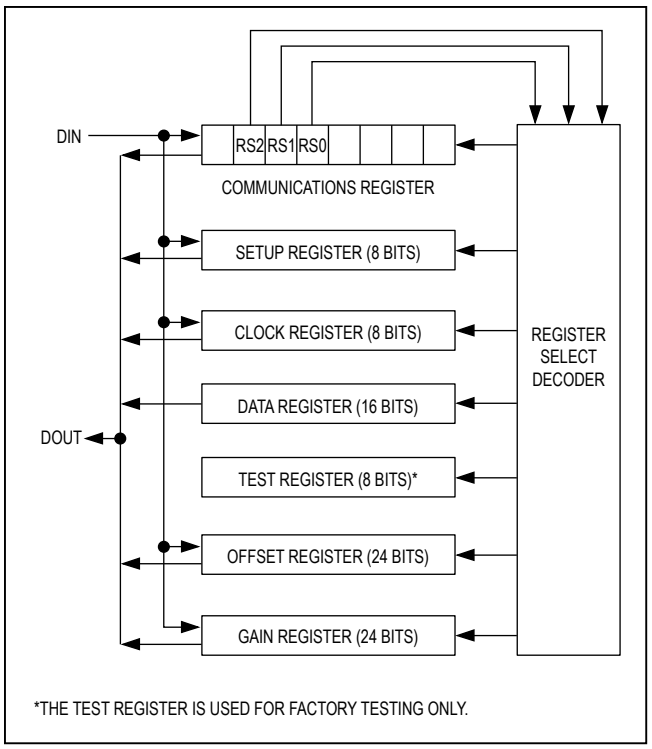


Figure 10. Register Summary

The default state of the MAX1415/MAX1416 is to wait for a write to the communications register. Any write or read operation on the MAX1415/MAX1416 is a two-step process. First, a command byte is written to the communications register. This command selects the input channel, the desired register for the next read or write operation, and whether the next operation is a read or a write. The second step is to read from or write to the selected register. At the end of the data-transfer cycle, the device returns to the default state. See the *Performing a Conversion* section for examples.

If the serial communication is lost, write 32 ones to the serial interface to return the MAX1415/MAX1416 to the default state. The registers are not reset after this operation.

Communications Register

The byte-wide communications register is bidirectional so it can be written and read. The byte written to the communications register indicates the next read or write operation on the selected register, the power-down mode, and the analog input channel (see Table 6). The $\overline{DRDY}$ bit indicates the conversion status.

0/$\overline{DRDY}$: (Default = 0) Communication-Start/Data-Ready Bit. Write a 0 to the 0/$\overline{DRDY}$ bit to start a write operation to the communications register. If 0/$\overline{DRDY}$ = 1, then the device waits until a 0 is written to 0/$\overline{DRDY}$ before continuing to load the remaining bits. For a read operation, the 0/$\overline{DRDY}$ bit shows the status of the conversion. The $\overline{DRDY}$ bit returns a 0 if the conversion is complete and the data is ready. $\overline{DRDY}$ returns a 1 if the new data has been read and the next conversion is not yet complete. It has the same value as the $\overline{DRDY}$ output pin.

RS2, RS1, RS0: (Default = 0, 0, 0) Register-Select Bits. RS2, RS1, and RS0 select the next register to be accessed as shown in Table 7.

R/$\overline{W}$: (Default = 0) Read-/Write-Select Bit. Use this bit to select if the next register access is a read or a write operation. Set R/$\overline{W}$ = 0 to select a write operation, or set R/$\overline{W}$ = 1 for a read operation on the selected register.

PD: (Default = 0) Power-Down Control Bit. Set PD = 1 to initiate power-down mode. Set PD = 0 to take the device out of power-down mode. If the internal oscillator or external crystal/resonator is used and CLKDIS = 0, CLKOUT remains active during power-down mode to provide a clock source for other devices in the system.

CH1, CH0: (Default = 0, 0) Channel-Select Bit. Write to the CH1 and CH0 bits to select the conversion channel or to access the calibration data shown in Table 8. The calibration coefficients of a particular channel are stored in one of the three offset and gain register pairs in Table 8. Set CH1 = 1 and CH0 = 0 to evaluate the noise performance of the part without external noise sources. In this noise-evaluation mode, connect AIN1- to an external voltage within the allowable common-mode range.

Setup Register

The byte-wide setup register is bidirectional so it can be written and read. The byte written to the setup register sets the calibration modes, PGA gain, unipolar/bipolar mode, buffer enable, and conversion start (see Table 9).

MD1, MD0: (Default = 0, 0) Mode-Select Bits. See Table 10 for normal operating mode, self-calibration, zero-scale calibration, or full-scale calibration-mode selection.

Table 6. Communications Register

(MSB)							(LSB)	
FUNCTION	**COMMUNICATION START/DATA READY**	**REGISTER SELECT**			**READ/WRITE SELECT**	**POWER-DOWN MODE**	**CHANNEL SELECT**	
Name	0/$\overline{DRDY}$	RS2	RS1	RS0	R/$\overline{W}$	PD	CH1	CH0
Defaults	0	0	0	0	0	0	0	0

Table 7. Register Selection

RS2	RS1	RS0	REGISTER	POWER-ON RESET STATUS	REGISTER SIZE (bits)
0	0	0	Communications register	0x00	8
0	0	1	Setup register	0x01	8
0	1	0	Clock register	0x85	8
0	1	1	Data register	N/A	16
1	0	0	Test register*	N/A	8
1	0	1	No operation	—	—
1	1	0	Offset register	0x1F 40 00	24
1	1	1	Gain register	0x57 61 AB	24

**The test register is used for factory testing only.*

Table 8. Channel Selection

CH1	CH0	AIN+	AIN-	OFFSET/GAIN REGISTER PAIR
0	0	AIN1+	AIN1-	0
0	1	AIN2+	AIN2-	1
1	0	AIN1-	AIN1-	0
1	1	AIN1-	AIN2-	2

Table 9. Setup Register

	(MSB)							(LSB)
FUNCTION	**MODE CONTROL**		**PGA GAIN CONTROL**			**BIPOLAR/UNIPOLAR MODE**	**BUFFER ENABLE**	**FSYNC**
Name	MD1	MD0	G2	G1	G0	$\overline{B}$/U	BUF	FSYNC
Defaults	0	0	0	0	0	0	0	1

G2, G1, G0: (Default = 0, 0, 0) Gain-Selection Bits. See Table 11 for PGA gain settings.

$\overline{B}$/U: (Default = 0) Bipolar-/Unipolar-Mode Selection: Set $\overline{B}$/U = 0 to select bipolar mode. Set $\overline{B}$/U = 1 to select unipolar mode.

BUF: (Default = 0) Buffer-Enable Bit. For unbuffered mode, disable the internal buffer of the MAX1415/MAX1416 to reduce power consumption by writing a 0 to the BUF bit. Write a 1 to this bit to enable the buffer. Use the internal buffer when acquiring high source-impedance input signals.

FSYNC: (Default = 1) Filter-Synchronization/ Conversion-Start Bit. Set FSYNC = 0 to begin calibration or conversion. The MAX1415/MAX1416 perform free-running conversions while FSYNC = 0. Set FSYNC = 1 to stop converting data and to hold the nodes of the digital filter, the filter-control logic, the calibration-control logic, and the analog modulator in a reset state. The $\overline{DRDY}$ output does not reset high if it is low (indicating that valid data has not yet been read from the data register) when FSYNC goes high. To clear $\overline{DRDY}$ output, read the data register.

Table 10. Operating-Mode Selection

MD1	MD0	OPERATING MODE
0	0	Normal Mode. Use this mode to perform normal conversions on the selected analog input channel.
0	1	Self-Calibration Mode. This mode performs self-calibration on the selected channel determined from CH0 and CH1 selection bits in the communications register (Table 6). Upon completion of self-calibration, the device returns to normal mode with MD1, MD0 returning to 0, 0. The $\overline{DRDY}$ output bit goes high when self-calibration is requested and returns low when the calibration is complete and a new data word is in the data register. Self-calibration performs an internal zero-scale and full-scale calibration. The analog inputs of the device are shorted together internally during zero-scale calibration and connected to an internally generated (V_{REF}/GAIN) voltage during full-scale calibration. The offset and gain registers for the selected channel are automatically updated with the calibration data.
1	0	Zero-Scale System-Calibration Mode. This mode performs zero-scale calibration on the selected channel determined from CH1 and CH0 selection bits in the communications register (Table 6). The $\overline{DRDY}$ output bit goes high when calibration is requested and returns low when the calibration is complete and a new data word is in the data register. Performing zero-scale calibration compensates for any DC offset voltage present in the ADC and system. Ensure that the analog input voltage is stable within 0.5 LSB for the duration of the calibration sequence. The offset register for the selected channel is updated with the zero-scale system-calibration data. Upon completion of calibration, the device returns to normal mode with MD1, MD0 returning to 0, 0.
1	1	Full-Scale System-Calibration Mode. This mode performs full-scale system-calibration on the selected channel determined from CH1 and CH0 selection bits in the communications register. This calibration assigns a full-scale output code to the voltage present on the selected channel. Ensure that the analog input voltage is stable within 0.5 LSB for the duration of the calibration sequence. The $\overline{DRDY}$ output bit goes high during calibration and returns low when the calibration is complete and a new data word is in the data register. The gain register for the selected channel is updated with the full-scale system-calibration data. Upon completion of calibration, the device returns to normal mode with MD1, MD0 returning to 0, 0.

Table 11. PGA Gain Selection

G2	G1	G0	PGA GAIN
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Clock Register

The byte-wide clock register is bidirectional, so it can be written and read. The byte written to the setup register sets the clock, filter first notch frequency, and the output data rate (see Table 12).

MXID: (Default = 1) Maxim-Identifier Bit. This is a read-only bit. Values written to this bit are ignored.

ZERO: (Default = 0) Zero Bit. This is a read-only bit. Values written to this bit are ignored.

INTCLK: (Default = 0) Internal Oscillator Bit. Set INTCLK = 1 to enable the internal oscillator. Set INTCLK = 0 to disable the internal oscillator.

CLKDIS: (Default = 0) Clock-Disable Bit. Set CLKDIS = 1 to disable the internally or externally generated clock from appearing on CLKOUT. When using a crystal or resonator across CLKIN and CLKOUT, the clock is stopped and no conversions take place when CLKDIS = 1. CLKOUT is held low during clock disable to save power. Set CLKDIS = 0 to allow other devices to use the output signal on CLKOUT as a clock source and/or to enable the external oscillator. The CLKOUT pin on the MAX1415/MAX1416 can drive one CMOS load.

CLKDIV: (Default = 0) Clock-Divider Control Bit. The MAX1415/MAX1416 each have an internal clock divider. Set this bit to 1 to divide the input clock by two. When this bit is set to 0, the MAX1415/MAX1416 operate at the internal or external oscillator frequency. CLKDIV has no effect on the internal oscillator.

CLK: (Default = 1) Clock Bit. When using the internal oscillator (INTCLK = 1), set CLK = 1 for a frequency of 2.4576MHz, and set CLK = 0 for a frequency of 1MHz. When using an external clock/oscillator, set CLK = 1 for f_{CLKIN} = 2.4576MHz with CLKDIV = 0, or f_{CLKIN} = 4.9152MHz with CLKDIV = 1.

Set CLK = 0 if the external clock frequency is 1MHz with CLKDIV = 0 or 2MHz with CLKDIV = 1.

FS1, FS0: (Default = 0, 1) Filter-Selection Bits. These bits, in addition to the CLK bit, determine the output data rate and the digital filter cutoff frequency. See Table 13 for FS1 and FS0 settings. Recalibrate when the filter characteristics are changed.

Data Register

The data register is a 16-bit read-only register. Figure 9 shows how to read conversion results using the data register.

The data from the data register is read through DOUT. DOUT changes on the falling edge of SCLK and is valid on the rising edge of SCLK. The data-register format is 16-bit straight binary for unipolar mode with zero scale equal to 0x0000, and offset binary for bipolar mode with zero scale equal to 0x1000.

Test Register

This register is reserved for factory testing of the device. For proper operation of the MAX1415/MAX1416, do not change this register from its default power-on reset values.

Offset and Gain-Calibration Registers

The MAX1415/MAX1416 contain one offset register and one gain register for each input channel. Each register is 24 bits wide and can be written and read. The offset registers store the calibration coefficients resulting from a zero-scale calibration, and the gain registers store the calibration coefficients resulting from a full-scale calibration. The data stored in these registers are 24-bit straight binary values representing the offset or gain errors associated with the selected channel. A 24-bit read or write operation can be performed on the calibration registers for any selected channel. During a write operation, 24 bits of data must be written to the register, or no data is transferred.

Table 12. Clock Register

	(MSB)							(LSB)
FUNCTION	**RESERVED**		**INTERNAL CLOCK ENABLE**	**CLOCK DISABLE**	**CLOCK DIVIDER**	**CLOCK SELECT**	**FILTER SELECT**	
Name	MXID	ZERO	INTCLK	CLKDIS	CLKDIV	CLK	FS1	FS0
Defaults	1	0	0	0	0	1	0	1

Table 13. Output Data Rate and Notch Frequency vs. Filter Select and CLKIN Frequency

CLKIN FREQUENCY f_{CLKIN} (MHz)*	CLK	FS1	FS0	OUTPUT DATA RATE (FIRST NOTCH) (Hz)	-3dB FILTER CUTOFF** (Hz)
1	0	0	0	20	5.24
1	0	0	1	25	6.55
1	0	1	0	100	26.2
1	0	1	1	200	52.4
2.4576	1	0	0	50	13.1
2.4576	1	0	1	60	15.7
2.4576	1	1	0	250	65.5
2.4576	1	1	1	500	131

**These values are given for CLKDIV = 0. External-clock frequency, f_{CLKIN}, equals two times the values in this column if CLKDIV = 1.*

***The filter -3dB filter cutoff frequency = 0.262 x filter first notch frequency.*

Write to the calibration registers in normal mode only. After writing to the calibration registers, the devices implement the new offset and gain-register calibration coefficients at the beginning of a new acquisition. To ensure the results are valid, discard the first conversion result after writing to the calibration registers.

To ensure that a conversion is not made using invalid calibration data, drive FSYNC high prior to writing to the calibration registers, and then release FSYNC low to initiate conversion.

Power-On Reset

At power-up, the serial interface, logic, digital filter, and modulator circuits are reset. The registers are set to their default values. The device returns to wait for a write to the communications register. For accurate measurements perform calibration routines after power-up. Allow time for the external reference and internal or external oscillator to start up before starting calibration. See the *Typical Operating Characteristics* for typical internal and external oscillator startup times.

Reset

Drive $\overline{\text{RESET}}$ low to reset the MAX1415/MAX1416 to power-on reset status. $\overline{\text{DRDY}}$ goes high and all communication to the MAX1415/MAX1416 is ignored while $\overline{\text{RESET}}$ is low. Upon releasing $\overline{\text{RESET}}$, the device must be reconfigured to begin a conversion. The device returns to waiting for a write to the communication register after a reset has been performed. Perform a calibration sequence following a reset for accurate conversions.

When using an external clock or crystal oscillator, the MAX1415/MAX1416 clock generator continues to run when $\overline{\text{RESET}}$ is pulled low. This allows any device running from CLKOUT to be uninterrupted when the device is in reset while using an external clock.

Selecting Custom Output Data Rates and First Notch Frequency

The recommended frequency range of the external clock is 400kHz to 2.5MHz (clkdw = 0). The output data rate and first notch frequency are dependent on the decimation rate of the digital filter. Table 14 shows the available decimation rates of the digital filter. The output data rate and filter first notch is calculated using the following formula:

$$\text{Output data rate} = \frac{f_{CLKIN}}{128 \times \text{Decimation Rate}} \times 0.5$$

(if CLKDIV = 1).

Table 14. Filter Select and Decimation Rate

CLK	FS1	FS0	DECIMATION RATE
0	0	0	391
0	0	1	313
0	1	0	78
0	1	1	39
1	0	0	384
1	0	1	320
1	1	0	77
1	1	1	38

$$\text{Output data rate} = \frac{f_{CLKIN}}{128 \times \text{Decimation Rate}}$$

(if CLKDIV = 0).

Note: First notch filter frequency = output data rate.

Performing a Conversion

At power-on reset, the MAX1415/MAX1416 expect a write to the communications register. Writing to the communications register selects the acquisition channel, read/write operation for the next register, power-down/normal mode, and the address of the following register to be accessed. The MAX1415/MAX1416 have six user-accessible registers, which control the function of the device and allow the result to be read. Write to the communications register before accessing any other registers.

Writing to the clock and setup registers after configuring and initializing the host processor serial port sets up the MAX1415/MAX1416. Use self- or system calibrations to minimize offset and gain errors (see the *Calibration* section for more details). Set FSYNC = 0 to begin calibration or conversion. The MAX1415/MAX1416 perform free-running acquisitions when FSYNC is low (see the Using FSYNC section). The µC can poll the $\overline{\text{DRDY}}$ bit of the communications register and read the data register when the $\overline{\text{DRDY}}$ bit returns a 0. For hardware polling, the $\overline{\text{DRDY}}$ output goes low when the new data is valid in the data register.

The data register can be read multiple times while the next conversion takes place.

The flow diagram in Figure 11 shows an example sequence required to perform a conversion on channel 1 (AIN1+/AIN1-) after a power-on reset.

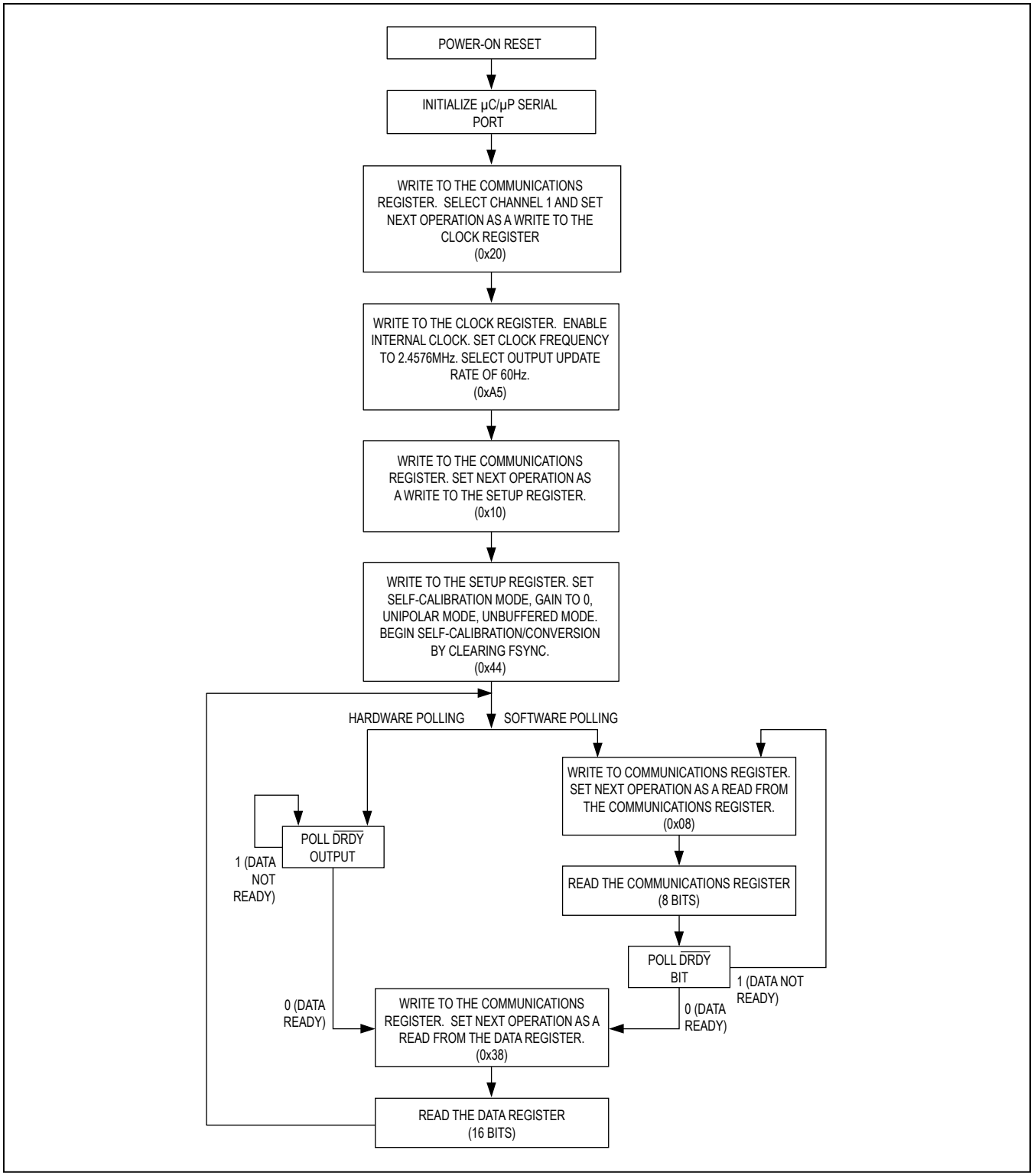


Figure 11. Sample Flow Diagram for Data Conversion

Using FSYNC

When FSYNC = 1, the digital filter and analog modulator are in a reset state, inhibiting normal operation. Set FSYNC = 0 to begin calibration or conversion.

When configured for normal operation (MD1 and MD0 set to 0), $\overline{DRDY}$ goes low 3 x 1/output data rate after FSYNC goes low to indicate that the new conversion result is ready to be read from the data register. $\overline{DRDY}$ returns high when a read operation on the data register is complete. As long as FSYNC remains low, the MAX1415/MAX1416 perform free-running conversions with the data registers updating at the output data rate. If the valid data is not read before the next conversion result is ready, $\overline{DRDY}$ returns high for 500 x $1/f_{CLKIN}$ before going low again to indicate a new conversion. Set FSYNC = 1 to stop converting data.

If FSYNC goes high while $\overline{DRDY}$ is low (indicating that valid data has not yet been read from the data register), $\overline{DRDY}$ does not reset high. $\overline{DRDY}$ remains low until the new data is read from the data register or until FSYNC goes low to begin a new conversion.

Table 15 provides the duration-to-mode bits and duration to $\overline{DRDY}$ for each calibration sequence. Duration-to-mode bits provide the time required for the calibration sequence to complete (MD1 and MD0 return to 0). Duration to $\overline{DRDY}$ provides the time until the first conversion result is valid in the data register ($\overline{DRDY}$ goes low).

The pipeline delay necessary to ensure that the first conversion result is valid is t_P (t_P = 2000 x $1/f_{CLKIN}$).

When selecting self-calibration (MD1 = 0, MD0 = 1), $\overline{DRDY}$ goes low 9 x 1/output data rate + t_P after FSYNC goes low (or after a write operation to the setup register with MD1 = 0 and MD0 = 1 is performed while FSYNC is already low) to indicate new data in the data register.

When zero-scale or full-scale calibration is selected, $\overline{DRDY}$ goes low 4 x 1/output data rate + t_P after FSYNC goes low (or while the zero-scale or full-scale calibration command is issued when FSYNC is already low) to indicate new data in the data register (see the *Calibration* section).

Calibration

To compensate for errors introduced by temperature variations or system DC offsets, perform an on-chip calibration. Select calibration options by writing to the MD1 and MD0 bits in the setup register (Table 9). If the part is in free running mode, that is, FSYNC = 0, then set FSYNC to 1 before the calibration command is written. Calibration removes gain and offset errors from the device and/or the system. Recalibrate with changes in ambient temperature, supply voltage, bipolar/unipolar mode, buffered/unbuffered mode, PGA gain, and output data rate.

The MAX1415/MAX1416 offer two calibration modes, self-calibration and system calibration. The channels of the MAX1415/MAX1416 are independently calibrated (see Table 8). The calibration coefficients resulting from a calibration sequence on a selected channel are stored in the corresponding offset and gain register pair.

Self- and system calibration automatically calculate the offset and gain coefficients, which are written to the offset and gain registers. These offset and gain coefficients provide offset and gain error correction for the specified channel.

Self-Calibration

Self-calibration compensates for offset and gain errors internal to the ADC. Prior to calibration, set the PGA gain, unipolar/bipolar mode, buffered/unbuffered mode, and input channel setting. During self-calibration, AIN+ and AIN- of the selected channel are internally shorted together. The ADC calibrates this condition as the zero-

Table 15. Calibration Sequences

CALIBRATION TYPE (MD1, MD0)	CALIBRATION SEQUENCE	DURATION-TO-MODE BITS*	DURATION TO $\overline{DRDY}$**
Self-calibration (0,1)	Internal zero-scale calibration at selected gain plus internal full-scale calibration at selected gain	6 x 1/output data rate	9 x 1/output data rate + t_P
Zero-scale system calibration (1,0)	Zero-scale calibration on AIN at selected gain	3 x 1/output data rate	4 x 1/output data rate + t_P
Full-scale system calibration (1,1)	Full-scale calibration on AIN at selected gain	3 x 1/output data rate	4 x 1/output data rate + t_P

**Duration-to-mode bits represents the completion of the calibration sequence.*

***Duration to $\overline{DRDY}$ represents the time at which a new conversion result is available in the data register.*

scale output level. For bipolar mode, this zero-scale point is the midscale of the bipolar transfer function. Next, an internally generated voltage (V_{REF}/GAIN) is applied across AIN+ and AIN-. This condition results in the full-scale calibration.

Start self-calibration by setting MD1 = 0, MD0 = 1, and FSYNC = 0 in the setup register. Self-calibration completes in 6 x 1/output data rate. The MD1 and MD0 bits both return to 0 at the end of calibration. The device returns to normal acquisition mode and performs a conversion, which completes in 3 x 1/output data rate after the self-calibration sequence.

The $\overline{DRDY}$ output goes high at the start of calibration and falls low when the calibration is complete and the next conversion result is valid in the data register. The total time for self-calibration and one conversion (time until $\overline{DRDY}$ goes low) is 9 x 1/output data rate. If $\overline{DRDY}$ is low before or goes low during the calibration command write to the setup register, $\overline{DRDY}$ takes up to one additional modulator cycle (128/f_{CLKIN}) to return high to indicate a calibration or conversion in progress.

System Calibration

System calibration compensates for offset and gain errors for the entire analog signal path including the ADC, signal conditioning, and signal source. System calibration is a two-step process and requires individual zero-scale and full-scale calibrations on the selected channel at a specified PGA gain. Recalibration is recommended with changes in ambient temperature, supply voltage, buffered/unbuffered mode, bipolar/unipolar mode, PGA gain, and output data rate.

Set the zero-scale reference point across AIN+ and AIN-. Start the zero-scale calibration by setting MD1 = 1, MD0 = 0, and FSYNC = 0 in the setup register. When zero-scale calibration is complete (3 x 1/output data rate), MD1 and MD0 both return to 0. $\overline{DRDY}$ goes high at the start of the zero-scale system calibration and returns low when there is a valid word in the data register (4 x 1/output data rate). The time until $\overline{DRDY}$ goes low is comprised of one zero-scale calibration sequence (3 x 1/output data rate) and one conversion on the AIN voltage (1 x 1/output data rate). If $\overline{DRDY}$ is low before or goes low during the calibration command write to the setup register, $\overline{DRDY}$ takes up to one additional modulator cycle (128/f_{CLKIN}) to return high to indicate a calibration or conversion in progress.

After performing a zero-scale calibration, connect the analog inputs to the full-scale voltage level (V_{REF}/GAIN). Perform a full-scale calibration by setting MD1 = 1 and MD0 = 1. After 3 x 1/output data rate, MD1 and MD0 both return to 0 at the completion of full-scale calibration. $\overline{DRDY}$ goes high at the beginning of calibration and returns low after calibration is complete and new data is in the data register (4 x 1/output data rate). The time until $\overline{DRDY}$ goes low is comprised of one full-scale calibration sequence (3 x 1/output data rate) and one conversion on the AIN voltage (1 x 1/output data rate). If $\overline{DRDY}$ is low before or goes low during the calibration command write to the setup register, $\overline{DRDY}$ takes up to one additional modulator cycle (128/f_{CLKIN}) to return high to indicate a calibration or conversion in progress.

In bipolar mode, the midpoint (zero scale) and positive full scale of the transfer function are used to calculate the calibration coefficients of the gain and offset registers. In unipolar mode, system calibration is performed using the two endpoints of the transfer function (Figures 4 and 5).

Power-Down Modes

The MAX1415/MAX1416 include a power-down mode to save power. Select power-down mode by setting PD = 1 in the communications register. The PD bit does not affect the serial interface or the status of the $\overline{DRDY}$ line. While in power-down mode, the MAX1415/MAX1416 retain the contents of all of its registers. Placing the part in power-down mode reduces current consumption to 2µA (typ) when in external CMOS clock mode and with CLKIN connected to V_{DD} or GND. If $\overline{DRDY}$ is high before the part enters power-down mode, then $\overline{DRDY}$ remains high until the part returns to normal operation mode and new data is available in the data register. If $\overline{DRDY}$ is low before the part enters power-down mode, indicating new data in the data register, the data register can be read during power-down mode. $\overline{DRDY}$ goes high at the end of this read operation. If the new data remains unread, $\overline{DRDY}$ stays low until the MAX1415/MAX1416 are taken out of power-down mode and resume data conversion. Resume normal operation by setting PD = 0. The device begins a new conversion with a result appearing in 3 x 1/output data rate + t_P, where t_P = 2000 x 1/f_{CLKIN}, after PD is set to 0. If the clock is stopped during power-down mode, allow sufficient time for the clock to startup before resuming conversion.

If the external crystal/resonator is used and CLKDIS = 0, CLKOUT remains active during power-down mode to provide a clock source for other devices in the system.

If the internal oscillator is used, power-down mode shuts off the internal oscillator.

Applications Information

Applications Examples

Strain-Gauge Measurement

Connect the differential inputs of the MAX1415/ MAX1416 to the bridge network of the strain gauge. In Figure 12, the analog positive supply voltage powers the bridge network and the MAX1415/MAX1416 along with the reference voltage in a ratiometric configuration. The on-chip PGA allows the MAX1415/MAX1416 to handle an analog input voltage range as low as 20mV to full scale.

Optical Isolation

For applications that require an optically isolated interface, see Figure 13. With 6N136-type optocouplers, the maximum clock speed is 4MHz. The maximum clock speed is limited by the degree of mismatch between the individual optocouplers. Faster optocouplers allow faster signaling at a higher cost.

Layout, Grounding, and Bypassing

Use PC boards with separate analog and digital ground planes. Connect the two ground planes together at the MAX1415/MAX1416 GND. Isolate the digital supply from the analog with a low-value resistor (10Ω) or ferrite bead when the analog and digital supplies come from the same source.

Ensure that digital return currents do not pass through the analog ground and that return-current paths are low impedance. A 5mA current flowing through a PC board ground trace impedance of only 0.05Ω creates an error voltage of approximately 250µV.

Layout the PC board to ensure digital and analog signal lines are kept separate. Do not run digital lines (especially the SCLK and DOUT) parallel to any analog lines. If they must cross one another, do so at right angles.

Bypass V_{DD} to the analog ground plane with a 0.1µF capacitor in parallel with a 1µF to 10µF low-ESR capacitor. Keep capacitor leads short for best supply-noise rejection. Bypass REF+, REF-, and all analog inputs with a 0.1µF capacitor to GND. Place all bypass capacitors as close to the device as possible to achieve the best decoupling.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. INL for the MAX1415/ MAX1416 is measured using the endpoint method. This is the more conservative method.

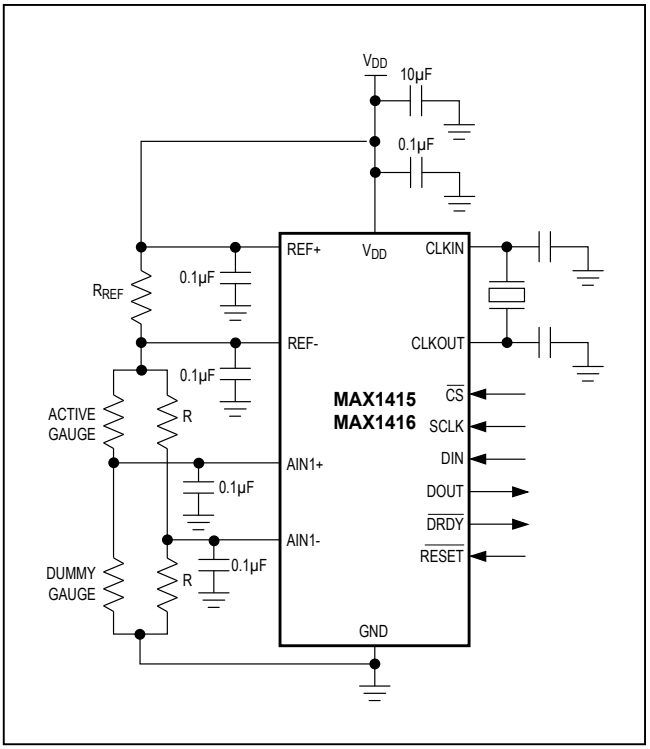


Figure 12. Strain Gauge Measurement

Unipolar Offset Error

For an ideal converter, the first transition occurs at 0.5 LSB above zero. Offset error is the amount of deviation between the measured first transition point and the ideal point.

Bipolar Zero Error

In bipolar mode, the ideal midscale transition occurs at AIN+ - AIN- = 0. Bipolar zero error is the measured deviation from this ideal value.

Gain Error

With a full-scale analog input voltage applied to the ADC (resulting in all ones in the digital code), gain error is defined as the amount of deviation between the ideal transfer function and the measured transfer function (with the offset error or bipolar zero error removed). Gain error is usually expressed in LSB or a percent of full-scale range (%FSR).

Positive Full-Scale Error

For the ideal transfer curve, the code edge transition that causes a full-scale transition to occur is 1.5 LSB below full scale. The positive full-scale error is the difference between this code transition of the ideal transfer function and the actual measured value at this code

transition. Unlike gain error, unipolar offset error and bipolar zero error are included in the positive full-scale error measurement.

Bipolar Negative Full-Scale Error

For the ideal transfer curve, the code edge transition that causes a negative full-scale transition to occur is 0.5 LSB above negative full scale. The negative full-scale error is the difference between the ideal value at this code transition and the actual measured value at this code transition.

Input Common-Mode Rejection

Input common-mode rejection is the ability of a device to reject a signal that is common to or applied to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels. Common-mode rejection ratio (CMRR) is the ratio of the differential signal gain to the common-mode signal gain.

Power-Supply Rejection Ratio

Power-supply rejection ratio (PSRR) is the ratio of the input signal change (V) to the change in the converter output (V). It is typically measured in decibels.

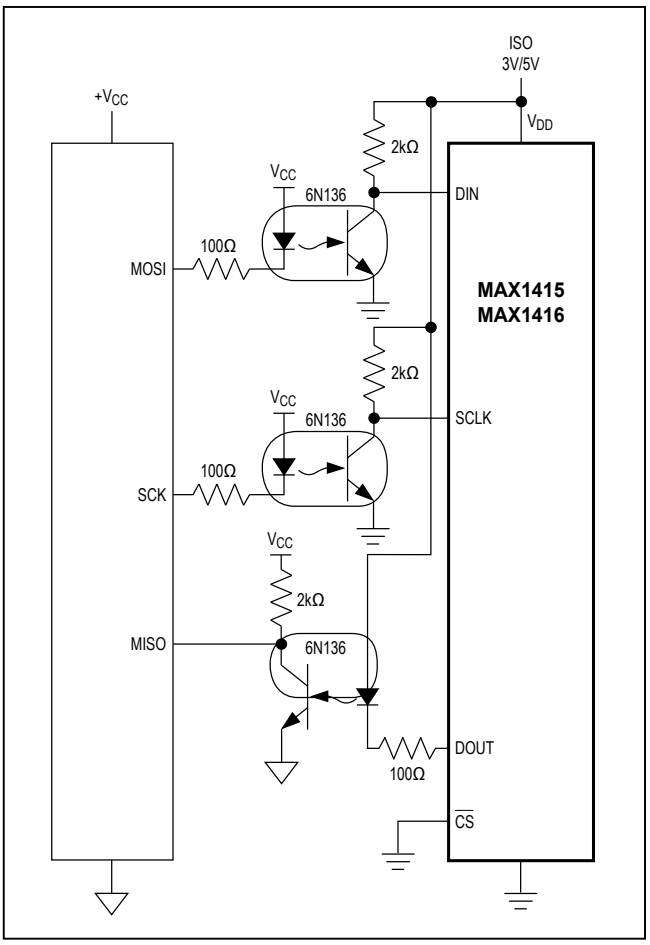


Figure 13. Optically Isolated Interface

Chip Information

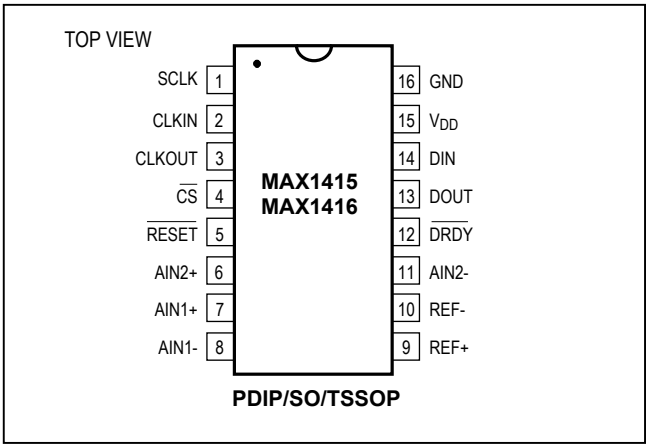
PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{DD} (V)
MAX1415EPE+	-45°C to +85°C	16 PDIP	3
MAX1415EWE+	-45°C to +85°C	16 Wide SO	3
MAX1415EUE+	-45°C to +85°C	16 TSSOP	3
MAX1416EPE+	-45°C to +85°C	16 PDIP	5
MAX1416EWE+	-45°C to +85°C	16 Wide SO	5
MAX1416EUE+	-45°C to +85°C	16 TSSOP	5
MAX1416AEWE+	-45°C to +85°C	16 Wide SO	5
MAX1416AEUE+	-45°C to +85°C	16 TSSOP	5

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
16 PDIP	P16+1	21-0043	—
16 SO	W16+1	21-0042	90-0107
16 TSSOP	U16+2	21-0066	90-0117

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	1/15	Updated *Benefits and Features* section	1
3	6/15	Updated *Absolute Maximum Ratings*, *Electrical Characteristics* globals, *Calibration* section, *Ordering Information*, and *Package Information*	2–8, 30, 33–35

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