19-2928; Rev 1; 2/07

EVALUATION KIT AVAILABLE

Quad Copper-Cable Signal Conditioner

General Description

The MAX3983 is a quad copper-cable signal conditioner that operates from 2.5Gbps to 3.2Gbps. It provides compensation for 4x copper InfiniBand and 10Gbase-CX4 Ethernet links, allowing spans of 20m with 24AWG and 15m with 28AWG. The cable driver section provides four selectable preemphasis levels. The input to the cable driver compensates for up to 0.5m of FR4 circuit board material. The cable receiver section provides additional fixed input equalization while offering selectable preemphasis to drive FR4 circuit boards up to 0.5m.

The MAX3983 also features signal detection on all eight inputs and internal loopback that allows for diagnostic testing. It is packaged in a 10mm x 10mm, 68-pin QFN and operates from 0°C to +85°C.

Applications

4x InfiniBand (4 x 2.5Gbps)

10Gbase-CX4 Ethernet (4 x 3.125Gbps)

10G Fibre Channel XAUI (4 x 3.1875Gbps)

4x Copper-Cable or Backplane Transmission (1Gbps to 3.2Gbps)

Pin Configuration appears at end of data sheet.

Features

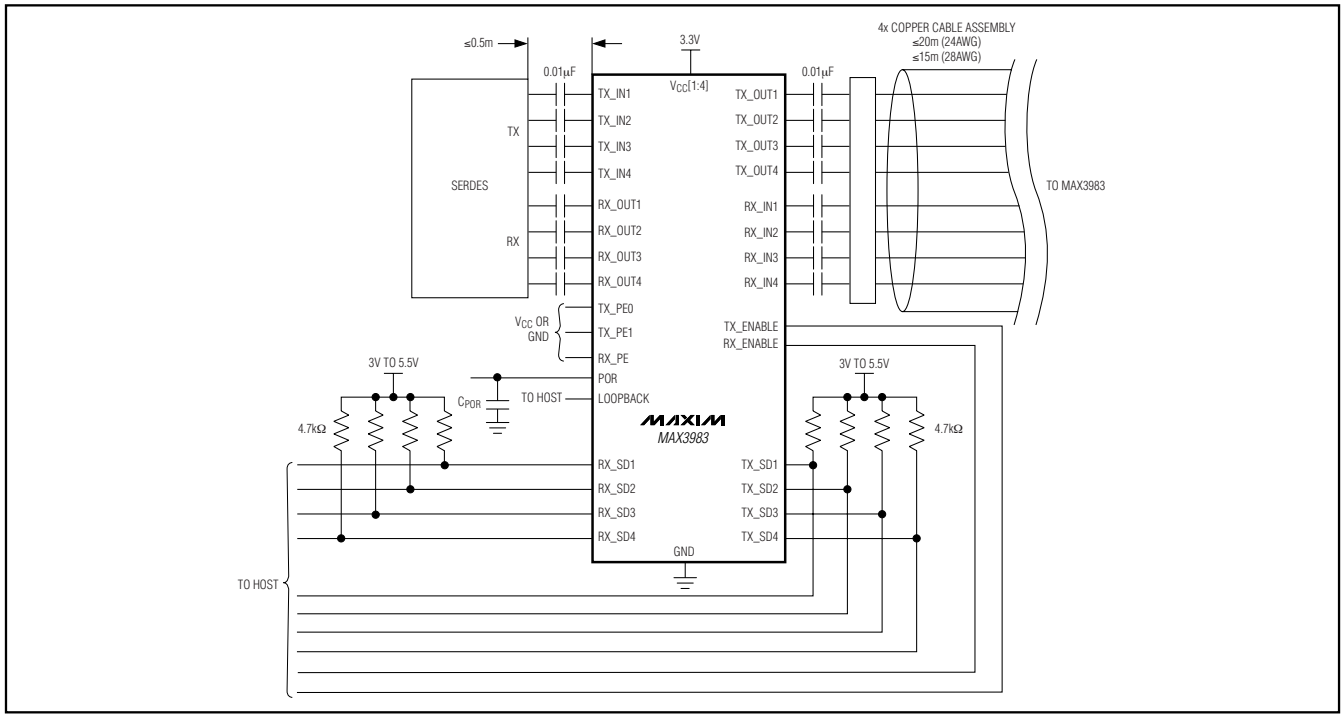
- **Link Features**
  - **Span 20m with 24AWG, 15m with 28AWG**
  - **Span 0.5m of FR4 on Each Host**
  - **1.6W Total Power with 3.3V Supply**
  - **Loopback Function**
- **Cable Driver Features**
  - **Selectable Output Preemphasis**
  - **FR4 Input Equalization**
  - **Signal Detect for Each Channel**
  - **Output Disable**
- **Cable Receiver Features**
  - **Selectable FR4 Output Preemphasis**
  - **Cable Input Equalization**
  - **Signal Detect for Each Channel**
  - **Output Disable**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3983UGK	0°C to +85°C	68 QFN	G6800-4
MAX3983UGK+	0°C to +85°C	68 QFN	G6800-4

+Denotes lead-free package.

Typical Application Circuit



Quad Copper-Cable Signal Conditioner

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +6.0V
Continuous CML Output Current at
TX_OUT[1:4]±, RX_OUT[1:4]± .....±25mA
Voltage at TX_IN[1:4]±, RX_IN[1:4]±, RX_SD[1:4], TX_SD[1:4], RX_ENABLE, TX_ENABLE, RX_PE, TX_PE[0:1], LOOPBACK, POR (with series resistor ≥4.7kΩ).....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
68-Pin QFN (derate 41.7mW/°C above +85°C).....2.7W
Operating Junction Temperature Range (T_J)....-55°C to +150°C
Storage Ambient Temperature Range (T_S) .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		RX_EN = V_{CC}, TX_EN = 0V		360	430	mA
		RX_EN = 0V, TX_EN = V_{CC}		365	430	
		RX_EN = V_{CC}, TX_EN = V_{CC}		495	580	
OPERATING CONDITIONS						
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply Noise Tolerance		1MHz ≤ f < 2GHz		40		mV_{P-P}
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data (Note 1)	2.5		3.2	Gbps
CID		Consecutive identical digits (bits)			10	Bits
STATUS OUTPUTS: RX_SD[1:4], TX_SD[1:4]						
Signal-Detect Open-Collector Current Sink		Signal detect asserted	0		25	µA
		Signal detect unasserted V_{OL} ≤ 0.4V with 4.7kΩ pullup resistor	1.0	1.11		mA
		V_{CC} = 0V, pullup supply = 5.5V, external pullup resistor ≥4.7kΩ	0		25	µA
Signal-Detect Response Time		Time from RX_IN[1:4] or TX_IN[1:4] dropping below $85mV_{P-P}$ or rising above $175mV_{P-P}$ to 50% point of signal detect		0.35		µs
Signal-Detect Transition Time		Rise time or fall time (10% to 90%)		200		ns
Power-On Reset Delay		1µF capacitor on POR to GND		6		ms
CONTROL INPUTS: RX_ENABLE, TX_ENABLE, RX_PE, TX_PE0, TX_PE1, LOOPBACK						
Voltage, Logic High	V_{IH}		1.5			V
Voltage, Logic Low	V_{IL}				0.5	V
Current, Logic High	I_{IH}	V_{IH} = V_{CC}	-150		+150	µA
Current, Logic Low	I_{IL}	V_{IL} = 0V	-150		+150	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
TX SECTION (CABLE DRIVER)									
PC Board Input Swing		Measured differentially at the signal source (Note 1)				800		1600	mV_{P-P}
Input Resistance		TX_IN[1:4]+ to TX_IN[1:4]-, differential				85	100	115	Ω
Input Return Loss		100MHz to 2GHz (Note 1)				10	17		dB
Output Swing		TX_ENABLE = high (Notes 1, 2)				1300	1500	1600	mV_{P-P}
		TX_ENABLE = low						30	
Output Resistance		TX_OUT[1:4]+ or TX_OUT[1:4]- to V_{CC}, single ended				42	50	58	Ω
Output Return Loss		100MHz to 2GHz (Note 1)				10	13		dB
Output Transition Time	t_r, t_f	20% to 80% (Notes 1, 3)						80	ps
Random Jitter		(Notes 1, 3)						1.6	ps_{RMS}
Output Preemphasis		See Figure 1	**TX_PE1**	**TX_PE0**					dB
			0	0			3		
			0	1			6		
			1	0			9		
			1	1			12		
Residual Output Deterministic Jitter at 2.5Gbps (Notes 1, 4, 5)		**Source to TX_IN**	**TX_OUT to Load**	**TX_PE1**	**TX_PE0**		0.10	0.15	UI_{P-P}
		6-mil FR4 ≤ 20in	1m, 28AWG	0	0				
			5m, 28AWG	0	1				
			10m, 24AWG	1	0				
			15m, 24AWG	1	1				
Residual Output Deterministic Jitter at 3.2Gbps (Notes 1, 4, 5)		**Source to TX_IN**	**TX_OUT to Load**	**TX_PE1**	**TX_PE0**		0.15	0.20	UI_{P-P}
		6-mil FR4 ≤ 20in	1m, 28AWG	0	0				
			5m, 28AWG	0	1				
			10m, 24AWG	1	0				
			15m, 24AWG	1	1				
Signal-Detect Assert Level		TX_IN for TX_SD = high (Note 6)				800			mV_{P-P}
Signal-Detect Off		TX_IN for TX_SD = low (Note 6)						200	mV_{P-P}
RX SECTION (CABLE RECEIVER)									
Cable Input Swing		Measured differentially at the signal source (Note 1)				1000		1600	mV_{P-P}
Input Vertical Eye Opening		Measured differentially at the input of the MAX3983 (Note 1)				175		1600	mV_{P-P}
Input Resistance		RX_IN[1:4]+ to RX_IN[1:4]-, differential				85	100	115	Ω
Input Return Loss		100MHz to 2GHz (Note 1)				10	18		dB

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Swing		RX_ENABLE = high (Notes 1, 7)			1100		1500	mV_{P-P}
		RX_ENABLE = low					30	
Output Resistance		RX_OUT[1:4]+ or RX_OUT[1:4]- to V_{CC}, single ended			42	50	58	Ω
Output Return Loss		100MHz to 2GHz (Note 1)			10	15		dB
Output Transition Time	t_r, t_f	20% to 80% (Notes 1, 8)				45	80	ps
Random Jitter		(Notes 1, 8)					1.6	ps_{RMS}
Output Preemphasis		RX_PE = low				3		dB
		RX_PE = high				6		
Residual Output Deterministic Jitter at 2.5Gbps (Notes 1, 5, 9, 10)		**Source to RX_IN**	**RX_OUT to Load**	**RX_PE**				
		5m, 28AWG IB Cable Assembly without preemphasis	0in, 6-mil FR4	0		0.10	0.15	UI_{P-P}
			20in, 6-mil FR4	1				
Residual Output Deterministic Jitter at 3.2Gbps (Notes 1, 5, 9, 10)		**Source to RX_IN**	**RX_OUT to Load**	**RX_PE**				
		5m, 28AWG IB cable assembly without preemphasis	0in, 6-mil FR4	0		0.15	0.20	UI_{P-P}
			20in, 6-mil FR4	1				
Signal-Detect Assert Level		RX_IN for RX_SD = high (Note 11)			175			mV_{P-P}
Signal-Detect Off		RX_IN for RX_SD = low (Note 11)					85	mV_{P-P}
END-TO-END JITTER (TX AND RX COMBINED PERFORMANCE)								
Residual Output Deterministic Jitter at 2.5Gbps (Notes 1, 12, 13, 14)		**Source to TX_IN**	**TX_OUT to RX_IN**	**TX_PE1** / **TX_PE0** / **RX_OUT to Load** / **RX_PE**		0.15	0.20	UI_{P-P}
		6-mil FR4 ≤ 20in	1m, 24AWG	0 / 0 / 0in / 0				
			15m, 24AWG	1 / 1 / 20in / 1				
			20m, 24AWG	1 / 1 / 20in / 1		0.2	0.25	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS						MIN	TYP	MAX	UNITS
		Source to TX_IN	TX_OUT to RX_IN	TX_PE1	TX_PE0	RX_OUT to Load	RX_PE				
Residual Output Deterministic Jitter at 3.2Gbps (Notes 1, 12, 13, 14)									0.20	0.25	UI_{P-P}
		6-mil FR4 ≤ 20 in	1m, 24AWG	0	0	5in	0				
			15m, 24AWG	1	1	20in	1				
			20m, 24AWG	1	1	20in	1		0.25	0.3	

Note 1: Guaranteed by design and characterization.

Note 2: Measured with 2in of FR4 through InfiniBand connector with TX_PE1 = TX_PE0 =1.

Note 3: Measured at the chip using 0000011111 or equivalent pattern. TX_PE1 = TX_PE0 = 0 for minimum preemphasis.

Note 4: All channels under test are not transmitting during test. Channel tested with XAUI CJPAT, as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5- character).

Note 5: Cables are unequalized, Amphenol Spectra-Strip 24AWG and 28AWG or equivalent equipped with Fujitsu "MicroGiga" connector or equivalent. All other channels are quiet. Residual deterministic jitter is the difference between the source jitter and the output jitter at the load. The deterministic jitter (DJ) at the output of the transmission line must be from media-induced loss and not from clock-source modulation. Depending upon the system environment, better results can be achieved by selecting different preemphasis levels.

Note 6: Tested with a 1GHz sine wave applied at TX_IN under test with less than 5in of FR4.

Note 7: Measured with 3in of FR4 with RX_PE = 1.

Note 8: Measured at the chip using 0000011111 or equivalent pattern. RX_PE = low (minimum). Signal source is $1V_{P-P}$ with 5m, 28AWG InfiniBand cable.

Note 9: All other receive channels are quiet. TX_ENABLE = 0. Channel tested with XAUI CJPAT as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5- character).

Note 10: FR4 board material: 6-mil-wide, 100Ω, edge-coupled stripline ($\tan\delta = 0.022$, $4.0 < \varepsilon_R < 4.4$).

Note 11: Tested with a 1GHz sine wave applied at RX_IN under test with less than 5in of FR4.

Note 12: Channel tested with XAUI CJPAT as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5- character).

Note 13: Cables are unequalized, Amphenol Spectra-Strip 24AWG or equivalent equipped with Fujitsu "MicroGiga" connector or equivalent. Residual deterministic jitter is the difference between the source jitter at point A and the load jitter at point B in Figure 2. The deterministic jitter (DJ) at the output of the transmission line must be from media-induced loss and not from clock-source modulation. Depending upon the system environment, better results can be achieved by selecting different preemphasis levels.

Note 14: Valid with pattern generator deterministic jitter as high as $0.17UI_{P-P}$.

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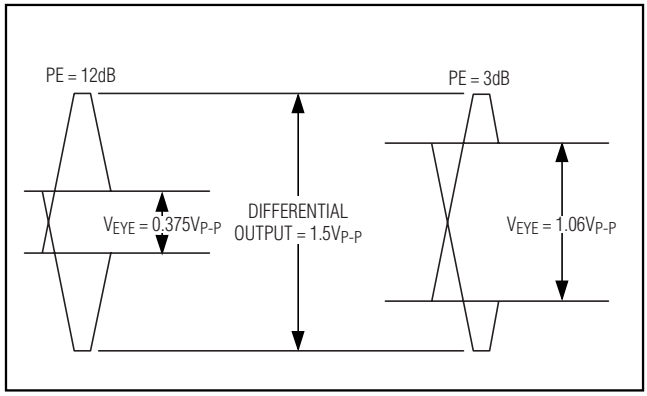


Figure 1. Illustration of TX Preemphasis in dB

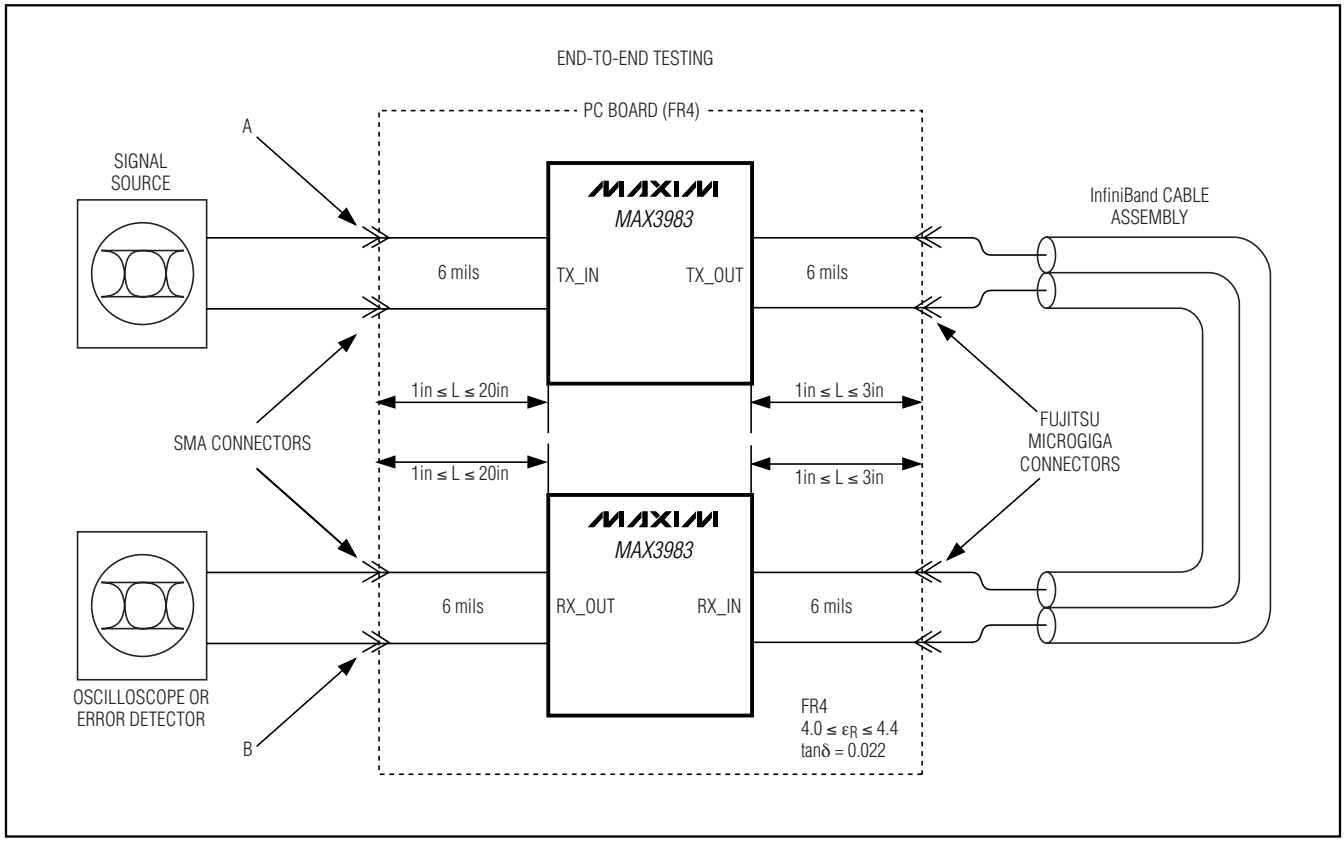
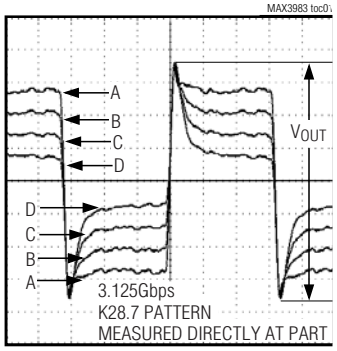


Figure 2. End-to-End Test Setup. The points labeled A and B are referenced for AC parameter test conditions.

Typical Operating Characteristics

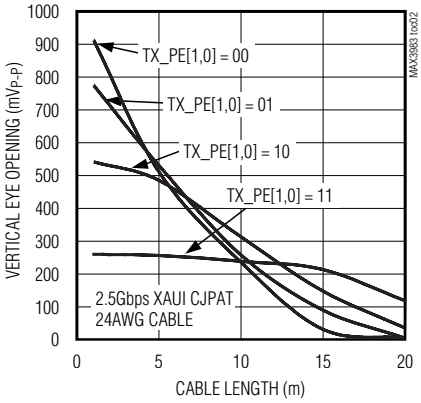
(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

TRANSIENT REPSONSE

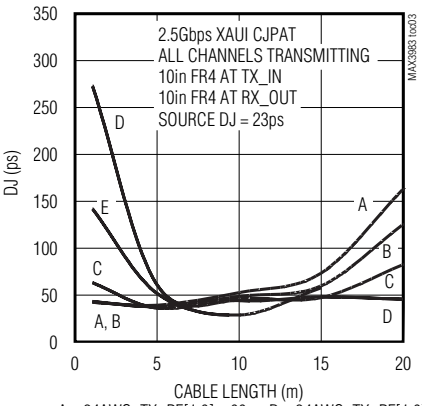


A = 3dB, TX_PE = 00 C = 9dB, TX_PE = 10
B = 6dB, TX_PE = 01 D = 12dB, TX_PE = 11

VERTICAL EYE OPENING vs. CABLE LENGTH

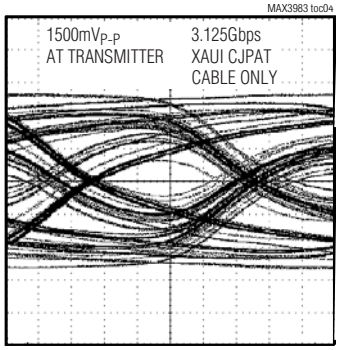


END-TO-END DETERMINISTIC JITTER vs. CABLE LENGTH



A = 24AWG, TX_PE[1,0] = 00 D = 24AWG, TX_PE[1,0] = 11
B = 24AWG, TX_PE[1,0] = 01 E = 28AWG, TX_PE[1,0] = 11
C = 24AWG, TX_PE[1,0] = 10

10m 24AWG UNEQUALIZED CABLE ASSEMBLY OUTPUT WITHOUT MAX3983



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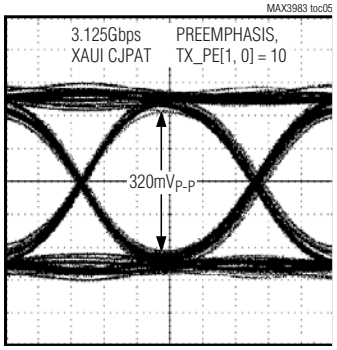
10m 24AWG UNEQUALIZED CABLE ASSEMBLY OUTPUT WITH MAX3983 PREEMPHASIS



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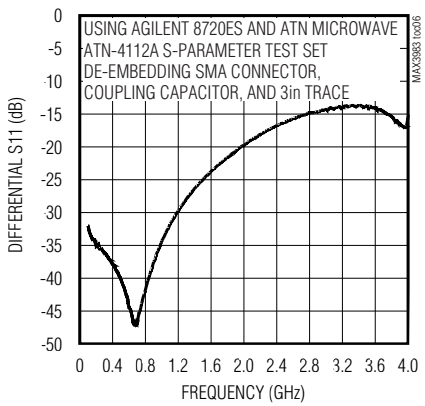
TX_IN INPUT RETURN LOSS vs. FREQUENCY



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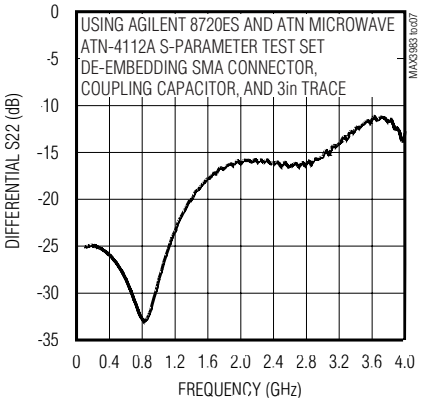
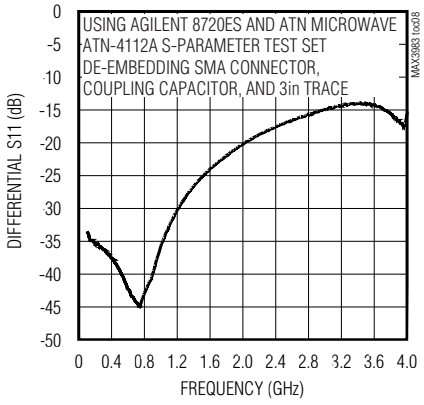
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

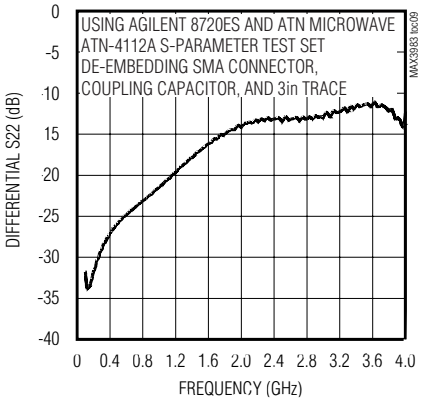
TX_OUT OUTPUT RETURN LOSS vs. FREQUENCY



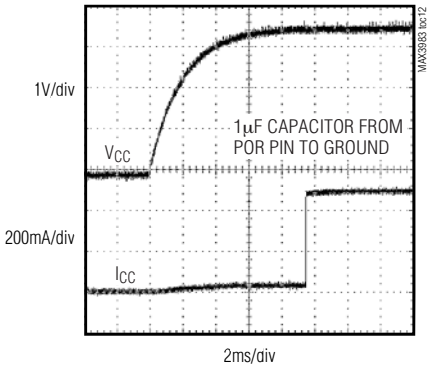
RX_IN INPUT RETURN LOSS vs. FREQUENCY



RX_OUT OUTPUT RETURN LOSS vs. FREQUENCY



POWER-ON RESET DELAY WITH SUPPLY RAMP



Pin Description

PIN	NAME	FUNCTION
1, 2, 16, 17	TX_SD1 to TX_SD4	PC Board Receiver Signal Detect, TTL Output. This output is open-collector TTL, and therefore requires an external 4.7kΩ to 10kΩ pullup resistor to V_{CC}. These outputs sink current when the input signal level is not valid.
3, 15	$V_{CC}1$	Power-Supply Connection for TX Inputs. Connect to +3.3V.
4, 7, 10, 13	TX_IN1- to TX_IN4-	PC Board Receiver Negative Data Inputs, CML. These inputs are internally differentially terminated to the corresponding TX_IN+ with 100Ω.
5, 8, 11, 14	TX_IN1+ to TX_IN4+	PC Board Receiver Positive Data Inputs, CML. These inputs are internally differentially terminated to the corresponding TX_IN- with 100Ω.
6, 9, 12, 40, 43, 46	GND	Circuit Ground
18	TX_ENABLE	Cable Transmitter Enable Input, LVTTL with 40kΩ Internal Pullup. This pin enables all four cable transmitter outputs TX_OUT[1:4]. When low, differential output is less than $30mV_{P-P}$. Set high or open for normal operation.
19	N.C.	No Connection. Do not connect this pin.
20, 23, 26, 29, 32	$V_{CC}2$	Power-Supply Connection for TX Outputs. Connect to +3.3V.
21, 24, 27, 30	TX_OUT1+ to TX_OUT4+	Cable Transmitter Positive Data Outputs, CML. These outputs are terminated with 50Ω to $V_{CC}2$.
22, 25, 28, 31	TX_OUT1- to TX_OUT4-	Cable Transmitter Negative Data Outputs, CML. These outputs are terminated with 50Ω to $V_{CC}2$.
33	TX_PE0	Cable Transmitter Preemphasis Control Input, LVTTL with 40kΩ Internal Pullup. This pin is the least significant bit of the 2-bit preemphasis control. Set high or open to assert this bit.
34	TX_PE1	Cable Transmitter Preemphasis Control Input, LVTTL with 40kΩ Internal Pullup. This pin is the most significant bit of the 2-bit preemphasis control. Set high or open to assert this bit.
35, 36, 50, 51	RX_SD4 to RX_SD1	Cable Receiver Signal Detect, TTL Output. This output is open-collector TTL, and therefore it requires an external 4.7kΩ to 10kΩ pullup resistor to V_{CC}. These outputs sink current when the input signal level is not valid.
37, 49	$V_{CC}3$	Power-Supply Connection for RX Inputs. Connect to +3.3V.
38, 41, 44, 47	RX_IN4- to RX_IN1-	Cable Receiver Negative Data Inputs, CML. These inputs are internally differentially terminated to the corresponding RX_IN+ with 100Ω.
39, 42, 45, 48	RX_IN4+ to RX_IN1+	Cable Receiver Positive Data Inputs, CML. These inputs are internally differentially terminated to the corresponding RX_IN- with 100Ω.
52	RX_ENABLE	PC Board Transmitter Enable Input, LVTTL with 40kΩ Internal Pullup. This pin enables all four PC board transmitter outputs RX_OUT[1:4]. When low, differential output is less than $30mV_{P-P}$. Set high or open for normal operation.
53	POR	Power-On Reset Connection. Connect external capacitor $0.1\mu F \le C_{POR} \le 10\mu F$ to ground. See the *Detailed Description*.
54, 57, 60, 63, 66	$V_{CC}4$	Power-Supply Connection for RX Outputs. Connect to +3.3V.

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Pin Description (continued)

PIN	NAME	FUNCTION
55, 58, 61, 64	RX_OUT4+ to RX_OUT1+	PC Board Transmitter Positive Data Outputs, CML. These outputs are terminated with 50Ω to $V_{CC}4$.
56, 59, 62, 65	RX_OUT4- to RX_OUT1-	PC Board Transmitter Negative Data Outputs, CML. These outputs are terminated with 50Ω to $V_{CC}4$.
67	RX_PE	PC Board Transmitter Preemphasis Control Input, LVTTL with 40kΩ Internal Pullup. Set high or open to assert this bit.
68	LOOPBACK	Loopback Enable Input, LVTTL with 40kΩ Internal Pullup. Set low for normal operation. Set high or open for internal connection of TX_IN to RX_OUT. TX_OUT continues to transmit when loopback is enabled.
EP	Exposed Pad	Exposed Pad. Signal and supply ground. For optimal high-frequency performance and thermal conductivity, this pad must be soldered to the circuit board ground.

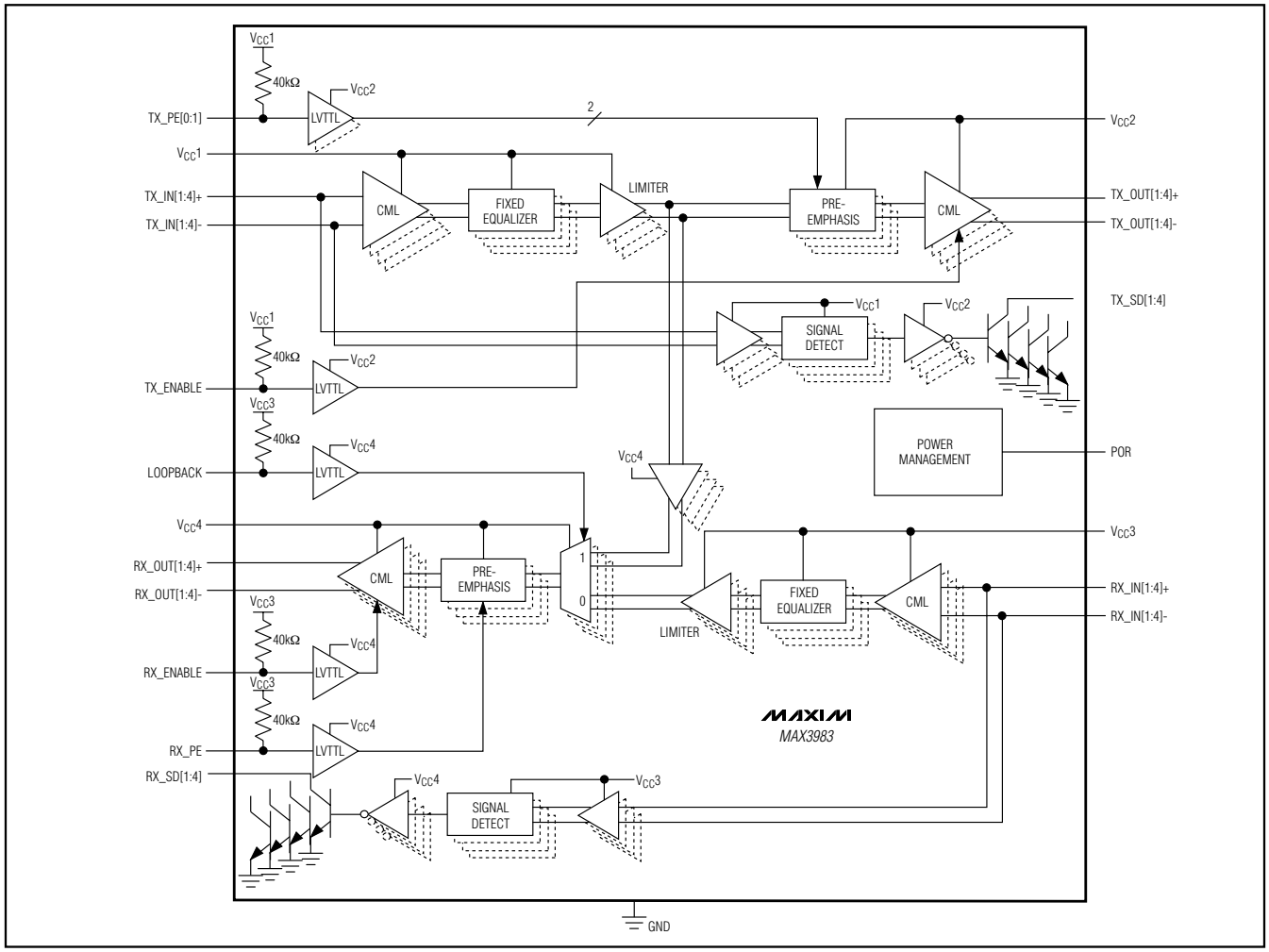


Figure 3. Functional Diagram

Detailed Description

The MAX3983 comprises a PC board receiver and cable driver section (TX), as well as a cable receiver and PC board driver section (RX). Equalization and signal detection are provided in each receiver, and preemphasis is included in each transmitter. The MAX3983 includes separate enable control for the TX outputs and RX outputs. Loopback is provided for diagnostic testing.

PC Board Receiver and Cable Driver (TX_IN and TX_OUT)

Data is fed into the MAX3983 from the host through a CML input stage and fixed equalization stage. The fixed equalizer in the PC board receiver corrects for up to 20in of PC board loss on FR4 material. The cable driver includes four-state preemphasis to compensate for up to 20m of 24AWG, 100Ω balanced cable. Table 1 is provided for easy translation between preemphasis expressions. Residual jitter of the MAX3983 is independent of up to $0.17UI_{P-P}$ source jitter.

Cable Receiver and PC Board Driver (RX_IN and RX_OUT)

The fixed equalizer on each RX input provides approximately 6dB equalization to correct for up to 5m of 28AWG, 100Ω balanced cable. The PC board driver includes two-state preemphasis to compensate for up to 20in of FR4 material.

Signal-Detect Outputs

Signal detect (SD) is provided on all eight data inputs. Pullup resistors should be connected from the SD outputs to a supply in the 3.0V to 5.5V range. The signal-detect outputs are not valid until power-up is complete. Typical signal-detect response time is 0.35µs.

In the RX section, the SD output asserts high when the RX_IN signal amplitude is greater than $175mV_{P-P}$. RX_SD deasserts low when the RX_IN signal amplitude drops below $85mV_{P-P}$.

In the TX section, the SD output asserts high when the TX_IN signal amplitude is greater than $800mV_{P-P}$. TX_SD deasserts low when the TX_IN signal amplitude drops below $200mV_{P-P}$.

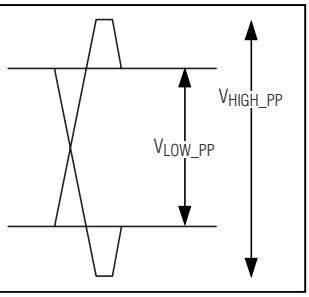
TX and RX Enable

The TX_ENABLE and RX_ENABLE pins enable TX and RX, respectively. Typical enable time is 15ns, and typical disable time is 25ns. The enable inputs may be connected to signal-detect outputs to automatically detect an incoming signal (see the *Autodetect* section).

Power-On Reset

To limit inrush current, the MAX3983 includes internal power-on reset circuitry. Connect a capacitor $0.1µF \le C_{POR} \le 10µF$ from POR to ground. With C_{POR} = 1µF, power-on delay is 6ms (typ).

Table 1. Preemphasis Translation

RATIO	α	10Gbase-CX4	IN dB	
$\frac{V_{HIGH\_PP}}{V_{LOW\_PP}}$	$\frac{V_{HIGH\_PP} - V_{LOW\_PP}}{V_{HIGH\_PP} + V_{LOW\_PP}}$	$1 - \frac{V_{LOW\_PP}}{V_{HIGH\_PP}}$	$20\left[\log\left(\frac{V_{HIGH\_PP}}{V_{LOW\_PP}}\right)\right]$	
1.41	0.17	0.29	3	
2.00	0.33	0.50	6	
2.82	0.48	0.65	9	
4.00	0.60	0.75	12	

Quad Copper-Cable Signal Conditioner

Applications Information

Signal-Detect Output Leakage Current Considerations

If all four RX or TX signal-detect outputs are to be connected together to form one signal detect, the leakage current of the output stage needs to be considered. Each SD output sinks a maximum of 25µA when asserted, so when four are connected together, a maximum of 100µA is possible. The value of the pullup resistor connected to pullup voltage V_{PULLUP} should be selected so the leakage current does not cause the output voltage to fall below the threshold of the next stage. For example, if the signal-detect outputs are connected together and to a stage with a logic-high threshold of 1.5V, the pullup resistor needs to be chosen so $V_{PULLUP} - I_{LEAKAGE} \times R_{PULLUP} > 1.5V$. In this case, if $V_{PULLUP} = 3.0V$, R_{PULLUP} should be less than 15kΩ.

Autodetect

The MAX3983 can automatically detect an incoming signal and enable the appropriate outputs. Autodetect of the RX side is done by connecting RX_SD[1:4] together with a pullup resistor (value 4.7kΩ to 10kΩ to V_{CC}) to RX_ENABLE. For the TX side, this is done by connecting TX_SD[1:4] together with a pullup resistor (value 4.7kΩ to 10kΩ to V_{CC}) to TX_ENABLE (Figure 4). If signal is detected on all channels, SD is high and forces the corresponding ENABLE high. Leaving the inputs to the MAX3983 open (i.e., floating) is not recommended, as noise amplification can occur and create undesirable output signals. Autodetect is recommended to eliminate noise amplification or possible oscillation. When using autodetect, the link length is determined by the received signal strength. It is possible to reach longer distances if the autodetect configuration is not used.

Using Loopback with Autodetect

If the MAX3983 is configured for autodetection, RX_ENABLE is controlled by the RX_SD[1:4] outputs. Since loopback requires RX_ENABLE to be high, a simple OR gate can be used to enable the RX outputs when either RX_SD[1:4] is high or when LOOPBACK is high (Figure 5).

InfiniBand and 10Gbase-CX4 Transition Time Specification

InfiniBand specifies a minimum transition time (20% to 80%) of 100ps and CX4 specifies a minimum of 60ps. Both are specified at the connector interface to the cable. The output transition times of the MAX3983 are 45ps (typ) and therefore require some care to increase this time. Approximately 3in of FR4 with 4-mil-wide lines is sufficient to lengthen the transition time to 60ps. For 100ps transition times, additional length can be used or an additional 1.5pF capacitor can be placed across the outputs of the MAX3983. Do not use high-speed dielectric material for the circuit board if the application requires the use of the InfiniBand or CX4 type connector system. With such materials, the fast edges of the

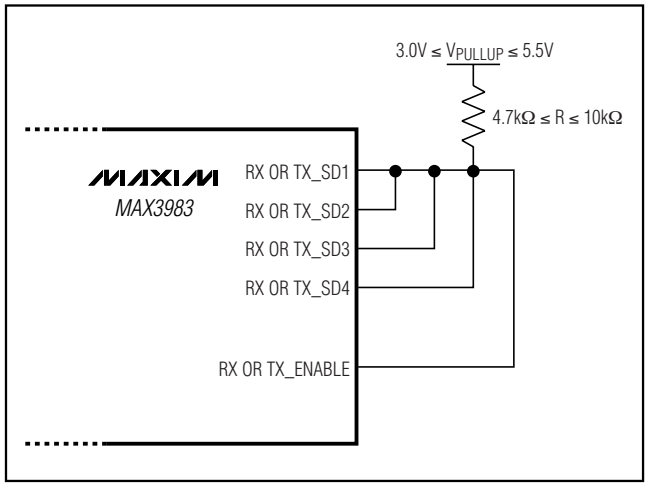


Figure 4. Autodetection Using Corresponding Signal-Detect Outputs and Enable Input

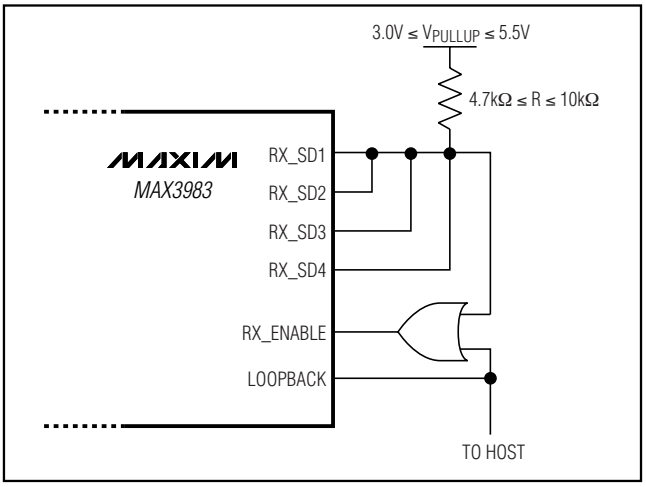


Figure 5. Loopback in Autodetect Mode

MAX3983 will produce excessive crosstalk in InfiniBand and CX4 cable assemblies.

Crosstalk

For InfiniBand and 10Gbase-CX4 applications, it is imperative to know the near-end crosstalk characteristics of the cable assemblies. 10Gbase-CX4 has defined the upper limit over frequency for near-end crosstalk (NEXT) with single and multiple aggressors. InfiniBand has only specified a percentage as measured in the time domain relative to the transmitter output. Regardless of the specification method, NEXT is a critical component of the link performance. When using larger amounts of preemphasis, the received eye height is small and vulnerable to NEXT. For those situations requiring a large transmit preemphasis, the NEXT should be less than -30dB at frequencies from 1GHz to 3GHz. It should be noted that cables that meet the 10Gbase-CX4 NEXT and MDNEXT should provide adequate isolation.

Layout Considerations

Circuit board layout and design can significantly affect the performance of the MAX3983. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on the data signals. Power-supply decoupling should also be placed as close to the V_{CC} pins as possible. There should be sufficient supply filtering. Always connect all V_{CC}s to a power plane. Take care to isolate the input from the output signals to reduce feedthrough. The performance of the equalizer is optimized for lossy environments. For best results, use board material with a dielectric tangential loss of approximately 0.02 and 4-mil-wide transmission lines. High-speed materials with tangential loss of less than 0.01 can be used, but require special care to reduce near-end crosstalk in cable assemblies.

Exposed-Pad Package

The exposed-pad, 68-pin QFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The pad is electrical ground on the MAX3983 and must be soldered to the circuit board for proper thermal and electrical performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Interface Schematics

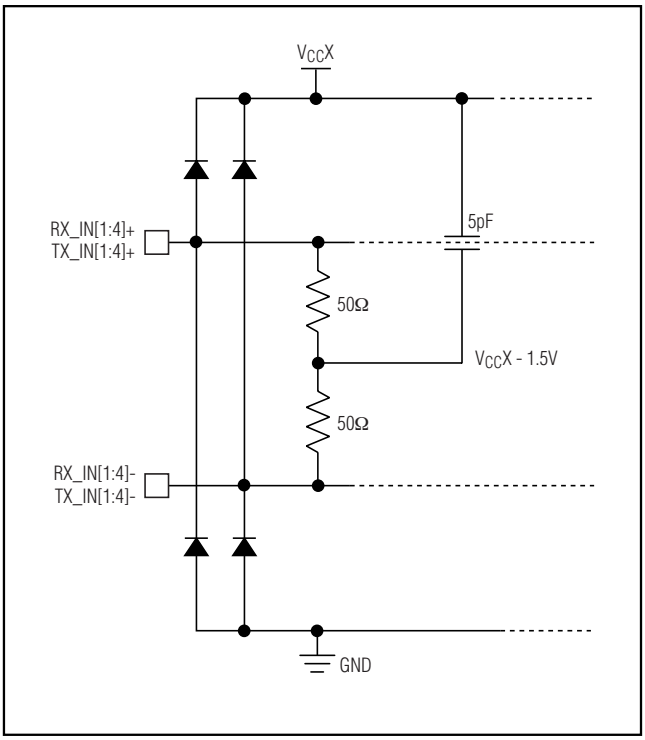


Figure 6. RX_IN and TX_IN Equivalent Input Structure

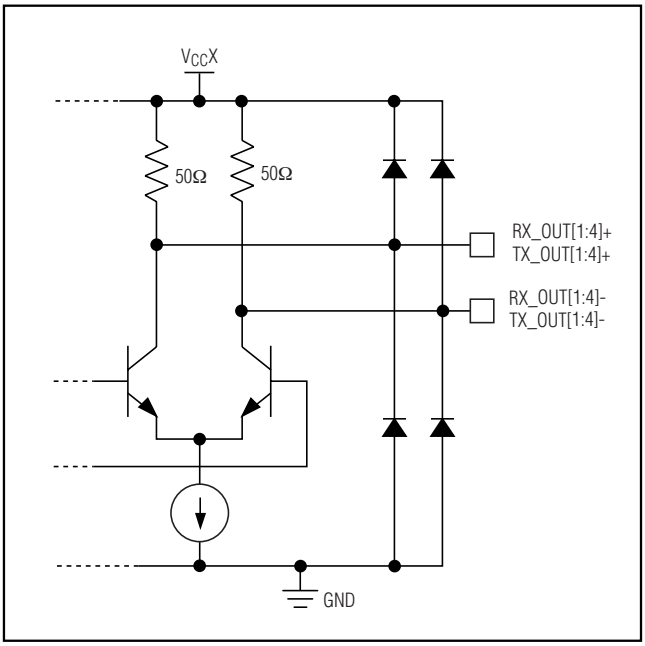
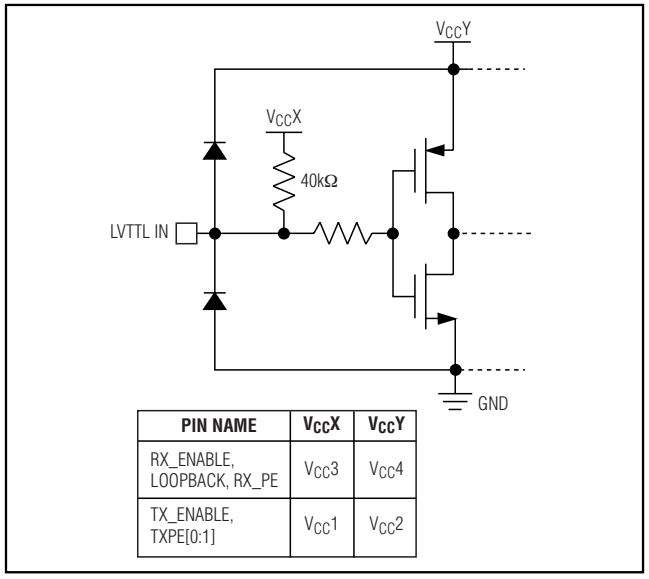


Figure 7. RX_OUT and TX_OUT Equivalent Output Structure

Quad Copper-Cable Signal Conditioner



PIN NAME	$V_{CC}X$	$V_{CC}Y$
RX_ENABLE, LOOPBACK, RX_PE	$V_{CC}3$	$V_{CC}4$
TX_ENABLE, TXPE[0:1]	$V_{CC}1$	$V_{CC}2$

Figure 8. LVTTL Equivalent Input Structure

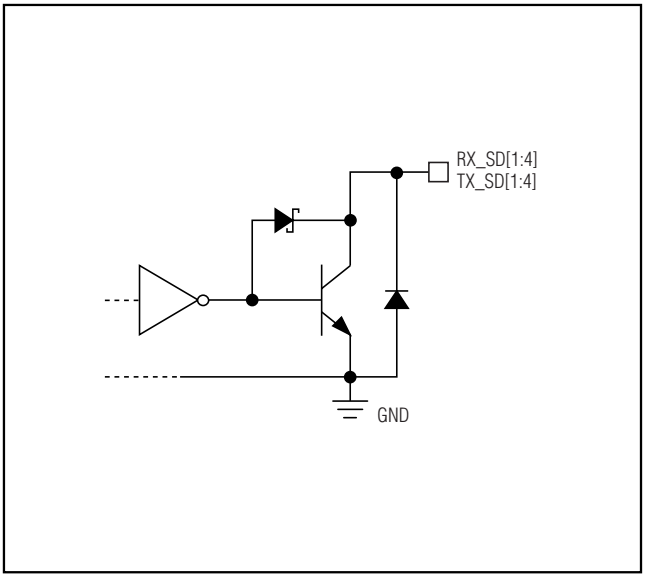
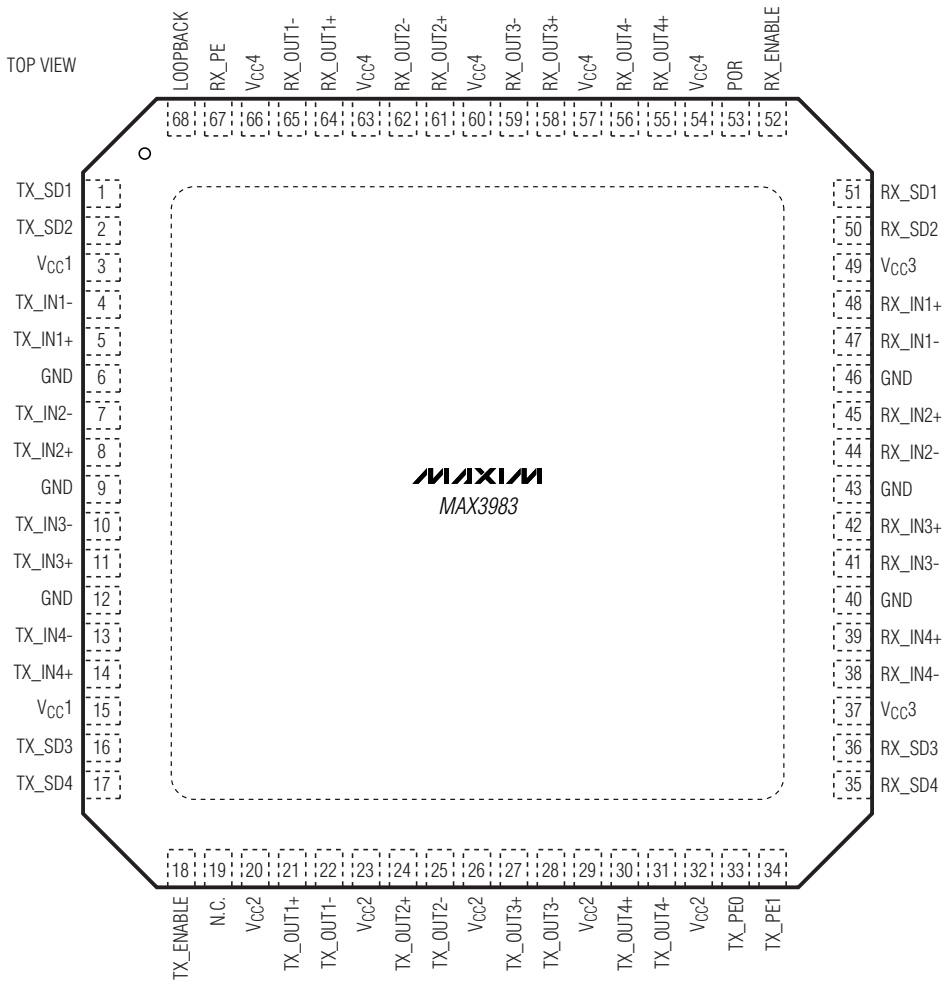


Figure 9. Signal-Detect Equivalent Output Structure

Pin Configuration



68 QFN*

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION OF THE MAX3983.

Chip Information

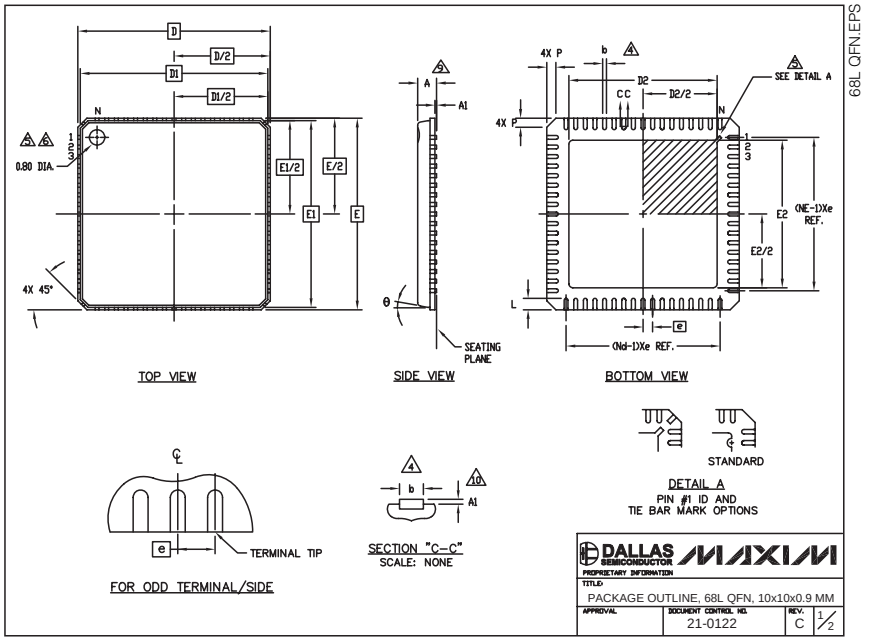
TRANSISTOR COUNT: 7493

PROCESS: SiGe Bipolar

Quad Copper-Cable Signal Conditioner

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM
21-0122
C
1/2

Revision History

Rev 0;	7/03:	Initial data sheet release.
Rev 1;	2/07:	Added lead-free package to Ordering Information table (page 1).

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX3983UGK+D MAX3983UGK+TD