19-1718; Rev 3; 1/09

Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

General Description

The MAX5383/MAX5384/MAX5385 low-cost, 8-bit digital-to-analog converters (DACs) in miniature 6-pin SOT23 packages have a simple 3-wire, SPI™/QSPI™/MICROWIRE™-compatible serial interface that operates up to 10MHz. The MAX5383 has an internal +2V reference and operates from a +2.7V to +3.6V supply. The MAX5384 has an internal +4V reference and operates from a +4.5V to +5.5V supply. The MAX5385 operates over the full +2.7V to +5.5V supply range and has an internal reference equal to 0.9 × V_{DD}.

The MAX5383/MAX5384/MAX5385 require an extremely low supply current of only 150µA (typ) and provide a buffered voltage output. These devices power up at zero code and remain there until a new code is written to the DAC registers. This provides additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5383/MAX5384/MAX5385 include a 1µA, low-power shutdown mode that features software-selectable output loads of 1kΩ, 100kΩ, or 1MΩ to ground.

Applications

Automatic Tuning (VCO)

Power Amplifier Bias Control

Programmable Threshold Levels

Automatic Gain Control

Automatic Offset Adjustment

SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **8-Bit Resolution in a Miniature 6-Pin SOT23 Package**
- **Wide +2.7V to +5.5V Supply Range (MAX5385)**
- **<1µA Shutdown Mode**
- **Software-Selectable Output Resistance During Shutdown**
- **Buffered Output Drives Resistive Loads**
- **Low-Glitch Power-On Reset to Zero DAC Output**
- **3-Wire SPI/QSPI/MICROWIRE-Compatible Interface**
- **< ±5% Full-Scale Error (MAX5385)**
- **< ±1LSB max INL/DNL**
- **Low 230µA (max) Supply Current**

Ordering Information

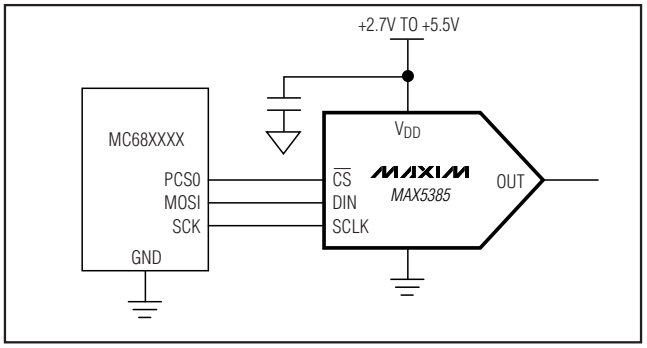
PART	TEMP RANGE	PIN-PACKAGE	SOT TOP MARK
MAX5383EUT+T	-40°C to +85°C	6 SOT23	AADF
MAX5383EZT+T	-40°C to +85°C	6 SOT23-Thin	AAAH
MAX5384EUT+T	-40°C to +85°C	6 SOT23	AADH
MAX5384EZT+T	-40°C to +85°C	6 SOT23-Thin	AAAI
MAX5385EUT+T	-40°C to +85°C	6 SOT23	AADJ
MAX5385EZT+T	-40°C to +85°C	6 SOT23-Thin	AAAJ

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

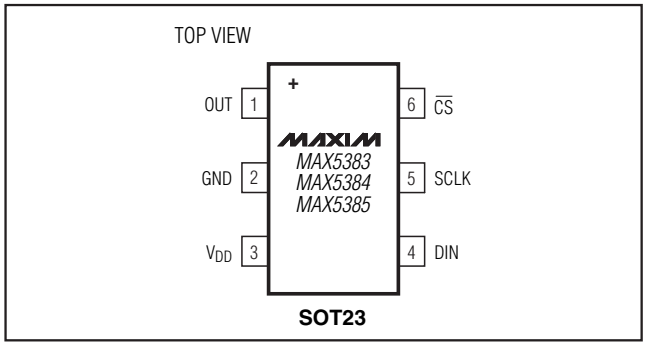
Selector Guide

PART	INTERNAL REFERENCE
MAX5383	2V
MAX5384	4V
MAX5385	0.9 × V_{DD}

Typical Operating Circuit



Pin Configuration



Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
$\overline{OUT}$ .....-0.3V to (V_{DD} + 0.3V)
$\overline{CS}$, SCLK, DIN to GND .....-0.3V to +6V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX5383), V_{DD} = +4.5V to +5.5V (MAX5384), V_{DD} = +2.7V to +5.5V (MAX5385), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Integral Linearity Error	INL	(Note 1)				±1	LSB
Differential Linearity Error	DNL	Guaranteed monotonic				±1	LSB
Offset Error	V_{OS}	(Note 2)			±1	±25	mV
Offset Error Supply Rejection		MAX5385 (Notes 2, 3)				60	dB
Offset Error Temperature Coefficient		MAX5383/MAX5384			3		ppm/°C
		MAX5385			1		
Full-Scale Error		Code = 255, no load	MAX5383/MAX5384			10	% of ideal FS
			MAX5385			5	
Full-Scale Error Supply Rejection		Code = 255 (Note 4)	MAX5383/MAX5384			50	dB
Full-Scale Error Temperature Coefficient		Code = 255	MAX5383/MAX5384		±40		ppm/°C
			MAX5385		±10		
DAC OUTPUT							
Internal Reference Voltage (Note 5)	REF	MAX5383		1.8	2	2.2	V
		MAX5384		3.6	4	4.4	
		MAX5385		0.85 × V_{DD}	0.9 × V_{DD}	0.95 × V_{DD}	
Output Load Regulation		Code = 255, 0µA to 100µA			0.5		LSB
		Code = 0, 0µA to 100µA			0.5		
Shutdown Output Resistance to GND		V_{OUT} = 0 to V_{DD}	[D13, D12] = 0, 1		1k		Ω
			[D13, D12] = 1, 0		100k		
			[D13, D12] = 1, 1		1M		
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		Positive and negative			0.4		V/µs
Output Settling Time		To 1/2 LSB, 50kΩ and 50pF load (Note 6)			20		µs
Digital Feedthrough		Code = 0, all digital inputs from 0 to V_{DD}			2		nVs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX5383), V_{DD} = +4.5V to +5.5V (MAX5384), V_{DD} = +2.7V to +5.5V (MAX5385), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-Analog Glitch Impulse		Code 127 to 128		40		nVs
Wake-Up Time		From software shutdown		50		µs
POWER REQUIREMENTS						
Supply Voltage	V_{DD}	MAX5383	2.7		3.6	V
		MAX5384	4.5		5.5	
		MAX5385	2.7		5.5	
Supply Current	I_{DD}	No load, all digital inputs at 0 or V_{DD}, code = 255		150	230	µA
		Shutdown mode			1	
DIGITAL INPUTS						
Input Low Voltage	V_{IL}				0.3 × V_{DD}	V
Input High Voltage	V_{IH}		0.7 × V_{DD}			V
Input Hysteresis	V_H			0.05 × V_{DD}		V
Input Capacitance	C_{IN}	(Note 7)		10		pF
Input Leakage Current	I_{IN}				±1	µA

TIMING CHARACTERISTICS

(Figures 3 and 4, V_{DD} = +2.7V to +3.6V (MAX5383), V_{DD} = +4.5V to +5.5V (MAX5384), V_{DD} = +2.7V to +5.5V (MAX5385), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns

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TIMING CHARACTERISTICS (continued)

(Figures 3 and 4, V_{DD} = +2.7V to +3.6V (MAX5383), V_{DD} = +4.5V to +5.5V (MAX5384), V_{DD} = +2.7V to +5.5V (MAX5385), R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C.) (Note 7)

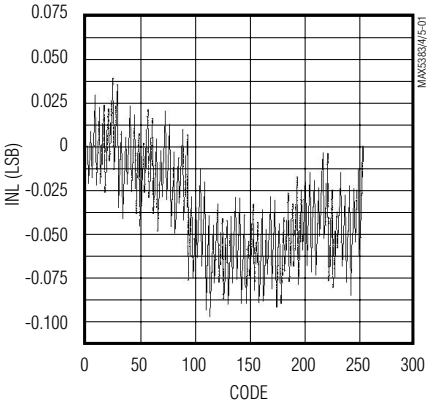
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Guaranteed from code 5 to code 255.
Note 2: The offset value extrapolated from the range over which the INL is guaranteed.
Note 3: MAX5385 tested at 5V ±10%.
Note 4: MAX5383 tested at 3V ±10%; MAX5384 tested at 5V ±10%.
Note 5: Actual output voltages at full-scale are 255/256 × V_{REF}.
Note 6: Output settling time is measured by stepping from code 5 to code 255, and from code 255 to code 5.
Note 7: Guaranteed by design.

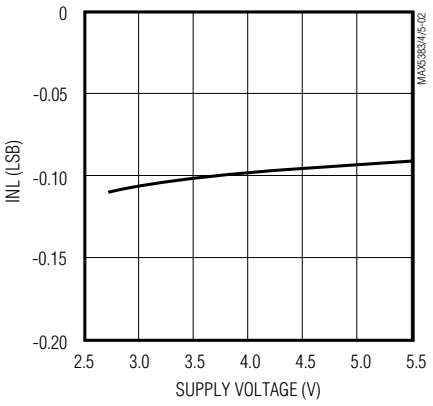
Typical Operating Characteristics

(V_{DD} = +3.0V (MAX5383), V_{DD} = +5.0V (MAX5384/MAX5385), T_A = +25°C, unless otherwise noted.)

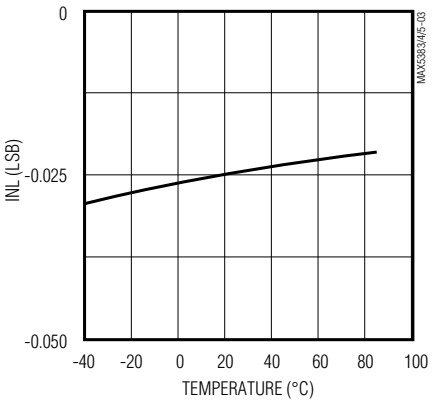
INTEGRAL NONLINEARITY vs. CODE



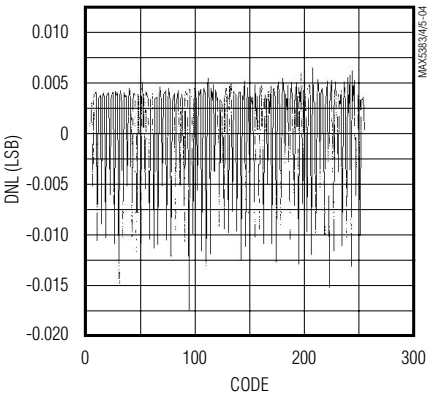
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



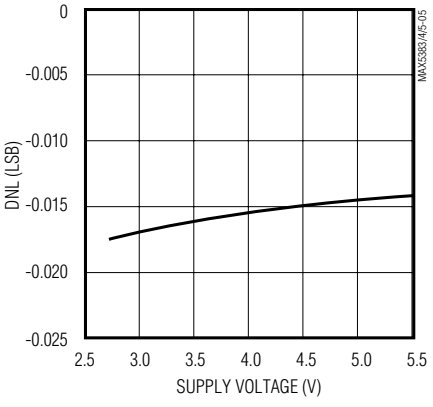
INTEGRAL NONLINEARITY vs. TEMPERATURE



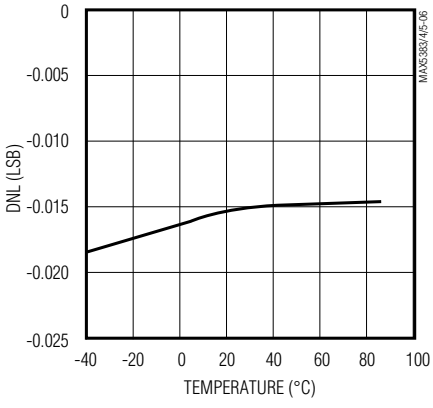
DIFFERENTIAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. SUPPLY VOLTAGE



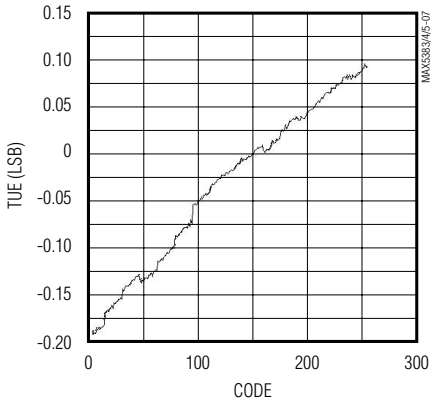
DIFFERENTIAL NONLINEARITY vs. TEMPERATURE



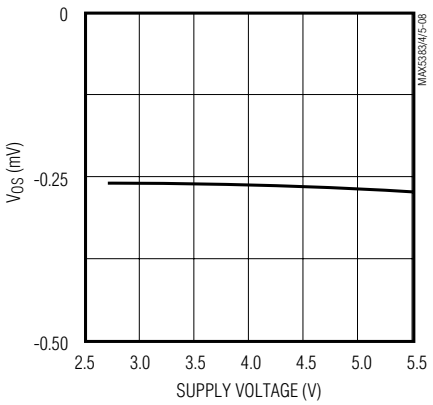
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5383), V_{DD} = +5.0V (MAX5384/MAX5385), T_A = +25°C, unless otherwise noted.)

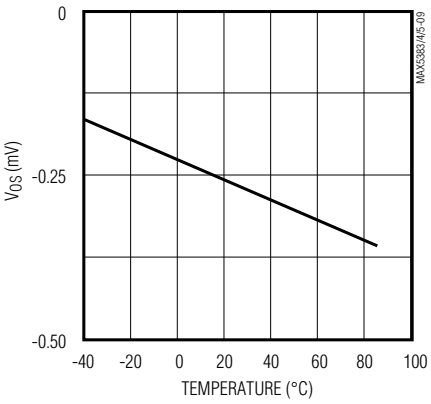
TOTAL UNADJUSTED ERROR vs. CODE



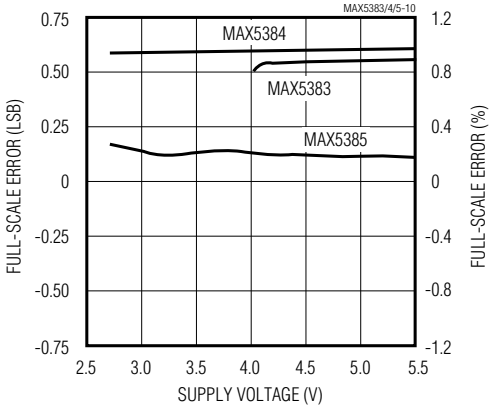
OFFSET ERROR vs. SUPPLY VOLTAGE



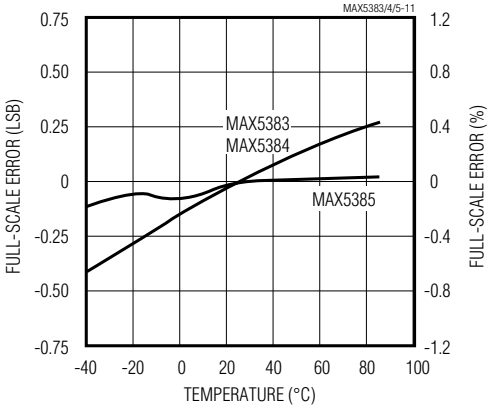
OFFSET ERROR vs. TEMPERATURE



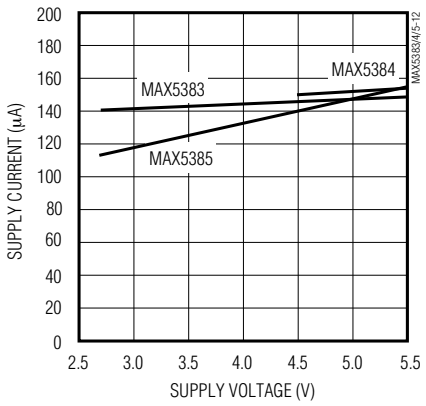
FULL-SCALE ERROR vs. SUPPLY VOLTAGE



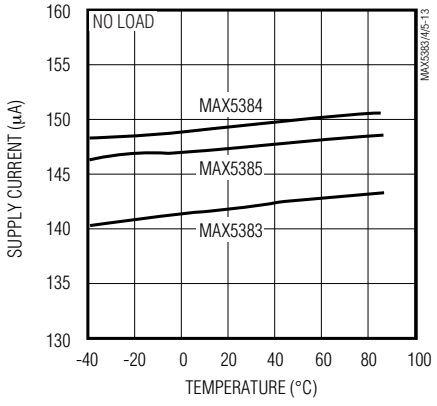
FULL-SCALE ERROR vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



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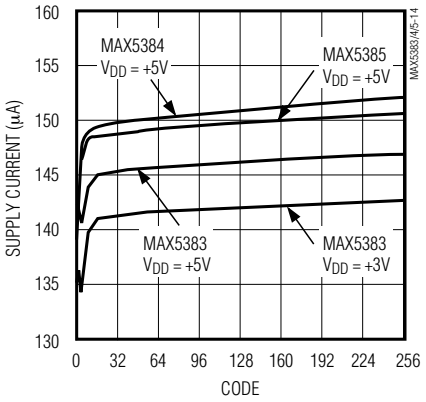
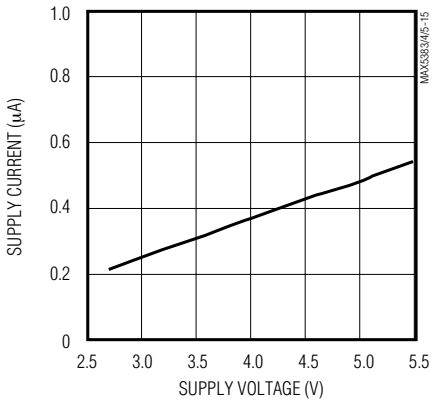
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5383), V_{DD} = +5.0V (MAX5384/MAX5385), T_A = +25°C, unless otherwise noted.)

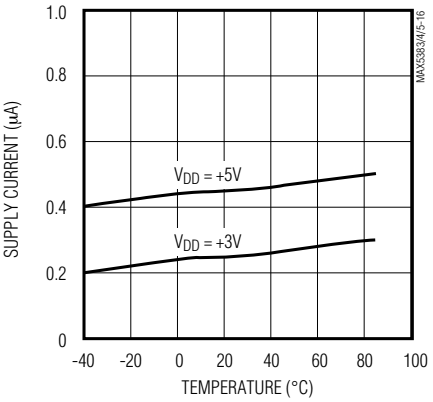
SUPPLY CURRENT vs. CODE



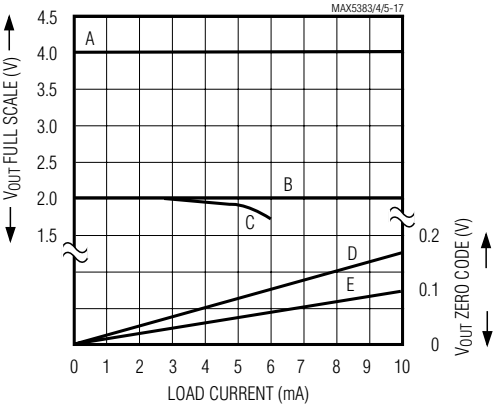
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

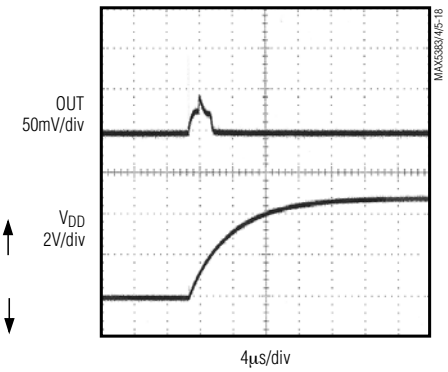


OUTPUT LOAD REGULATION

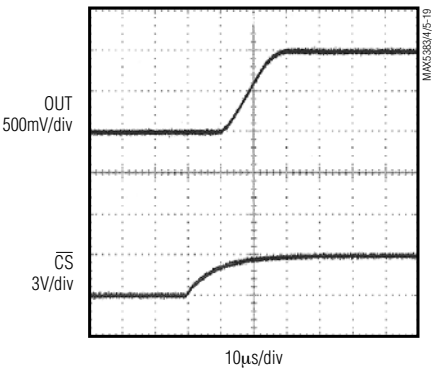


A: MAX5384/MAX5385, V_{DD} = +4.5V, FULL SCALE OR SOURCING
B: MAX5383, FULL SCALE, V_{DD} = +2.7V SINKING, V_{DD} = +5.0V SOURCING
C: MAX5383, FULL SCALE, V_{DD} = +2.7V SOURCING
D: ZERO CODE, V_{DD} = +2.7V SINKING
E: ZERO CODE, V_{DD} = +5.5V SINKING

OUTPUT VOLTAGE ON POWER-UP

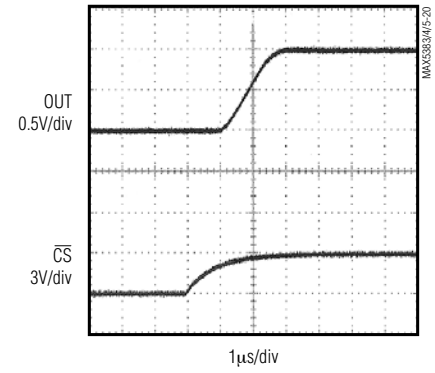


MAX5383 OUTPUT VOLTAGE EXITING SHUTDOWN

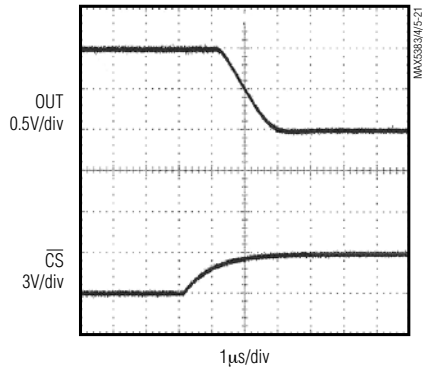


SHDN TO 0 x 80

MAX5383 OUTPUT SETTLING FROM 1/4FS TO 3/4FS



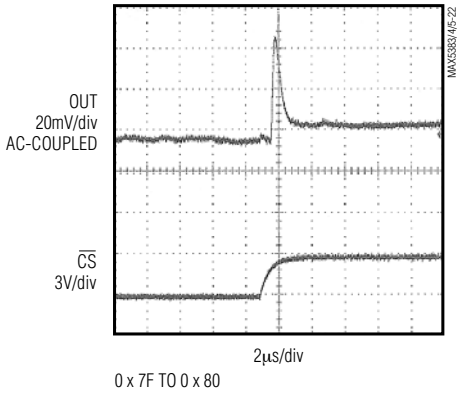
MAX5383 OUTPUT SETTLING FROM 3/4FS TO 1/4FS



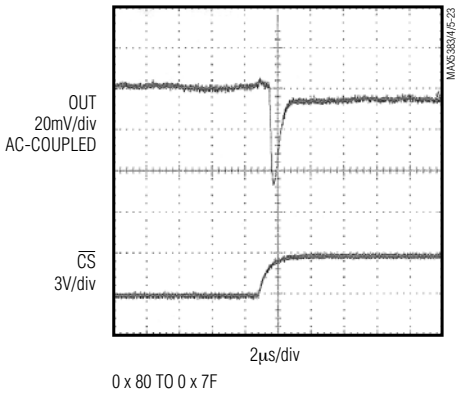
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V (MAX5383), V_{DD} = +5.0V (MAX5384/MAX5385), T_A = +25°C, unless otherwise noted.)

MAX5383
OUTPUT SETTLING
1LSB STEP UP



MAX5383
OUTPUT SETTLING
1LSB STEP DOWN



Pin Description

PIN	NAME	DESCRIPTION
1	OUT	DAC Voltage Output
2	GND	Ground
3	V_{DD}	Power-Supply Input
4	DIN	Serial Data Input
5	SCLK	Serial Clock Input
6	$\overline{CS}$	Chip-Select Input

Detailed Description

The MAX5383/MAX5384/MAX5385 voltage-output, 8-bit DACs ensure monotonic performance by offering full 8-bit performance with less than 1LSB integral nonlinearity error and less than 1LSB differential nonlinearity error. The devices use a simple 3-wire, SPI/QSPI/MICROWIRE-compatible serial interface that operates up to 10MHz. They include an internal reference, an output buffer, and three low-current shutdown modes, making these devices ideal for low-power, highly integrated applications. Figure 1 shows the devices' functional diagram.

Analog Section

The MAX5383/MAX5384/MAX5385 employ a current-steering DAC topology as shown in Figure 2. At the core of the DAC is a reference voltage-to-current converter (V/I) that generates a reference current. This current is mirrored to 255 equally weighted current sources. DAC switches control the outputs of these current mirrors so that only the desired fraction of the total current-mirror currents is steered to the DAC output. The current is then converted to a voltage across a resistor, and this voltage is buffered by the output buffer amplifier.

Output Voltage

Table 1 shows the relationship between the DAC code and the analog output voltage. The 8-bit DAC code is binary unipolar with 1LSB = (V_{REF}/256). The MAX5383/MAX5384 have a full-scale output voltage of (+2V - 1LSB) and (+4V - 1LSB), set by the internal references. The MAX5385 has a full-scale output voltage of (0.9 × V_{DD} - 1LSB).

Output Buffer

The DAC voltage output is an internally buffered unity-gain follower that slews up to ±0.4V/µs. The output can swing from 0 to full scale. With a 1/4FS to 3/4FS output transition, the amplifier outputs typically settle to 1/2LSB in less than 5µs when loaded with 10kΩ in parallel with 50pF. The buffer amplifiers are stable with any

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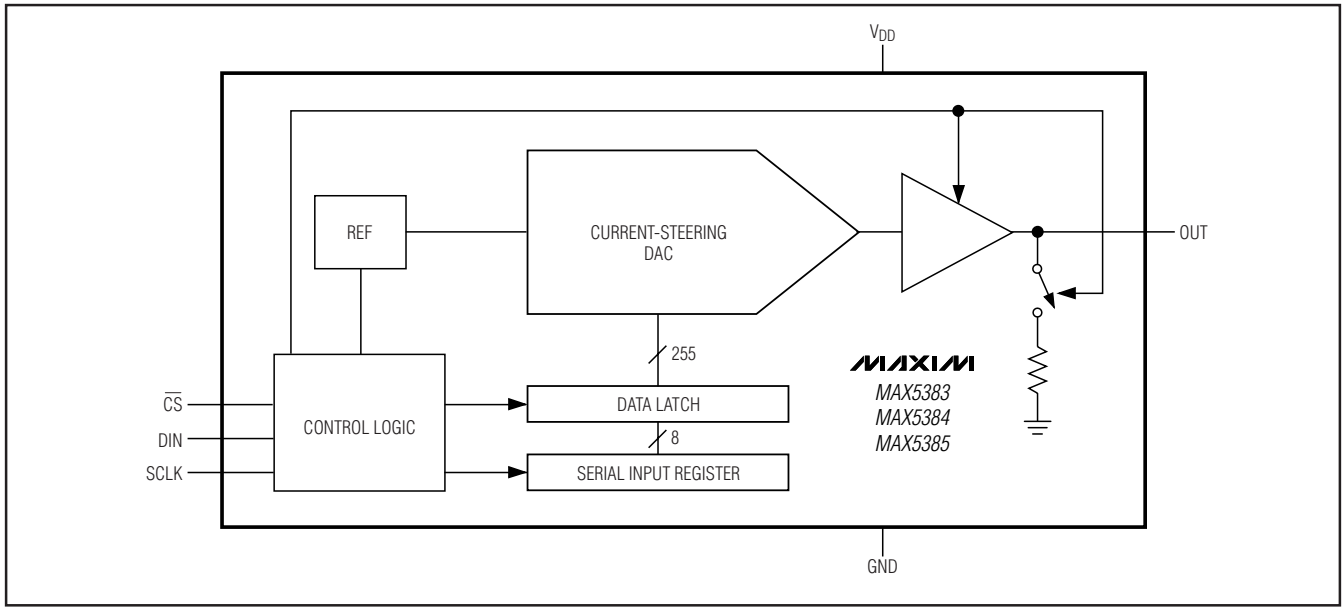


Figure 1. Functional Diagram

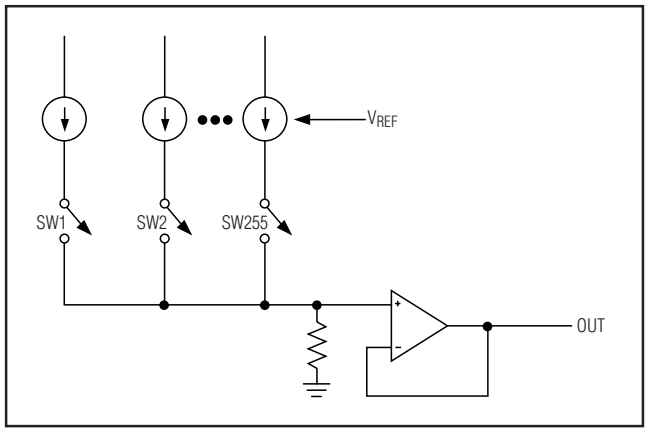


Figure 2. Current-Steering DAC Topology

Table 1. Unipolar Code Output Voltage

DAC CODE [D11–D4]	OUTPUT VOLTAGE		
	MAX5383	MAX5384	MAX5385
1111 1111	2V × (255/256)	4V × (255/256)	0.9 × V_{DD} × (255/256)
1000 0000	1V	2V	0.9 × V_{DD} / 2
0000 0001	7.8mV	15.6mV	0.9 × V_{DD} / 256
0000 0000	0	0	0

combination of resistive loads >10kΩ and capacitive loads <50pF.

Power-On Reset

The MAX5383/MAX5384/MAX5385 have a power-on reset circuit to set the DAC's output to 0 when V_{DD} is first applied or when V_{DD} dips below 1.7V (typ). This ensures that unwanted DAC output voltages will not occur immediately following a system startup, such as after a loss of power. The output glitch on startup is typically less than 50mV.

Shutdown Mode

The MAX5383/MAX5384/MAX5385 include three software-controlled shutdown modes that reduce the supply current to <1µA. All internal circuitry is disabled, and a known impedance is placed from OUT to GND to ensure 0V while in shutdown. Table 2 details the three shutdown modes of operation.

Digital Section

3-Wire Serial Interface

The MAX5383/MAX5384/MAX5385s' digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data-input pin (DIN). Immediately following $\overline{CS}$'s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial

input register, it transfers its contents to the DAC latch on $\overline{CS}$'s low-to-high transition (Figure 3). Note that if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word. The serial clock (SCLK) can idle either high or low between transitions. Figure 4 shows the complete 3-wire serial interface transmission. Table 3 lists serial interface mapping.

Applications Information

Device Powered by an External Reference

Since the MAX5385 generates an output voltage proportional to V_{DD}, a noisy power supply will affect the accuracy of the on-board reference, thereby affecting the overall accuracy of the DAC. The circuit in Figure 5 rejects this power-supply noise by powering the device directly with a precision voltage reference, improving overall system accuracy. The MAX6103 (+3V, 75ppm) or the MAX6105 (+5V, 75ppm) precision voltage references are ideal choices due to the low power requirements of the MAX5385. This solution is also useful when the required full-scale output voltage is different from the available supply voltages.

Digital Inputs and Interface Logic

The digital interface for the 8-bit DAC is based on a 3-wire standard that is compatible with SPI, QSPI, and MICROWIRE interfaces. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input serially into the DAC.

All the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5383/MAX5384/MAX5385 without additional external logic. The digital inputs are compatible with CMOS logic levels and can be driven with voltages up to +5.5V regardless of the supply voltage.

Power-Supply Bypassing and Layout

Careful PC board layout is important for best system performance. To reduce crosstalk and noise injection, keep analog and digital signals separate. To ensure that the ground return from GND to the supply ground is short and low impedance, a ground plane is recommended. Bypass V_{DD} with a 0.1µF capacitor to ground as close as possible to the device. If the supply is excessively noisy, connect a 10Ω resistor in series with the supply and V_{DD} and add additional capacitance.

Table 2. Shutdown Modes

DAC CODE [D13 AND D12]	MODE	OUTPUT RESISTANCE TO GROUND (Ω)	MAXIMUM SUPPLY CURRENT (µA)
01	Shutdown	1k	1
10	Shutdown	100k	1
11	Shutdown	1M	1

Table 3. Serial Interface Mapping

16-BIT SERIAL WORD				ANALOG OUTPUT	FUNCTION
MSB			LSB		
XX00	0000	0000	XXXX	0V	Normal operation
XX00	1111	1111	XXXX	$V_{REF} \times (255/256)$	Normal operation
XX00	0000	0001	XXXX	$V_{REF} \times (1/256)$	Normal operation
XX00	1000	0000	XXXX	$V_{REF} \times (128/256)$	Normal operation
XX01	XXXX	XXXX	XXXX	0V	Shutdown, 1kΩ to GND
XX10	XXXX	XXXX	XXXX	0V	Shutdown, 100kΩ to GND
XX11	XXXX	XXXX	XXXX	0V	Shutdown, 1MΩ to GND

X = Don't care

Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

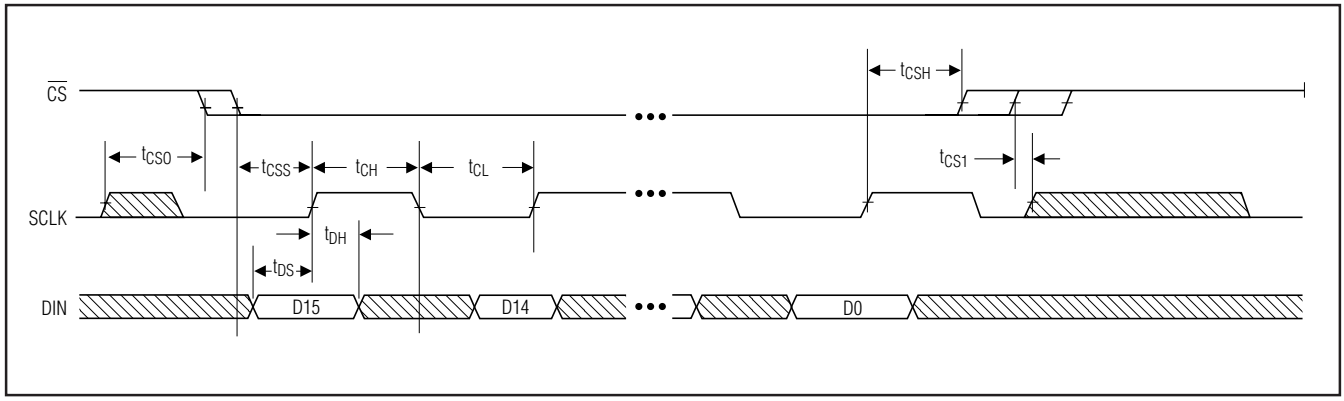


Figure 3. 3-Wire Serial Interface Timing Diagram

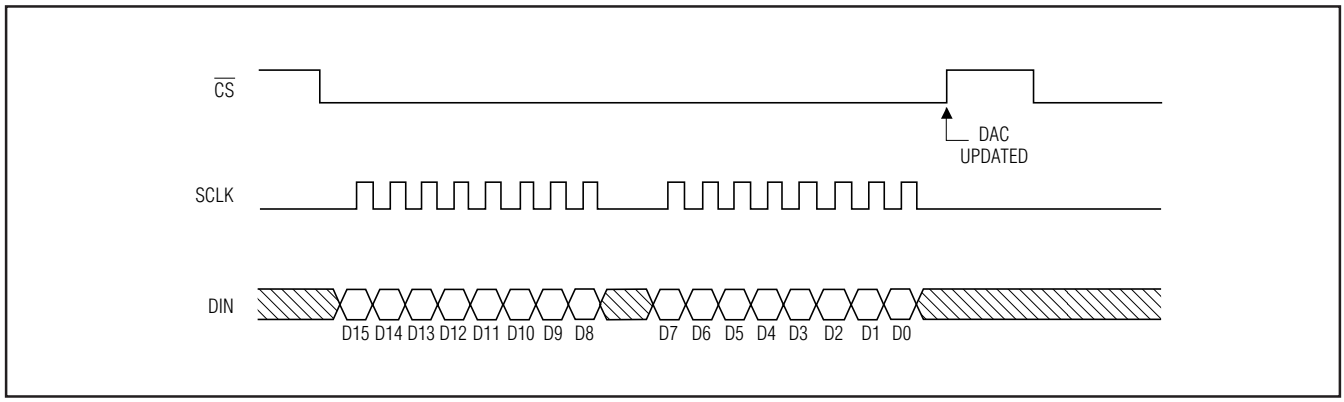


Figure 4. Complete 3-Wire Serial Interface Transmission

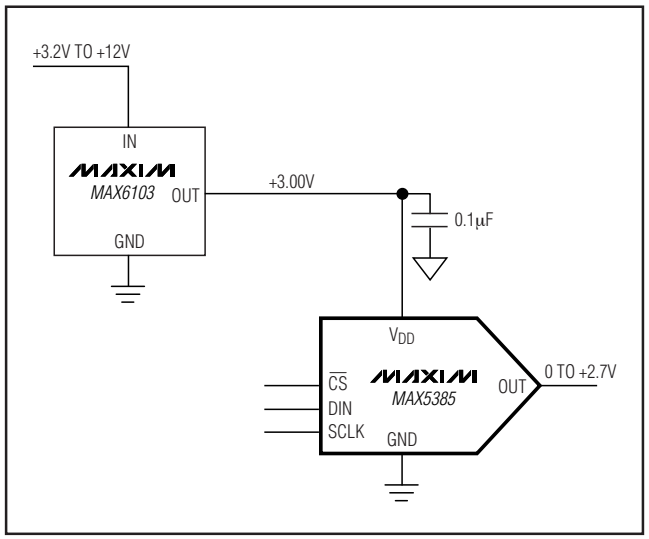


Figure 5. Powering the MAX5385 with a Precision Voltage Reference

Chip Information

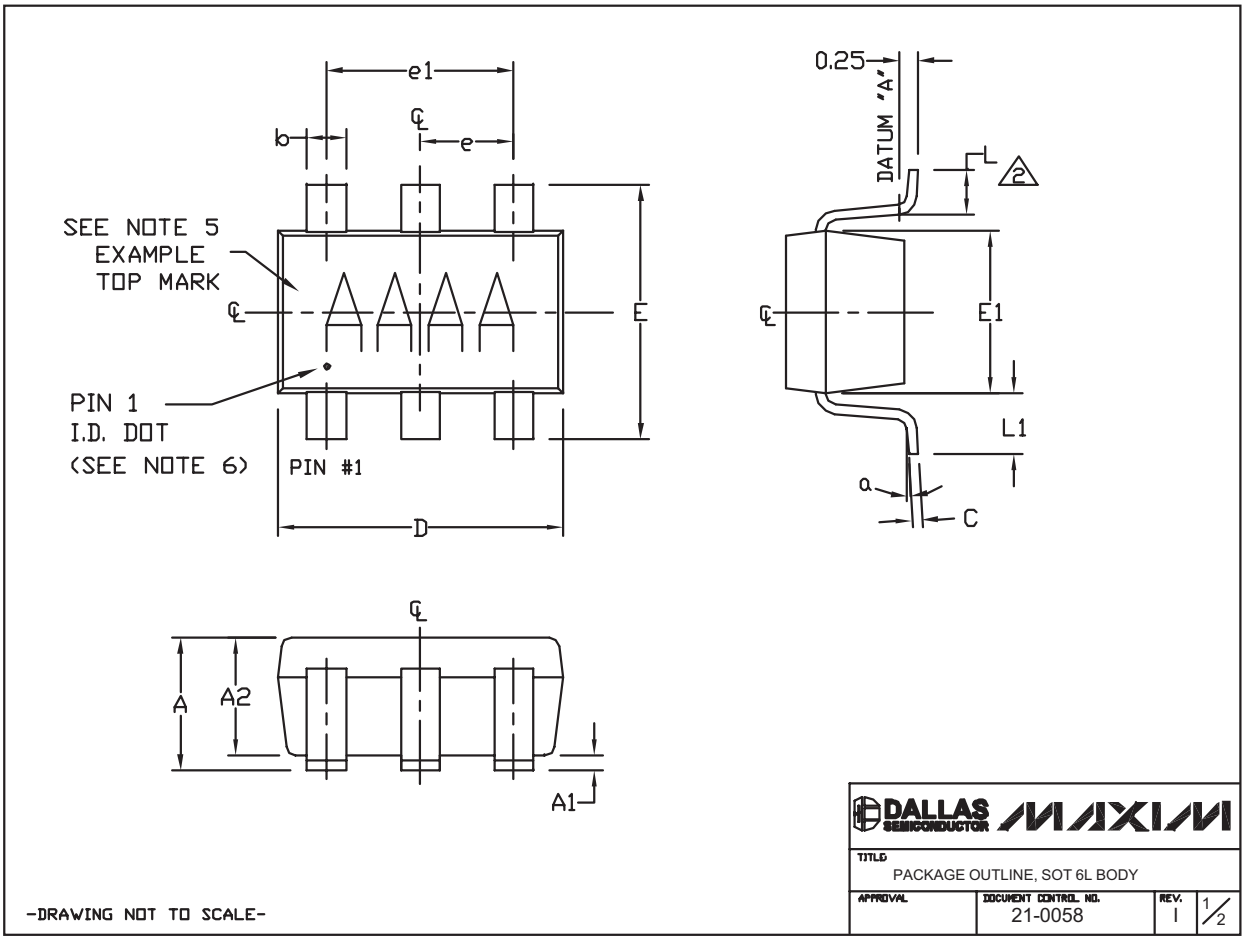
TRANSISTOR COUNT: 2160

Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SOT23	U6-4	21-0058
6 SOT23-Thin	Z6-1	21-0114



Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3mm ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6C-8, U6SN-1, U6CN-2, U6S-3, U6F-5, U6F-6, U6FH-5, U6FH-6

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

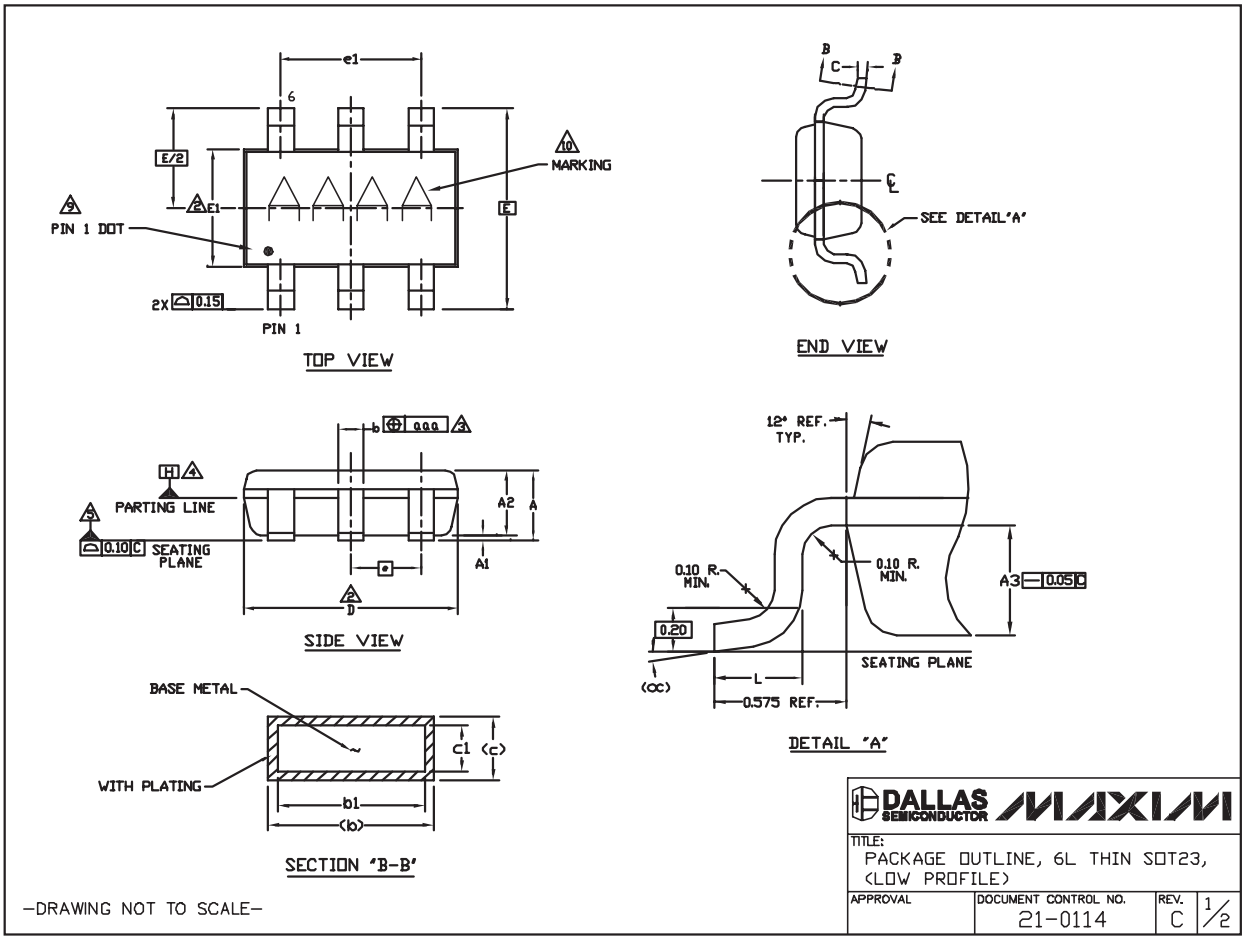
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	I	2/2

Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

6L THIN SOT23.EPS



Low-Cost, Low-Power, 8-Bit DACs with 3-Wire Serial Interface in SOT23

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3		0.50 BSC	
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
∝	0°	4°	8°
aaa		0.20	
Pkg. codes: Z6-1, Z6-2			

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L THIN SOT23, (LOW PROFILE)

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0114	C	2/2

-DRAWING NOT TO SCALE-

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	1/09	Added lead-free designation to parts in the *Ordering Information* and added 21-0058 package diagram	1, 11

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX5383EZT+T MAX5384EUT+T MAX5383EUT+T MAX5385EUT+T MAX5384EZT+T MAX5385EZT+T