19-3371; Rev 0; 7/04

EVALUATION KIT AVAILABLE

256-Tap, Nonvolatile, SPI-Interface, Digital Potentiometers

General Description

The MAX5422/MAX5423/MAX5424 nonvolatile, linear-taper, digital potentiometers perform the function of a mechanical potentiometer, but replace the mechanics with a simple 3-wire SPI™-compatible digital interface. Each device performs the same function as a discrete potentiometer or variable resistor and has 256 tap points.

The devices feature an internal, nonvolatile EEPROM used to store the wiper position for initialization during power-up. The 3-wire SPI-compatible serial interface allows communication at data rates up to 5MHz, minimizing board space and reducing interconnection complexity in many applications.

The MAX5422/MAX5423/MAX5424 provide three nominal resistance values: 50kΩ (MAX5422), 100kΩ (MAX5423), or 200kΩ (MAX5424). The nominal resistor temperature coefficient is 35ppm/°C end-to-end and only 5ppm/°C ratiometric. This makes the devices ideal for applications requiring a low-temperature-coefficient variable resistor, such as low-drift, programmable gain-amplifier circuit configurations.

The MAX5422/MAX5423/MAX5424 are available in a 3mm x 3mm 8-pin TDFN package, and are specified over the extended -40°C to +85°C temperature range.

Applications

Mechanical Potentiometer Replacement

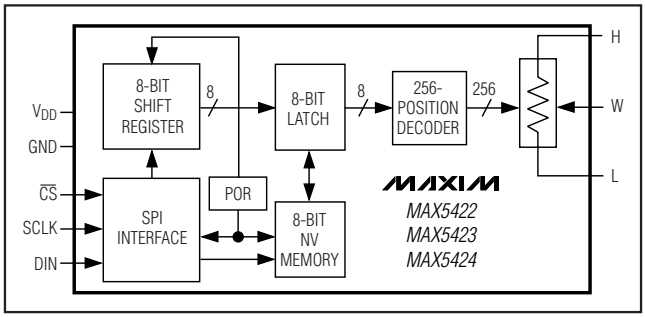
Low-Drift Programmable Gain Amplifiers

Audio Volume Control

Liquid-Crystal Display (LCD) Contrast Control

Low-Drift Programmable Filters

Functional Diagram

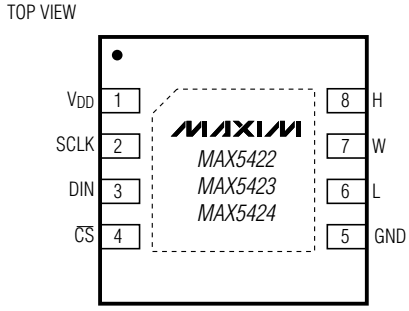


Features

- **Wiper Position Stored in Nonvolatile Memory (EEPROM) and Recalled Upon Power-Up or Interface Command**
- **3mm x 3mm x 0.8mm TDFN Package**
- **35ppm/°C End-to-End Resistance Temperature Coefficient**
- **5ppm/°C Ratiometric Temperature Coefficient**
- **50kΩ, 100kΩ, and 200kΩ Resistor Values**
- **5MHz SPI-Compatible Serial Interface**
- **500nA (typ) Static Supply Current**
- **Single-Supply Operation: +2.7V to +5.25V**
- **256 Tap Positions**
- **±0.5 LSB DNL in Voltage-Divider Mode**
- **±0.5 LSB INL in Voltage-Divider Mode**

SPI is a trademark of Motorola, Inc.

Pin Configuration



TDFN (3mm x 3mm)

Ordering Information/Selector Guide

PART	TEMP RANGE	END-TO-END RESISTANCE (kΩ)	PIN-PACKAGE	TOP MARK
MAX5422ETA	-40°C to +85°C	50	8 TDFN-EP*	AIJ
MAX5423ETA	-40°C to +85°C	100	8 TDFN-EP*	AII
MAX5424ETA	-40°C to +85°C	200	8 TDFN-EP*	AIH

**EP = Exposed pad.*

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6.0V
All Other Pins to GND.....-0.3V to (V_{DD} + 0.3V)
Maximum Continuous Current into H, L, and W
MAX5422.....±1.3mA
MAX5423.....±0.6mA
MAX5424.....±0.3mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (VOLTAGE-DIVIDER MODE)						
Resolution	N		256			Taps
Integral Nonlinearity	INL	(Note 1)			±0.5	LSB
Differential Nonlinearity	DNL	(Note 1)			±0.5	LSB
End-to-End Resistance Temperature Coefficient	TC_R			35		ppm/°C
Ratiometric Resistance Temperature Coefficient				5		ppm/°C
Full-Scale Error		MAX5422		-0.6		LSB
		MAX5423		-0.3		
		MAX5424		-0.15		
Zero-Scale Error		MAX5422		0.7		LSB
		MAX5423		0.35		
		MAX5424		0.18		
DC PERFORMANCE (VARIABLE-RESISTOR MODE)						
Integral Nonlinearity (Note 2)	INL	V_{DD} = 3V			±3.0	LSB
		V_{DD} = 5V			±1.5	
Differential Nonlinearity (Note 2)	DNL	V_{DD} = 3V, MAX5422, -40°C ≤ T_A ≤ +85°C, guaranteed monotonic	-1.0		+2.0	LSB
		V_{DD} = 3V, MAX5422, 0°C ≤ T_A ≤ +85°C, guaranteed monotonic	-1.0		+1.2	
		V_{DD} = 3V, MAX5423			±1.0	
		V_{DD} = 3V, MAX5424			±1.0	
		V_{DD} = 5V			±1.0	
DC PERFORMANCE (RESISTOR CHARACTERISTICS)						
Wiper Resistance	R_W	V_{DD} = 3V to 5.25V (Note 3)		325	675	Ω
Wiper Capacitance	C_W			10		pF
End-to-End Resistance		MAX5422	37.5	50	62.5	kΩ
		MAX5423	75	100	125	
		MAX5424	150	200	250	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS ($\overline{CS}$, DIN, SCLK)						
Input High Voltage (Note 4)	V_{IH}	V_{DD} = 3.4V to 5.25V	2.4			V
		V_{DD} < 3.4V	0.7 x V_{DD}			
Input Low Voltage	V_{IL}	V_{DD} = 2.7V to 5.25V (Note 4)			0.8	V
Input Leakage Current	I_{IN}			±0.1	±1	µA
Input Capacitance	C_{IN}			5		pF
DYNAMIC CHARACTERISTICS						
Wiper -3dB Bandwidth (Note 5)		MAX5422		100		kHz
		MAX5423		50		
		MAX5424		25		
NONVOLATILE MEMORY RELIABILITY						
Data Retention		T_A = +85°C		50		Years
Endurance		T_A = +25°C		200,000		Stores
		T_A = +85°C		50,000		
POWER SUPPLY						
Supply Voltage	V_{DD}		2.70		5.25	V
Standby Current	I_{DD}	Digital inputs = V_{DD} or GND, T_A = +25°C		0.5	1	µA
Programming Current	I_{PG}	During nonvolatile write to memory; digital inputs = V_{DD} or GND (Note 6)		200	400	µA

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted. See Figure 1.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SECTION						
Wiper Settling Time (Note 8)	t_S	MAX5422		400		ns
		MAX5423		600		
		MAX5424		1000		
DIGITAL SECTION						
SCLK Frequency	f_{SCLK}				5	MHz
SCLK Clock Period	t_{CP}		200			ns
SCLK Pulse-Width High	t_{CH}		80			ns
SCLK Pulse-Width Low	t_{CL}		80			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		80			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
DIN to SCLK Setup	t_{DS}		50			ns

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TIMING CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{DD} = +5.0V, T_A = +25°C, unless otherwise noted. See Figure 1.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN Hold after SCLK	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		20			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		80			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		200			ns
Write NV Register Busy Time	t_{BUSY}				12	ms

Note 1: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H = V_{DD} and L = GND. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

Note 2: The DNL and INL are measured with the potentiometer configured as a variable resistor. H is unconnected and L = GND. For the 5V condition, the wiper terminal is driven with a source current of 80µA for the 50kΩ configuration, 40µA for the 100kΩ configuration, and 20µA for the 200kΩ configuration. For the 3V condition, the wiper terminal is driven with a source current of 40µA for the 50kΩ configuration, 20µA for the 100kΩ, and 10µA for the 200kΩ configuration.

Note 3: The wiper resistance is measured using the source currents given in Note 2. For operation to V_{DD} = 2.7V, see Maximum Wiper Resistance vs. Temperature in the *Typical Operating Characteristics*.

Note 4: The device draws higher supply current when the digital inputs are driven with voltages between (V_{DD} - 0.5V) and (GND + 0.5V). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.

Note 5: Wiper at midscale with a 10pF load (DC measurement). L = GND; an AC source is applied to H; and the W output is measured. A 3dB bandwidth occurs when the AC W/H value is 3dB lower than the DC W/H value.

Note 6: The programming current operates only during power-up and NV writes.

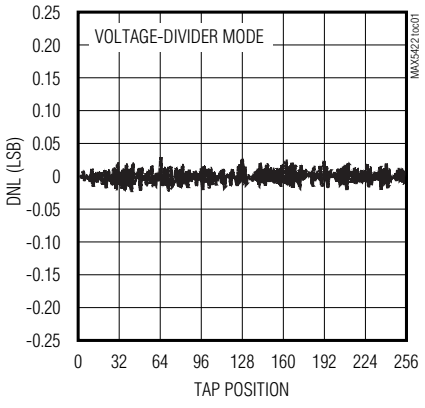
Note 7: Digital timing is guaranteed by design and characterization, and is not production tested.

Note 8: Wiper-settling time is the worst-case 0% to 50% rise-time measured between consecutive wiper positions. H = V_{DD}, L = GND, and the wiper terminal is unloaded and measured with a 10pF oscilloscope probe.

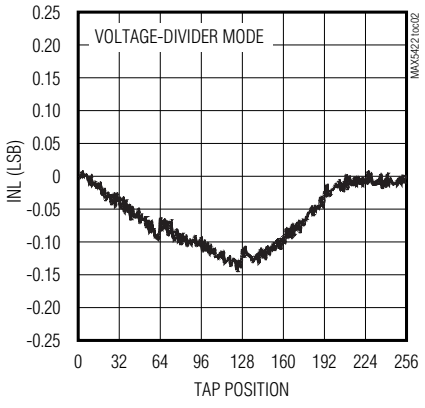
Typical Operating Characteristics

(V_{DD} = 5.0V, T_A = +25°C, unless otherwise noted.)

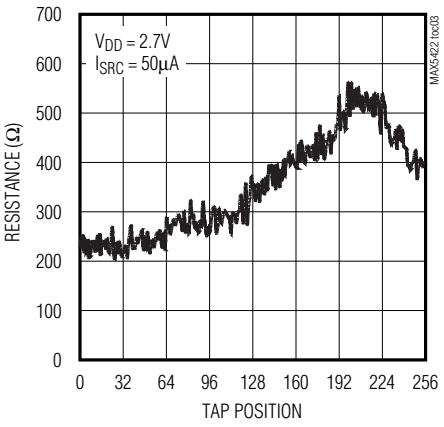
DNL vs. TAP POSITION



INL vs. TAP POSITION



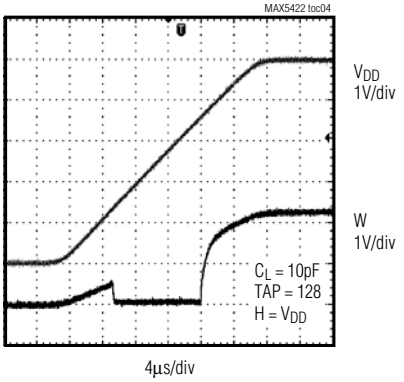
WIPER RESISTANCE vs. TAP POSITION



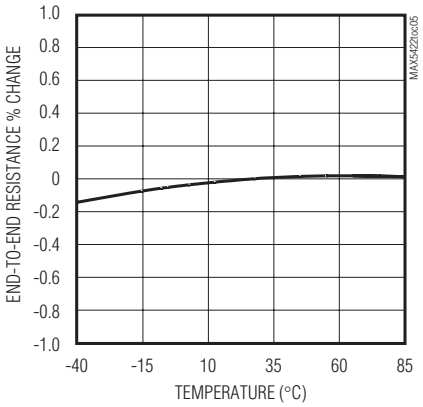
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, T_A = +25°C, unless otherwise noted.)

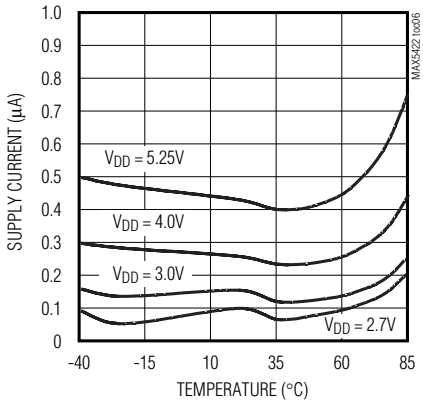
WIPER TRANSIENT AT POWER-ON



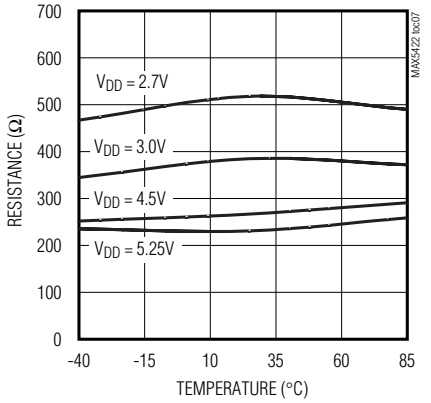
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



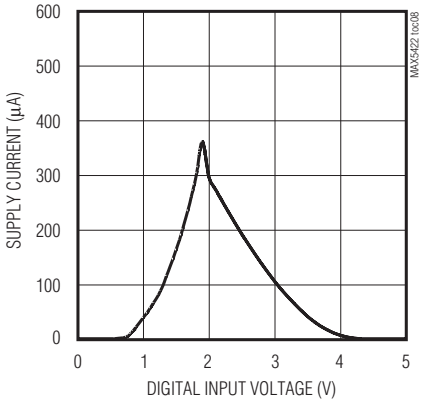
STANDBY SUPPLY CURRENT vs. TEMPERATURE



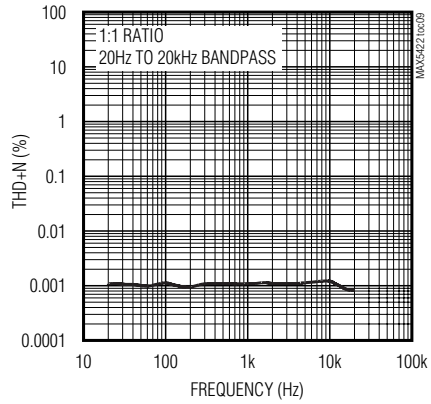
MAXIMUM WIPER RESISTANCE vs. TEMPERATURE



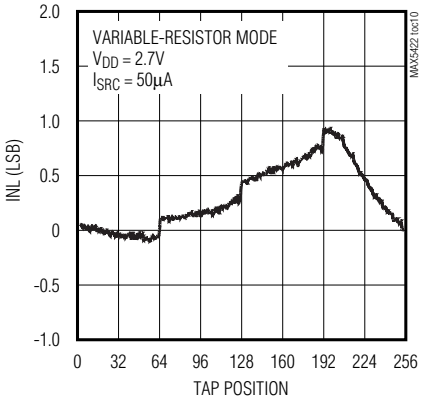
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



THD+N RESPONSE



INL vs. TAP POSITION (MAX5422)



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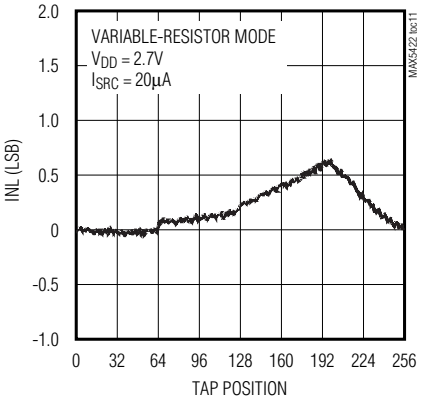
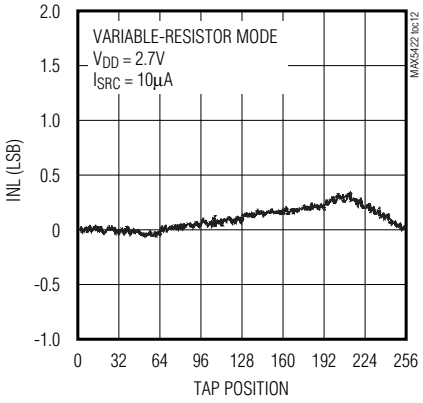
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, T_A = +25°C, unless otherwise noted.)

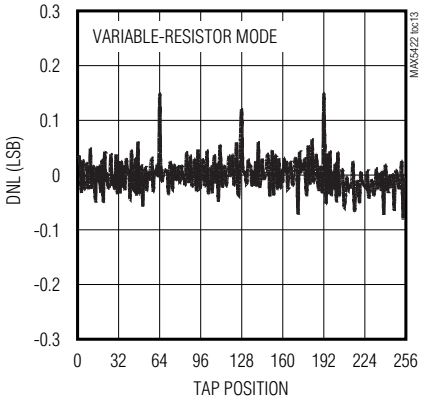
INL vs. TAP POSITION (MAX5423)



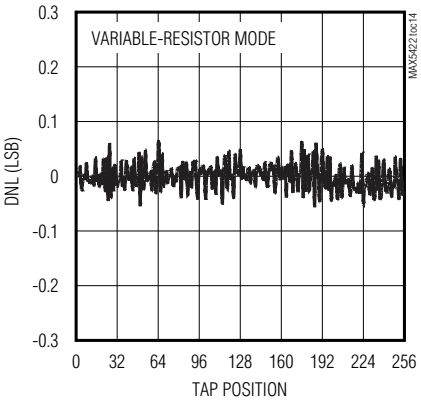
INL vs. TAP POSITION (MAX5424)



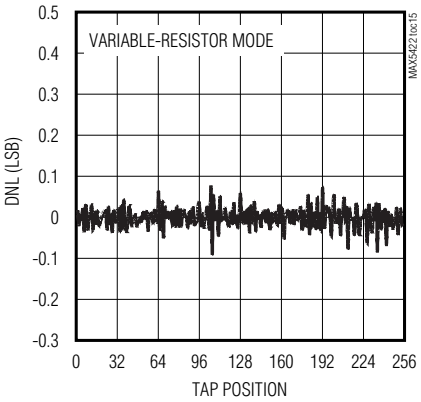
DNL vs. TAP POSITION (MAX5422)



DNL vs. TAP POSITION (MAX5423)



DNL vs. TAP POSITION (MAX5424)



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power-Supply Input. Bypass V_{DD} with a 0.1µF capacitor from V_{DD} to GND.
2	SCLK	Serial-Interface Clock Input
3	DIN	Serial-Interface Data Input
4	$\overline{CS}$	Active-Low Digital-Input Chip Select
5	GND	Ground
6	L	Low Terminal. The voltage at L can be greater than or less than the voltage at H. Current can flow into or out of L.
7	W	Wiper Terminal
8	H	High Terminal. The voltage at H can be greater than or less than the voltage at L. Current can flow into or out of H.
—	EP	Exposed Pad. The exposed pad is not internally connected. Connect to GND or leave floating.

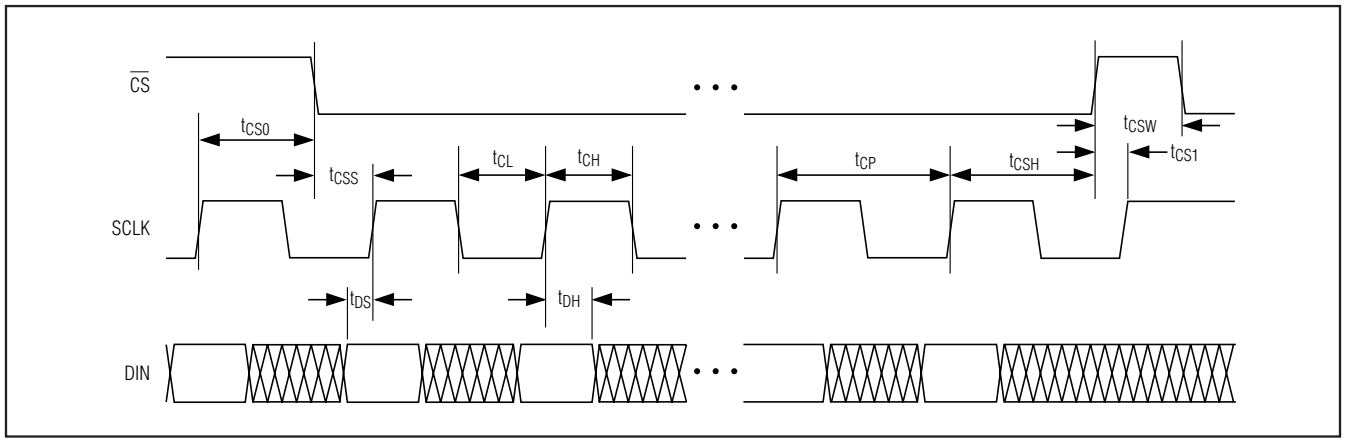


Figure 1. Digital Interface and Timing Diagram

Detailed Description

The MAX5422/MAX5423/MAX5424 contain a resistor array with 255 resistive elements. The MAX5422 has a total end-to-end resistance of 50kΩ; the MAX5423 has an end-to-end resistance of 100kΩ; and the MAX5424 has an end-to-end resistance of 200kΩ. The MAX5422/MAX5423/MAX5424 allow access to the high, low, and wiper terminals for a standard voltage-divider configuration. H, L, and W can be connected in any desired configuration as long as their voltages fall between GND and V_{DD}.

A simple, 3-wire, SPI serial interface moves the wiper among the 256 tap points. The nonvolatile memory stores the wiper position and recalls the stored wiper position upon power-up. The nonvolatile memory is guaranteed for 50 years for wiper data retention and up to 200,000 wiper store cycles.

Analog Circuitry

The MAX5422/MAX5423/MAX5424 consist of a resistor array with 255 resistive elements; 256 tap points are accessible to the wiper, W, along the resistor string between H and L. Select the wiper tap point by programming the potentiometer through the 3-wire (SPI) interface. Eight data bits, and a control byte program the wiper position. The H and L terminals of the MAX5422/MAX5423/MAX5424 are similar to the two end terminals of a mechanical potentiometer. The MAX5422/MAX5423/MAX5424 feature power-on reset circuitry that loads the wiper position from the nonvolatile memory at power-up.

Digital Interface

The MAX5422/MAX5423/MAX5424 use a 3-wire, SPI-compatible, serial data interface (Figure 1 and 2). This write-only interface contains three inputs: chip-select

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($\overline{CS}$), data clock (SCLK), and data in (DIN). Drive $\overline{CS}$ low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge.

The WRITE commands (C1, C0 = 00 or 01) require 16 clock cycles to clock in the command and data (Figure 2a). The COPY commands (C1, C0 = 10, 11) can use either eight clock cycles to transfer the command bits (Figure 2b) or 16 clock cycles with 8 data bits that are disregarded by the device (Figure 2a).

After loading data into the shift register, drive $\overline{CS}$ high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep $\overline{CS}$ low during the entire serial-data stream to avoid corruption of the data.

The serial-data timing for the potentiometer is shown in Figures 1 and 2.

Table 1. Register Map

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bit name	—	—	C1	C0	—	—	—	—	D7	D6	D5	D4	D3	D2	D1	D0
Write wiper register	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Write NV register	0	0	0	1	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Copy wiper register to NV register	0	0	1	0	0	0	0	0	—	—	—	—	—	—	—	—
Copy NV register to wiper register	0	0	1	1	0	0	0	0	—	—	—	—	—	—	—	—

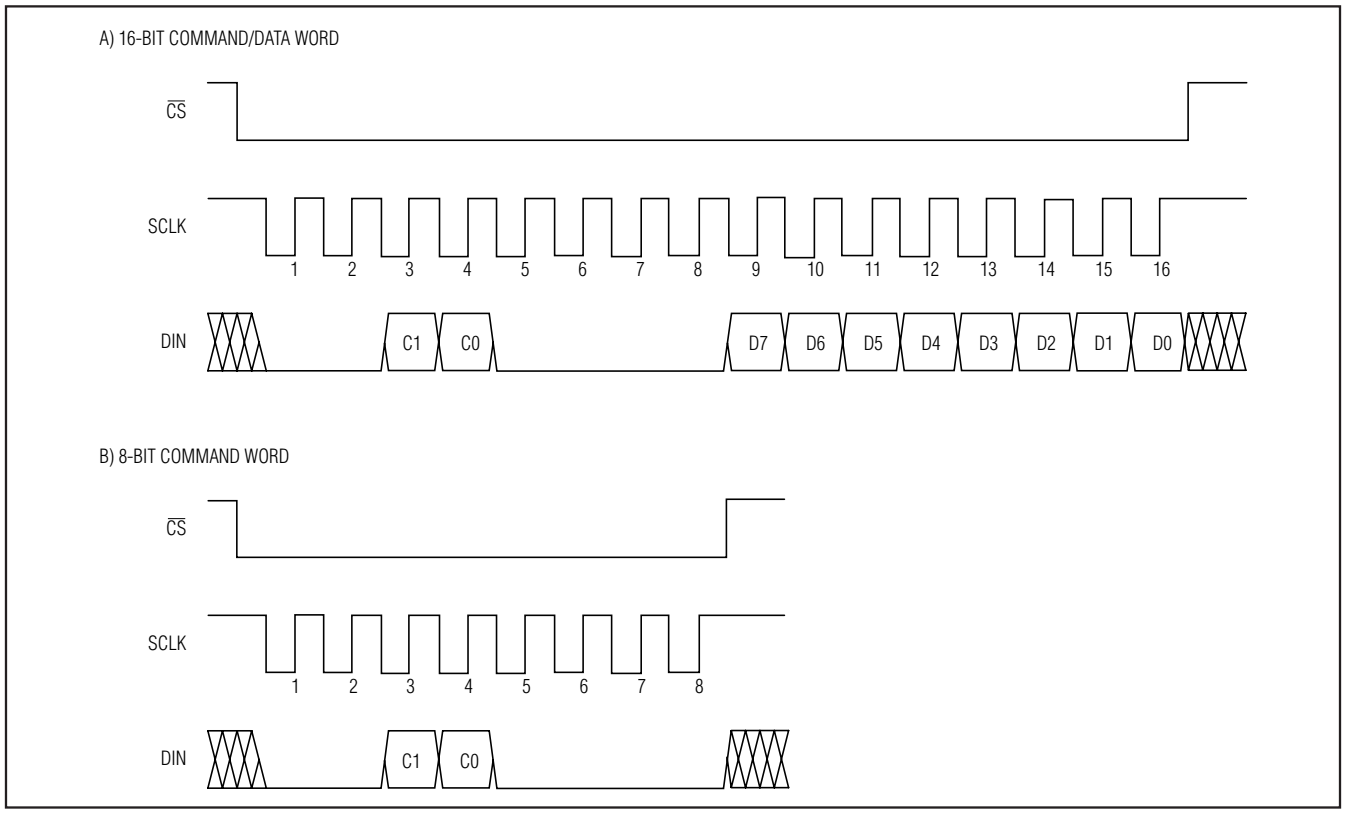


Figure 2. Digital-Interface Format

Write Wiper Register

Data written to this register (C1, C0 = 00) controls the wiper positions. The 8 data bits (D7 to D0) indicate the position of the wiper. For example, if DIN = 0000 0000, the wiper moves to the position closest to L. If DIN = 1111 1111, the wiper moves closest to H.

This command writes data to the volatile random access memory (RAM), leaving the NV registers unchanged. When the device powers up, the data stored in the NV registers transfers to the volatile wiper register, moving the wiper to the stored position.

Write NV Register

The "write NV register" command (C1, C0 = 01) stores the position of the wipers to the NV registers for use at power-up. Alternatively, the "copy wiper register to NV register" command writes to the NV register. Writing to the NV registers, does not affect the position of the wipers.

Copy Wiper Register to NV Register

The "copy wiper register to NV register" command (C1, C0 = 10) stores the current position of the wiper to the NV register for use at power-up.

Copy NV Register to Wiper Register

The "copy NV register to wiper register" (C1, C0 = 11) restores the wiper position to the current value stored in the NV register.

Standby Mode

The MAX5422/MAX5423/MAX5424 feature a low-power standby mode. When the device is not being programmed, it enters into standby mode and supply current drops to 0.5µA (typ).

Nonvolatile Memory

The internal EEPROM consists of a nonvolatile register that retains the last value stored prior to power-down. The nonvolatile register is programmed to midscale at the factory. The nonvolatile memory is guaranteed for 50 years for wiper data retention and up to 200,000 wiper write cycles.

Power-Up

Upon power-up, the MAX5422/MAX5423/MAX5424 load the data stored in the nonvolatile wiper register into the volatile wiper register, updating the wiper position with the data stored in the nonvolatile wiper register. This initialization period takes 10µs.

Applications Information

The MAX5422/MAX5423/MAX5424 are intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figures 3 and 4 show an application where a voltage-divider or variable resistor is used to make an adjustable, positive LCD-bias voltage. The op amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 3) or to a fixed resistor and a variable resistor (see Figure 4).

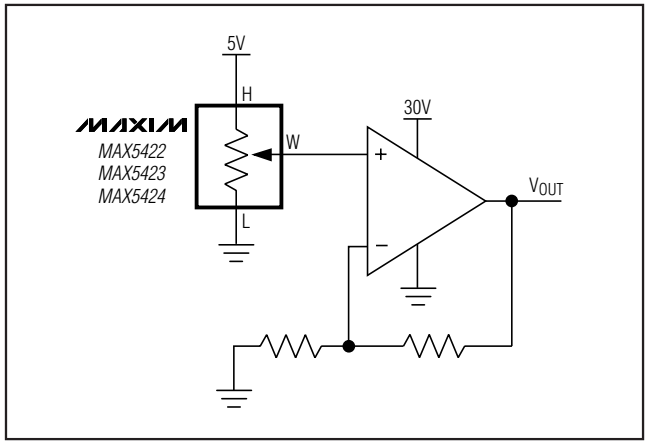


Figure 3. Positive LCD-Bias Control Using a Voltage-Divider

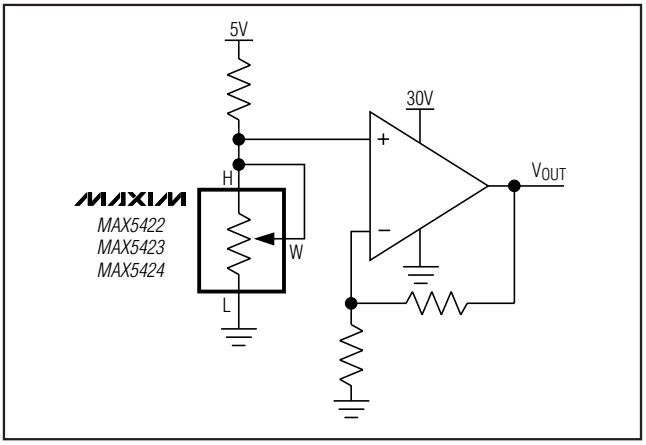


Figure 4. Positive LCD-Bias Control Using a Variable Resistor

256-Tap, Nonvolatile, SPI-Interface, Digital Potentiometers

Programmable Filter

Figure 5 shows the configuration for a 1st-order programmable filter. The gain of the filter is adjusted by R2, and the cutoff frequency is adjusted by R3. Use the following equations to calculate the DC gain (G) and the 3dB cutoff frequency (f_C):

$$G = 1 + \frac{R1}{R2}$$

$$f_C = \frac{1}{2\pi \times R3 \times C}$$

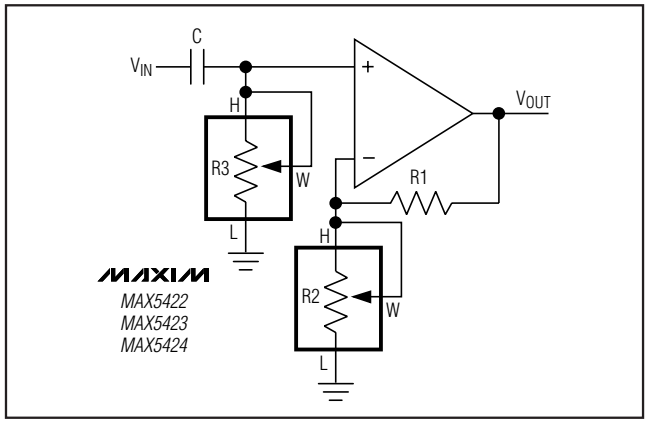


Figure 5. Programmable Filter

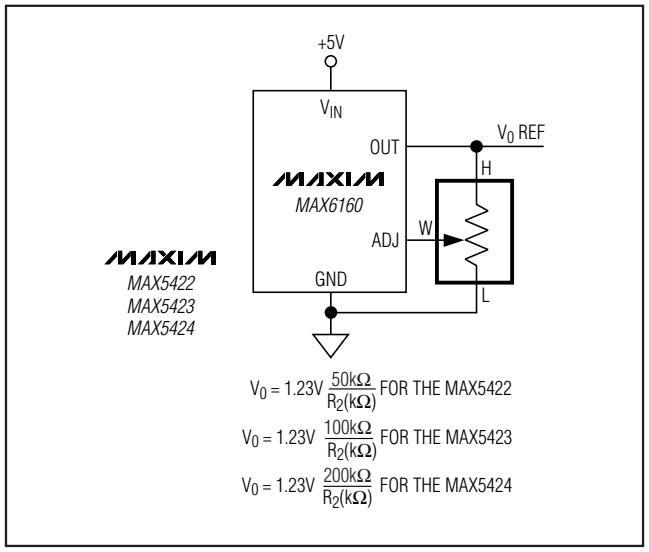


Figure 6. Adjustable Voltage Reference

Adjustable Voltage Reference

Figure 6 shows the MAX5422/MAX5423/MAX5424 used as the feedback resistors in an adjustable voltage-reference application. Independently adjust the output voltage of the MAX6160 from 1.23V to V_{IN} - 0.2V by changing the wiper position of the MAX5422/MAX5423/MAX5424.

Offset Voltage and Gain Adjustment

Connect the high and low terminals of one potentiometer of a MAX5422/MAX5423/MAX5424 between the NULL inputs of a MAX410 and the wiper to the op amp's positive supply to nullify the offset voltage over the operating temperature range. Install another MAX5422/MAX5423/MAX5424 potentiometer in the feedback path to adjust the gain of the MAX410 (see Figure 7).

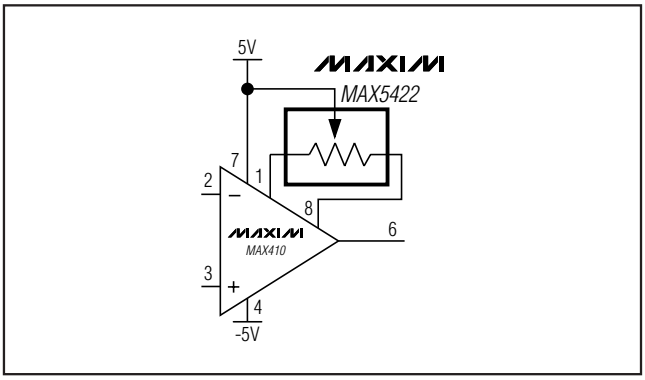


Figure 7. Offset Voltage Adjustment Circuit

Chip Information

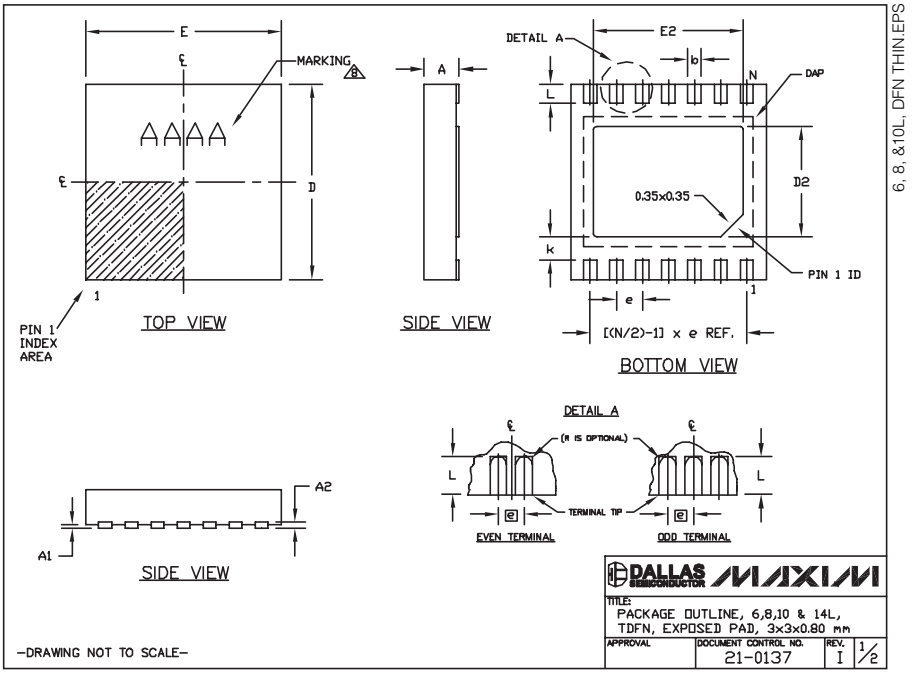
TRANSISTOR COUNT: 10,191

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L,
TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
I
2/2
-DRAWING NOT TO SCALE-

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX5422ETA+T MAX5423ETA+T MAX5424ETA+T