MAX5891

16-Bit, 600Msps, High-Dynamic-Performance DAC with LVDS Inputs

General Description

The MAX5891 advanced 16-bit, 600Msps, digital-to-analog converter (DAC) meets the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from 3.3V and 1.8V supplies, the MAX5891 DAC supports update rates of 600Msps using high-speed LVDS inputs while consuming only 298mW of power and offers exceptional dynamic performance such as 80dBc spurious-free dynamic range (SFDR) at f_{OUT} = 30MHz.

The MAX5891 utilizes a current-steering architecture that supports a 2mA to 20mA full-scale output current range, and produces -2dBm to -22dBm full-scale output signal levels with a double-terminated 50Ω load. The MAX5891 features an integrated 1.2V bandgap reference and control amplifier to ensure high-accuracy and low-noise performance. A separate reference input (REFIO) allows for the use of an external reference source for optimum flexibility and improved gain accuracy.

The MAX5891 digital inputs accept LVDS voltage levels, and the flexible clock input can be driven differentially or single-ended, AC- or DC-coupled. The MAX5891 is available in a 68-pin QFN package with an exposed paddle (EP) and is specified for the extended (-40°C to +85°C) temperature range.

Refer to the MAX5890 and MAX5889 data sheets for pin-compatible 14-bit and 12-bit versions of the MAX5891.

Applications

- Base Stations: Single/Multicarrier UMTS, CDMA, GSM
- Communications: Fixed Broadband Wireless Access, Point-to-Point Microwave
- Direct Digital Synthesis (DDS)
- Cable Modem Termination Systems (CMTS)
- Automated Test Equipment (ATE)
- Instrumentation

Selector Guide

PART	RESOLUTION (BITS)	UPDATE RATE (Msps)	LOGIC INPUT
MAX5889	12	600	LVDS
MAX5890	14	600	LVDS
MAX5891	16	600	LVDS

***Pin Configuration** appears at end of data sheet.*

Features

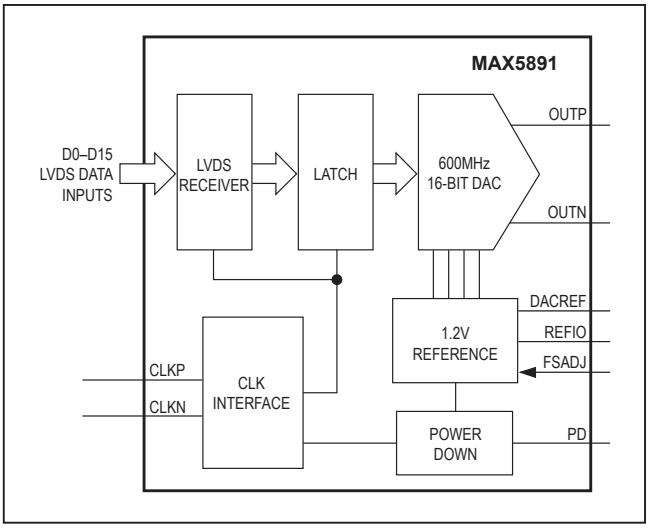
- 600Msps Output Update Rate
- Low Noise Spectral Density: -163dBFS/Hz at f_{OUT} = 36MHz
- Excellent SFDR and IMD Performance
  - SFDR = 80dBc at f_{OUT} = 30MHz (to Nyquist)
  - SFDR = 71dBc at f_{OUT} = 130MHz (to Nyquist)
  - IMD = -95dBc at f_{OUT} = 30MHz
  - IMD = -70dBc at f_{OUT} = 130MHz
- ACLR = 73dB at f_{OUT} = 122.88MHz
- 2mA to 20mA Full-Scale Output Current
- LVDS-Compatible Digital Inputs
- On-Chip 1.2V Bandgap Reference
- Low 298mW Power Dissipation at 600Msps
- Compact (10mm x 10mm) QFN-EP Package
- Evaluation Kit Available (MAX5891EVKIT)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5891EGK-D	-40°C to +85°C	68 QFN-EP*	G6800-4
MAX5891EGK+D	-40°C to +85°C	68 QFN-EP*	G6800-4

**EP = Exposed paddle.*
+ = Lead-free package.
D = Dry pack.

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

$AV_{DD1.8}$, $DV_{DD1.8}$ to AGND, DGND, DACREF, and CGND .....-0.3V to +2.16V
$AV_{DD3.3}$, $DV_{DD3.3}$, AV_{CLK} to AGND, DGND, DACREF, and CGND.....-0.3V to +3.9V
REFIO, FSADJ to AGND, DACREF, DGND, and CGND .....-0.3V to ($AV_{DD3.3}$ + 0.3V)
OUTP, OUTN to AGND, DGND, DACREF, and CGND .....-1.2V to ($AV_{DD3.3}$ + 0.3V)
CLKP, CLKN to AGND, DGND, DACREF, and CGND ..... -0.3V to (AV_{CLK} + 0.3V)
PD to AGND, DGND, DACREF, and CGND ..... -0.3V to ($DV_{DD3.3}$ + 0.3V)
Digital Data Inputs (D0N–D15N, D0P–D15P) to AGND, DGND, DACREF, and CGND..... -0.3V to ($DV_{DD1.8}$ + 0.3V)
Continuous Power Dissipation (T_A = +70°C) (Note 1)
68-Pin QFN-EP (derate 28.6mW/°C above +70°C) ..3333mW
Thermal Resistance θ_{JA} (Note 1) .....24°C/W
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Thermal resistance based on a multilayer board with 4x4 via array in exposed paddle area.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference V_{REFIO} = 1.2V, output load 50Ω double-terminated, transformer-coupled output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution					16		Bits
Integral Nonlinearity	INL	Measured differentially			±3.8		LSB
Differential Nonlinearity	DNL	Measured differentially			±2.8		LSB
Offset Error	OS			-0.02	±0.001	+0.02	%FS
Full-Scale Gain Error	GE_{FS}	External reference		-4	±1	+4	%FS
Gain-Drift Tempco		Internal reference			±130		ppm/°C
		External reference			±100		
Full-Scale Output Current	I_{OUT}			2		20	mA
Output Compliance		Single-ended		-1.0		+1.1	V
Output Resistance	R_{OUT}				1		MΩ
Output Capacitance	C_{OUT}				5		pF
Output Leakage Current		PD = high, power-down mode			±1		µA
DYNAMIC PERFORMANCE							
Maximum DAC Update Rate				600			Msps
Minimum DAC Update Rate					1		Msps
Noise Spectral Density	N	f_{CLK} = 500MHz, -12dBFS, 20MHz offset from the carrier	f_{OUT} = 36MHz $A_{FULL-SCALE}$ = -3.5dBm		-163		dBFS/Hz
			f_{OUT} = 151MHz $A_{FULL-SCALE}$ = -6.4dBm		-155		

Electrical Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference V_{REFIO} = 1.2V, output load 50Ω double-terminated, transformer-coupled output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{CLK} = 200MHz, 0dBFS (Note 2)	f_{OUT} = 16MHz		89		dBc
			f_{OUT} = 30MHz		85		
		f_{CLK} = 200MHz, -12dBFS (Note 2)	f_{OUT} = 16MHz		79		
			f_{OUT} = 30MHz		81		
		f_{CLK} = 500MHz, 0dBFS	f_{OUT} = 16MHz (Note 3)	76	81		
			f_{OUT} = 30MHz (Note 2)		80		
			f_{OUT} = 130MHz (Note 2)		71		
			f_{OUT} = 200MHz (Note 2)		56		
Two-Tone IMD	TTIMD	f_{CLK} = 500MHz	f_{OUT1} = 29MHz, f_{OUT2} = 30MHz, -6.5dBFS per tone		-95		dBc
		f_{CLK} = 500MHz	f_{OUT1} = 129MHz, f_{OUT2} = 130MHz, -6.5dBFS per tone		-70		
Adjacent Channel Leakage Power Ratio	ACLR	WCDMA single carrier	f_{CLK} = 491.52MHz, f_{OUT} = 30.72MHz		82		dB
			f_{CLK} = 491.52MHz, f_{OUT} = 122.88MHz		73		
		WCDMA four carriers	f_{CLK} = 491.52MHz, f_{OUT} = 30.72MHz		74		
			f_{CLK} = 491.52MHz, f_{OUT} = 122.88MHz		67		
Output Bandwidth	BW_{-1dB}	(Note 4)			1000		MHz
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.14	1.2	1.26	V
Reference Input Voltage Range	$V_{REFIOCR}$	Using external reference		0.10	1.2	1.32	V
Reference Input Resistance	R_{REFIO}				10		kΩ
Reference Voltage Temperature Drift	TCO_{REF}				±30		ppm/°C
ANALOG OUTPUT TIMING (Figure 3)							
Output Fall Time	t_{FALL}	90% to 10% (Note 5)			0.4		ns
Output Rise Time	t_{RISE}	10% to 90% (Note 5)			0.4		ns
Output Propagation Delay	t_{PD}	Reference to data latency (Note 5)			2.5		ns
Output Settling Time		To 0.025% of the final value (Note 5)			11		ns
Glitch Impulse		Measured differentially			1		pV•s
Output Noise	N_{OUT}	I_{OUT} = 2mA			30		pA/√Hz
		I_{OUT} = 20mA			30		

Electrical Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference V_{REFIO} = 1.2V, output load 50Ω double-terminated, transformer-coupled output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Input Data Rate					600	Mwps
Data Latency				5.5		Clock cycles
Data to Clock Setup Time	t_{SETUP}	Referenced to rising edge of clock (Note 6)	-1.5			ns
Data to Clock Hold Time	t_{HOLD}	Referenced to rising edge of clock (Note 6)	2.6			ns
Clock Frequency	f_{CLK}	CLKP, CLKN			600	MHz
Minimum Clock Pulse-Width High	t_{CH}	CLKP, CLKN		0.6		ns
Minimum Clock Pulse-Width Low	t_{CL}	CLKP, CLKN		0.6		ns
Turn-On Time	t_{SHDN}	External reference, PD falling edge to output settle within 1%		350		µs
CMOS LOGIC INPUT (PD)						
Input Logic High	V_{IH}		0.7 x $DV_{DD3.3}$			V
Input Logic Low	V_{IL}				0.3 x $DV_{DD3.3}$	V
Input Current	I_{IN}		-10	±1.8	+10	µA
Input Capacitance	C_{IN}			3		pF
LVDS INPUTS						
Differential Input High	V_{IHLVDS}	(Notes 6, 7, 8)	+100		+1000	mV
Differential Input Low	V_{ILLVDS}	(Notes 6, 7, 8)	-1000		-100	mV
Internal Common-Mode Bias	$V_{ICMLVDS}$		1.125		1.375	V
External Common-Mode Tolerance	$V_{ECMLVDS}$	(Notes 6, 8)	0.8		$V_{DD1.8}$ - 0.15	V
Differential Input Resistance	R_{IDLVDS}			110		Ω
Common-Mode Input Resistance	$R_{ICMLVDS}$			3.2		kΩ
Input Capacitance	C_{INLVDS}			3		pF
DIFFERENTIAL CLOCK INPUTS (CLKP, CLKN)						
Clock Common-Mode Voltage		CLKP and CLKN are internally biased		AV_{CLK}/2		V
Minimum Differential Input Voltage Swing				0.5		V_{P-P}
Minimum Common-Mode Voltage				1		V
Maximum Common-Mode Voltage				1.9		V
Input Resistance	R_{CLK}	Single-ended		5		kΩ
Input Capacitance	C_{CLK}			3		pF
POWER SUPPLIES						
Analog Supply Voltage Range	$AV_{DD3.3}$		3.135	3.3	3.465	V
	$AV_{DD1.8}$		1.710	1.8	1.890	
Clock Supply Voltage Range	AV_{CLK}		3.135	3.3	3.465	V

Electrical Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference V_{REFIO} = 1.2V, output load 50Ω double-terminated, transformer-coupled output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage Range	$DV_{DD3.3}$		3.135	3.3	3.465	V
	$DV_{DD1.8}$		1.710	1.8	1.890	
Analog Supply Current	$I_{AVDD3.3}$	f_{CLK} = 100MHz, f_{OUT} = 16MHz		26.5		mA
		f_{CLK} = 500MHz, f_{OUT} = 16MHz		26.5	28.5	
		f_{CLK} = 600MHz, f_{OUT} = 16MHz		26.5		
	$I_{AVDD1.8}$	f_{CLK} = 100MHz, f_{OUT} = 16MHz		11.3		
		f_{CLK} = 500MHz, f_{OUT} = 16MHz		50	58	
		f_{CLK} = 600MHz, f_{OUT} = 16MHz		61		
Clock Supply Current	I_{AVCLK}	f_{CLK} = 100MHz, f_{OUT} = 16MHz		2.8		mA
		f_{CLK} = 500MHz, f_{OUT} = 16MHz		2.8	3.6	
		f_{CLK} = 600MHz, f_{OUT} = 16MHz		2.8		
Digital Supply Current	$I_{DVDD3.3}$	f_{CLK} = 100MHz, f_{OUT} = 16MHz		0.2		mA
		f_{CLK} = 500MHz, f_{OUT} = 16MHz		0.2	0.5	
		f_{CLK} = 600MHz, f_{OUT} = 16MHz		0.2		
	$I_{DVDD1.8}$	f_{CLK} = 100MHz, f_{OUT} = 16MHz		10.6		
		f_{CLK} = 500MHz, f_{OUT} = 16MHz		44	50	
		f_{CLK} = 600MHz, f_{OUT} = 16MHz		50.5		
Total Power Dissipation	P_{DISS}	f_{CLK} = 100MHz, f_{OUT} = 16MHz		137		mW
		f_{CLK} = 500MHz, f_{OUT} = 16MHz		267	301	
		f_{CLK} = 600MHz, f_{OUT} = 16MHz		298		
		Power-down, clock static low, data input static		13		µW
Power-Supply Rejection Ratio	PSRR	(Note 9)		±0.025		%FS

Note 2: Parameter tested with input data pattern based on 16,384 data points. f_{OUT} has been chosen so the corresponding input pattern contains prime number of f_{OUT} cycles and is a nonrepetitive sequence. f_{OUT} has been rounded to the nearest MHz number in both the *Electrical Characteristics* table and *Typical Operating Characteristics*.

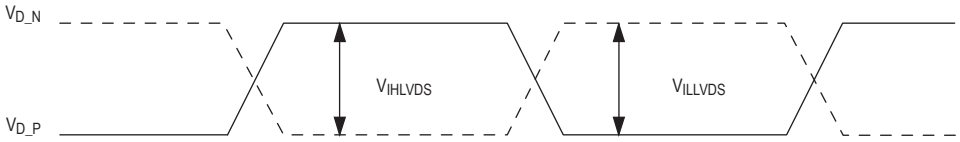
Note 3: Parameter tested exactly at f_{OUT} = 16.204833984375MHz and with a clock frequency of 500MHz at an output amplitude of 0dBFS.

Note 4: This parameter does not include update-rate-dependent effects of sin(x)/x filtering inherent in the MAX5891.

Note 5: Parameter measured single-ended with 50Ω double-terminated outputs.

Note 6: Not production tested. Guaranteed by design.

Note 7: Differential input voltage defined as V_{D_P} - V_{D_N}.



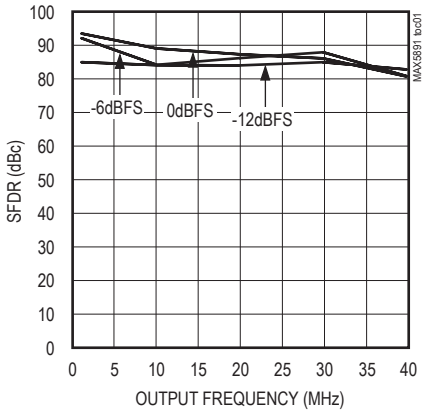
Note 8: Combination of logic-high/-low and common-mode voltages must not exceed absolute maximum rating for D_P/D_N inputs.

Note 9: Parameter defined as the change in midscale output caused by a ±5% variation in the nominal supply voltages.

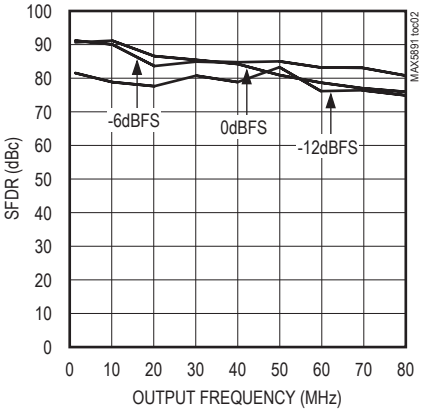
Typical Operating Characteristics

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference V_{REFIO} = 1.2V, output load 50Ω double-terminated, transformer-coupled output, I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

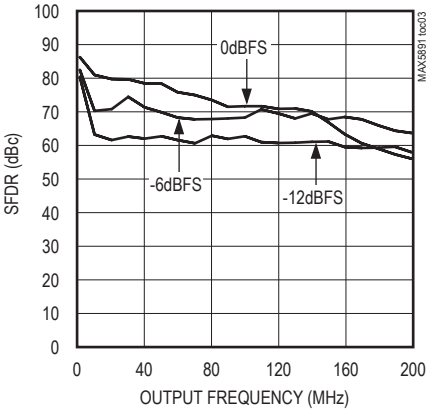
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 100MHz)



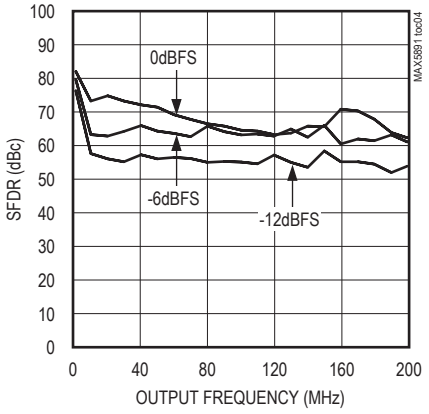
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 200MHz)



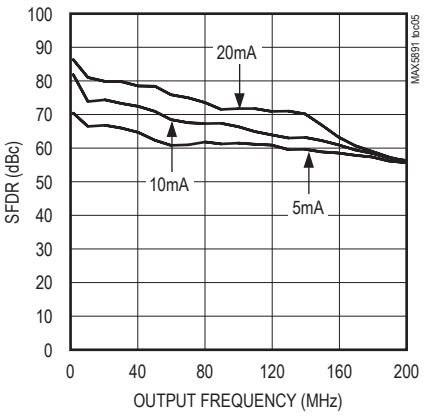
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 500MHz)



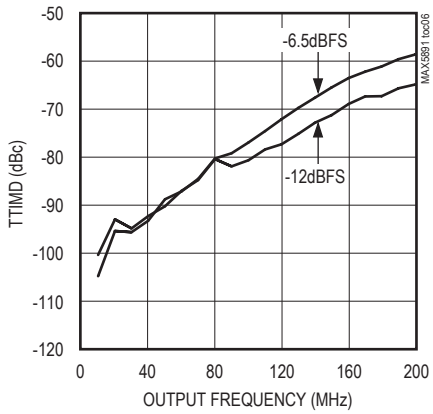
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 600MHz)



SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 500MHz, I_{OUT} = 20mA, 10mA, 5mA)



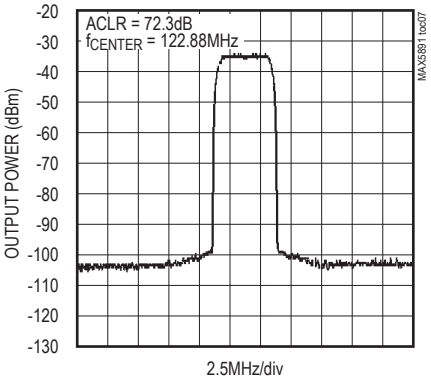
TWO-TONE INTERMODULATION DISTORTION vs. OUTPUT FREQUENCY (f_{CLK} = 500MHz, 1MHz CARRIER SPACING)



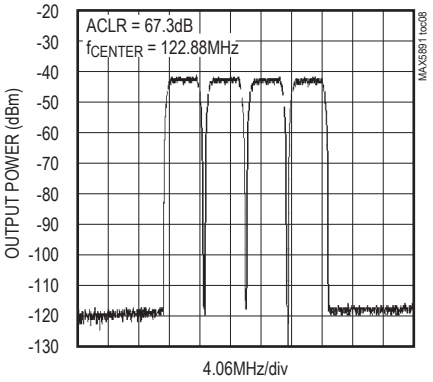
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference V_{REFIO} = 1.2V, output load 50Ω double-terminated, transformer-coupled output, I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

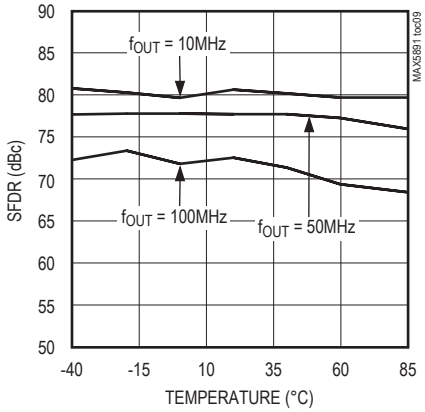
SINGLE-CARRIER WCDMA ACLR (f_{CLK} = 491.52MHz)



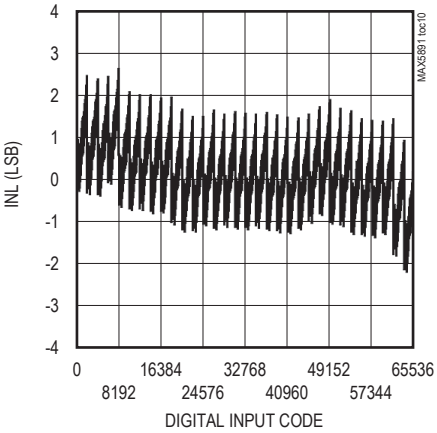
FOUR-CARRIER WCDMA ACLR (f_{CLK} = 491.52MHz)



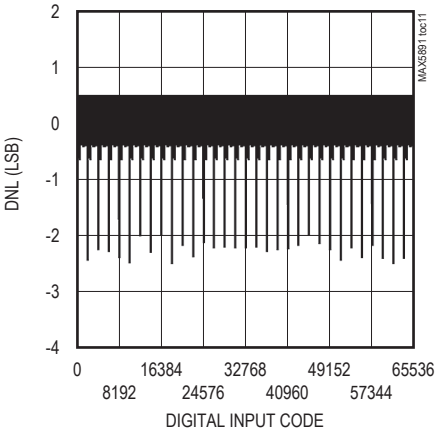
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE (f_{CLK} = 500MHz)



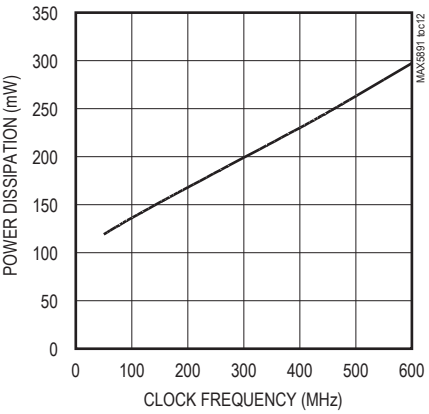
INTEGRAL NONLINEARITY



DIFFERENTIAL NONLINEARITY



TOTAL POWER DISSIPATION vs. CLOCK FREQUENCY (f_{OUT} = 16MHz, A_{OUT} = 0dBFS)



Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 9, 46, 48, 50, 52, 54, 56, 58, 60, 63, 65, 67	D4N, D3N, D2N, D1N, D0N, D15N, D14N, D13N, D12N, D11N, D10N, D9N, D8N, D7N, D6N, D5N	Differential Negative LVDS Inputs. Data bits D0–D15 (offset binary format).
2, 4, 6, 8, 45, 47, 49, 51, 53, 55, 57, 59, 62, 64, 66, 68	D3P, D2P, D1P, D0P, D15P, D14P, D13P, D12P, D11P, D10P, D9P, D8P, D7P, D6P, D5P, D4P	Differential Positive LVDS Inputs. Data bits D0–D15 (offset binary format).
10	DGND	Digital Ground. Ground return for $DV_{DD3.3}$ and $DV_{DD1.8}$.
15, 20, 23, 24, 27, 30, 33	AGND	Analog Ground. Ground return for $AV_{DD3.3}$ and $AV_{DD1.8}$.
11	$DV_{DD3.3}$	Digital Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to DGND.
12	PD	Power-Down Input. Set PD high to force the DAC into power-down mode. Set PD low for normal operation. PD has an internal 2µA pulldown.
13, 42, 43, 44	N.C.	No Connection. Leave floating or connect to AGND.
14, 21, 22, 25, 26, 31, 32	$AV_{DD3.3}$	Analog Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to AGND.
16	REFIO	Reference I/O. Output of the internal 1.2V precision bandgap reference. Bypass with a 0.1µF capacitor to AGND. REFIO can be driven with an external reference source.
17	FSADJ	Full-Scale Current Adjustment. Connect an external resistor R_{SET} between FSADJ and DACREF to set the output full-scale current. The output full-scale current is equal to 32 x V_{REF}/R_{SET}.
18	DACREF	Current-Set Resistor Return Path. Internally connected to ground, but do not use as ground connection.
19, 34, 35	$AV_{DD1.8}$	Analog Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass with a 0.1µF capacitor to AGND.
28	OUTN	Complementary DAC Output. Negative terminal for current output.
29	OUTP	DAC Output. Positive terminal for current output.
36, 41	AV_{CLK}	Clock Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to CGND.
37, 40	CGND	Clock Supply Ground
38	CLKN	Complementary Converter Clock Input. Negative input terminal for differential converter clock.
39	CLKP	Converter Clock Input. Positive input terminal for differential converter clock.
61	$DV_{DD1.8}$	Digital Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass with a 0.1µF capacitor to DGND.
—	EP	Exposed Pad. Must be connected to common point for AGND, DGND, and CGND through a low-impedance path. EP is internally connected to AGND, DGND, and CGND.

Detailed Description

Architecture

The MAX5891 high-performance, 16-bit, current-steering DAC (see the *Functional Diagram*) operates with DAC update rates up to 600Msps. The current-steering array generates differential full-scale currents in the 2mA to 20mA range. An internal current-switching network, in combination with external 50Ω termination resistors, converts the differential output currents into a differential output voltage with a 0.1V to 1V peak-to-peak output voltage range. The analog outputs have a -1.0V to +1.1V voltage compliance. For applications requiring high dynamic performance, use the differential output configuration and limit the output voltage swing to ±0.5V at each output. An integrated 1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale output range.

Reference Architecture and Operation

The MAX5891 operates with the internal 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source or as a reference output when the DAC operates in internal reference mode. For stable operation with the internal reference, bypass REFIO to AGND with a 0.1µF capacitor. The REFIO output resistance is 10kΩ. Buffer REFIO with a high-input-impedance amplifier when using it as a reference source for external circuitry.

The MAX5891's reference circuit (Figure 1) employs a control amplifier to regulate the full-scale current, I_{OUTFS}, for the differential current outputs of the DAC. Calculate the output current as follows:

$$I_{OUTFS} = 32 \times \frac{V_{REFIO}}{R_{SET}} \times \left(1 - \frac{1}{2^{16}}\right)$$

where I_{OUTFS} is the full-scale output current of the DAC. R_{SET} (located between FSADJ and DACREF) determines the amplifier's full-scale output current for the DAC. See Table 1 for a matrix of different I_{OUTFS} and R_{SET} selections.

Table 1. I_{OUTFS} and RSET Selection Matrix Based on a Typical 1.200V Reference Voltage

FULL-SCALE CURRENT I_{OUTFS} (mA)	R_{SET} (Ω)	
	CALCULATED	1% EIA STD
2	19.2k	19.1k
5	7.68k	7.5k
10	3.84k	3.83k
15	2.56k	2.55k
20	1.92k	1.91k

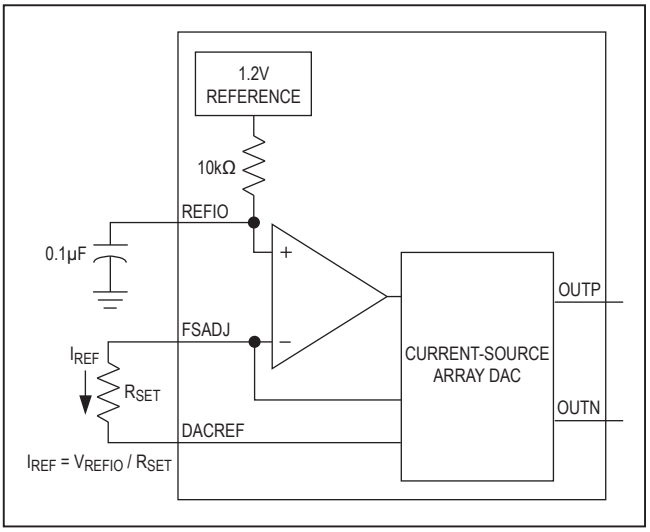


Figure 1. Reference Architecture, Internal Reference Configuration

Analog Outputs (OUTP, OUTN)

The complementary current outputs (OUTP, OUTN) can be connected in a single-ended or differential configuration. A load resistor converts these two output currents into complementary single-ended output voltages. A transformer or a differential amplifier converts the differential voltage existing between OUTP and OUTN to a single-ended voltage. When not using a transformer, terminate each output with a 25Ω resistor to ground and a 50Ω resistor between the outputs.

To generate a single-ended output, select OUTP as the output and connect OUTN to AGND. Figure 2 shows a simplified diagram of the internal output structure of the MAX5891.

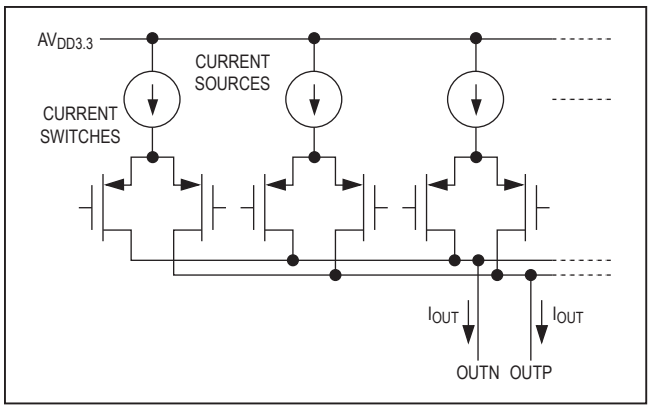


Figure 2. Simplified Analog Output Structure

Clock Inputs (CLKP, CLKN)

To achieve the best possible jitter performance, the MAX5891 features flexible differential clock inputs (CLKP, CLKN) that operate from a separate clock power supply (AV_{CLK}). Drive the differential clock inputs from a single-ended or a differential clock source. For highest dynamic performance, differential clock source is required. For single-ended operation, drive CLKP and bypass CLKN to CGND.

CLKP and CLKN are internally biased at $AV_{CLK}/2$, allowing the AC-coupling of clock sources directly to the device without external resistors to define the DC level. The input resistance from CLKP and CLKN to ground is approximately 5kΩ.

Data-Timing Relationship

Figure 3 shows the timing relationship between digital LVDS data, clock, and output signals. The MAX5891 features a 2.6ns hold, a -1.5ns setup, and a 2.5ns propagation delay time. There is a 5.5 clock-cycle latency between data write operation and the corresponding analog output transition.

LVDS Data Inputs

The MAX5891 has 16 pairs of LVDS data inputs (offset binary format) and can accept data rates up to 600Mwps. Each differential input pair is terminated with an internal 110Ω resistor. The common-mode input resistance is 3.2kΩ.

Power-Down Operation (PD)

The MAX5891 features a power-down mode that reduces the DAC's power consumption. Set PD high to power down the MAX5891. Set PD low or leave unconnected for normal operation.

When powered down, the MAX5891 overall power consumption is reduced to less than 13µW. The MAX5891 requires 350µs to wake up from power-down and enter a fully operational state if the external reference is used. If the internal reference is used, the power-down recovery time is 10ms. The PD internal pulldown circuit sets the MAX5891 in normal mode when PD is left unconnected.

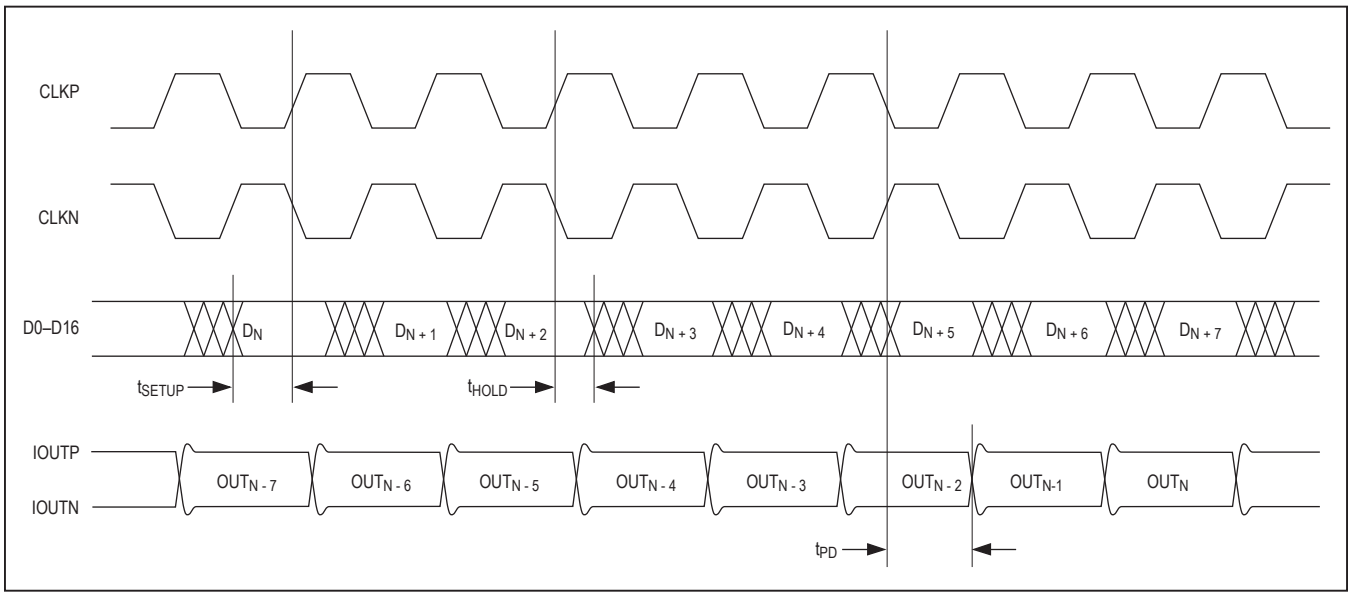


Figure 3. Timing Relationship Between Clock, Input Data, and Analog Output

Applications Information

Clock Interface

To achieve the best possible jitter performance, the MAX5891 features flexible differential clock inputs (CLKP, CLKN) that operate from a separate clock power supply (AV_{CLK}). Use a low-jitter clock to reduce the DAC's phase noise and wideband noise. To achieve the best DAC dynamic performance, the CLKP/CLKN input source must be designed carefully. The differential clock (CLKN and CLKP) input can be driven from a single-ended or a differential clock source. Use differential clock drive to achieve the best dynamic performance from the DAC. For single-ended operation, drive CLKP with a low noise source and bypass CLKN to CGND with a 0.1µF capacitor.

Figure 4 shows a convenient and quick way of applying a differential signal created from a single-ended source using a wideband transformer. Alternatively, drive CLKP/CLKN from a CMOS-compatible clock source. Use sinewave or AC-coupled differential ECL/PECL drive for best dynamic performance.

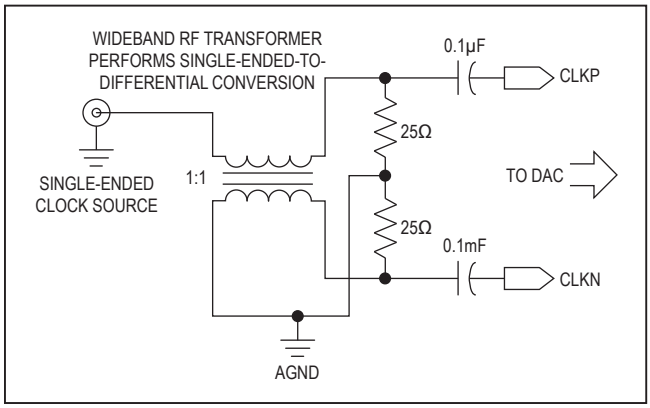


Figure 4. Differential Clock-Signal GenerationAnalog Output

Differential Output Coupling Using a Wideband RF Transformer

Use a pair of transformers (Figure 5) or a differential amplifier configuration to convert the differential voltage existing between OUTP and OUTN to a single-ended voltage. Optimize the dynamic performance by using a differential transformer-coupled output and limit the output power to < 0dBm full scale. To achieve the best dynamic performance, use the differential transformer configuration. Terminate the DAC as shown in Figure 5, and use 50Ω termination at the transformer single-ended output. This will provide double 50Ω termination for the DAC output network. With the double-terminated output and 20mA full-scale current, the DAC will produce a full-scale signal level of approximately -2dBm. Pay close attention to the transformer core saturation characteristics when selecting a transformer for the MAX5891. Transformer core saturation can introduce strong 2nd-order harmonic distortion especially at low output frequencies and high signal amplitudes. For best results, connect the center tap of the transformer to ground. When not using a transformer, terminate each DAC output to ground with a 25Ω resistor. Additionally, place a 50Ω resistor between the outputs (Figure 6).

For a single-ended unipolar output, select OUTP as the output and connect OUTN to AGND. Operating the MAX5891 single-ended is not recommended because it degrades the dynamic performance.

The distortion performance of the DAC depends on the load impedance. The MAX5891 is optimized for 50Ω differential double termination. Using higher termination impedance degrades distortion performance and increases output noise voltage.

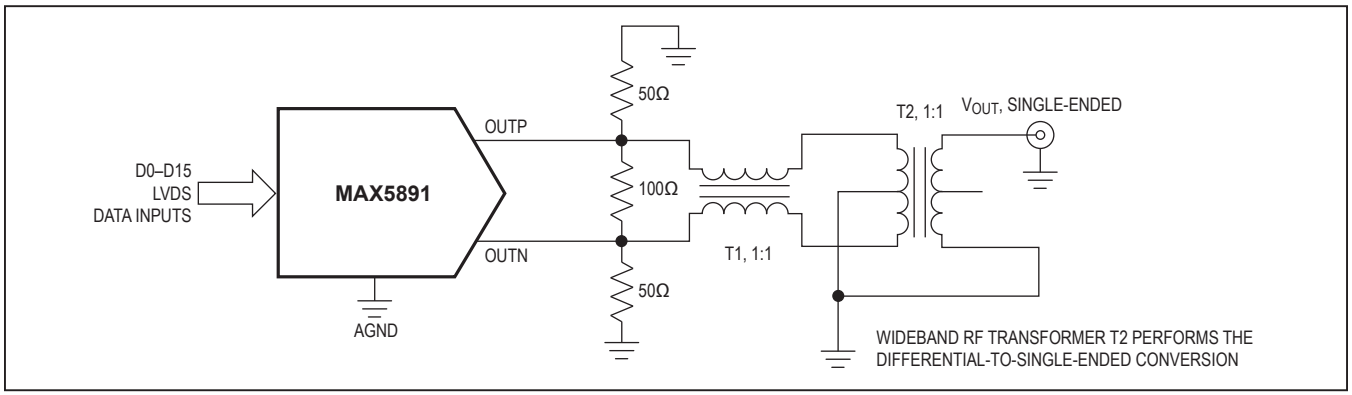


Figure 5. Differential-to-Single-Ended Conversion Using a Wideband RF Transformer

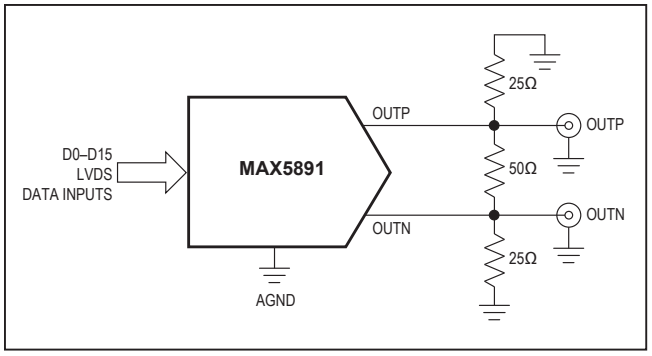


Figure 6. Differential Output Configuration

Grounding, Bypassing, and Power-Supply Considerations

Grounding and power-supply decoupling strongly influence the MAX5891 performance. Unwanted digital crosstalk coupling through the input, reference, power supply, and ground connections affects dynamic performance. High-speed, high-frequency applications require closely followed proper grounding and power-supply decoupling. These techniques reduce EMI and internal crosstalk that can significantly affect the MAX5891 dynamic performance.

Use a multilayer printed circuit board (PCB) with separate ground and power-supply planes. Run high-speed signals on lines directly above the ground plane. Keep digital signals as far away from sensitive analog inputs and outputs, reference input sense lines, common-mode inputs, and clock inputs as practical. Use a symmetric design of clock input and the analog output lines to minimize 2nd-order harmonic distortion components, thus optimizing the DAC's dynamic performance. Keep digital signal paths short and run lengths matched to avoid propagation delay and data skew mismatches.

The MAX5891 requires five separate power-supply inputs for analog ($AV_{DD1.8}$ and $AV_{DD3.3}$), digital ($DV_{DD1.8}$ and $DV_{DD3.3}$), and clock (AV_{CLK}) circuitry. Decouple each $AV_{DD3.3}$, $AV_{DD1.8}$, AV_{CLK}, $DV_{DD3.3}$, and $DV_{DD1.8}$ input with a separate 0.1µF capacitor as close to the device as possible with the shortest possible connection to the respective ground plane (Figure 7). Connect all of the 3.3V supplies together at one point with ferrite beads to minimize supply noise coupling. Decouple all five power-supply voltages at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi network can also improve performance. Similarly, connect all 1.8V supplies together at one point with ferrite beads.

The analog and digital power-supply inputs $AV_{DD3.3}$, AV_{CLK}, and $DV_{DD3.3}$ allow a 3.135V to 3.465V supply voltage range. The analog and digital power-supply inputs $AV_{DD1.8}$ and $DV_{DD1.8}$ allow a 1.71V to 1.89V supply voltage range.

The MAX5891 is packaged in a 68-pin QFN-EP package with exposed paddle, providing optimized DAC AC performance. The exposed pad must be soldered to the ground plane of the PCB. Thermal efficiency is not the key factor, since the MAX5891 features low- power operation. The exposed pad ensures a solid ground connection between the DAC and the PCB's ground layer.

The data converter die attaches to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PCB side of the package. This allows for a solid attachment of the package to the PCB with standard infrared (IR) reflow soldering techniques. A specially created land pattern on the PCB, matching the size of the EP (6mm x 6mm), ensures the proper attachment and grounding of the DAC. Place vias into the land area and implement large ground planes in the PCB design

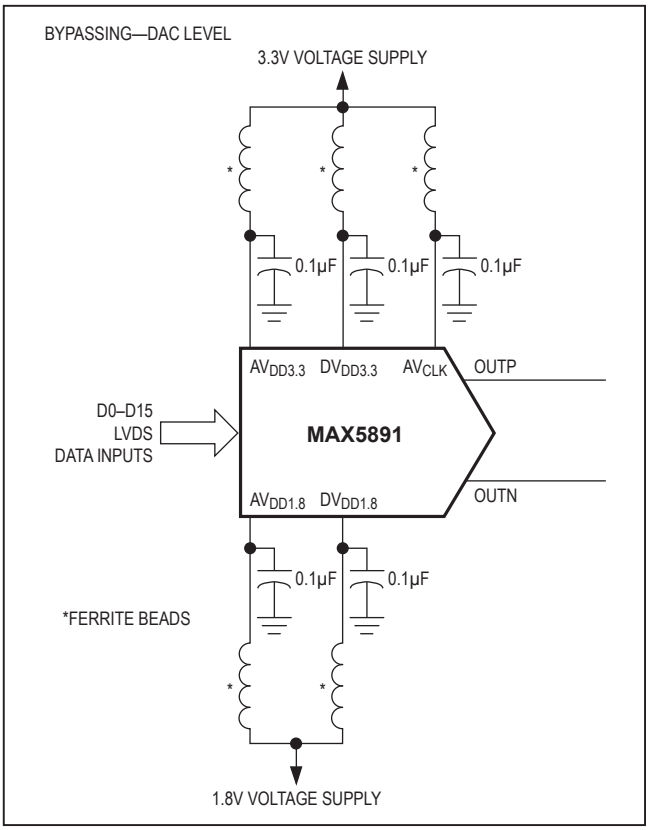


Figure 7. Recommended Power-Supply Decoupling and Bypassing Circuitry

to ensure the highest dynamic performance of the DAC. Connect the MAX5891 exposed paddle to the common connection point of DGND, AGND, and CGND. Vias connect the top land pattern to internal or external copper planes. Use as many vias as possible to the ground plane to minimize inductance. The vias should have a diameter greater than 0.3mm.

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB.

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011...111 to 100...000. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impluse is usually specified in pV•s.

Dynamic Performance Parameter Definitions

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog output (RMS value) to the RMS quantization error (residual error). The ideal, theoretical maximum can be derived from the DAC's resolution (N bits):

$$SNRdB = 6.02dB \times N + 1.76dB$$

However, noise sources such as thermal noise, reference noise, clock jitter, etc., affect the ideal reading; therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

Noise Spectral Density

The DAC output noise floor is the sum of the quantization noise and the output amplifier noise (thermal and shot noise). Noise spectral density is the noise power in 1Hz bandwidth, specified in dBFS/Hz.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of their next-largest distortion component. SFDR is usually measured in dBc and with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

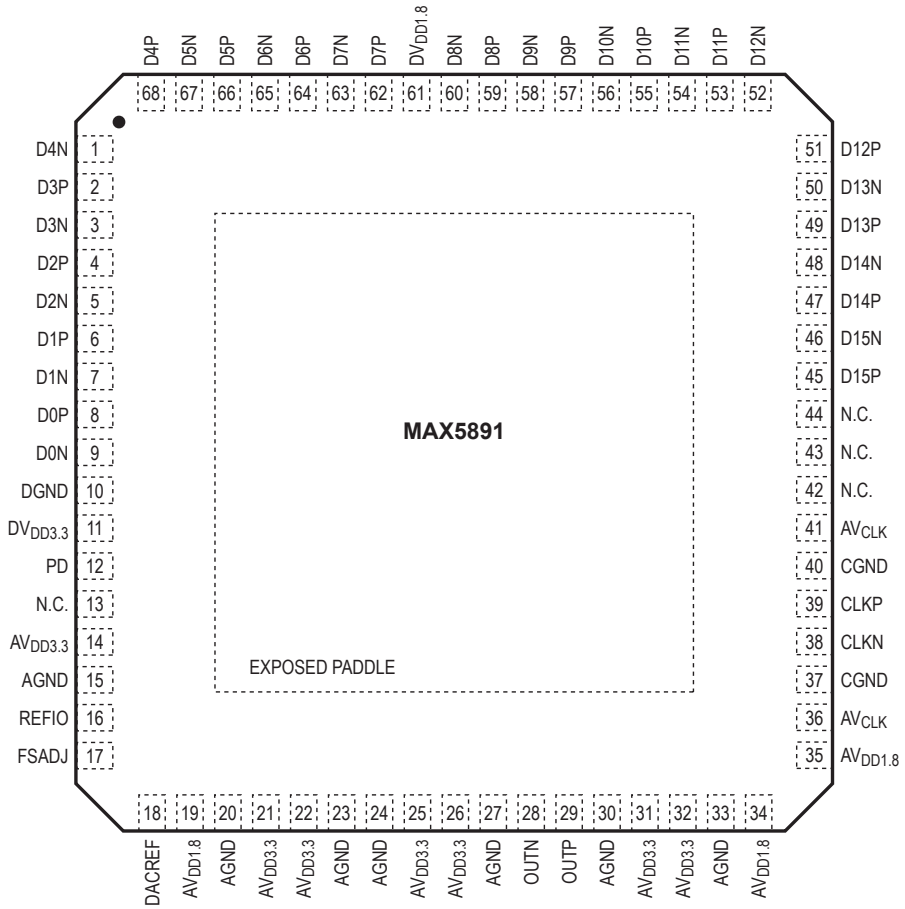
Two-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order IMD differential product to either output tone. The two-tone IMD performance of the MAX5891 is tested with the two individual output tone levels set to at least -6.5dBFS.

Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with wideband code-division multiple-access (WCDMA), ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

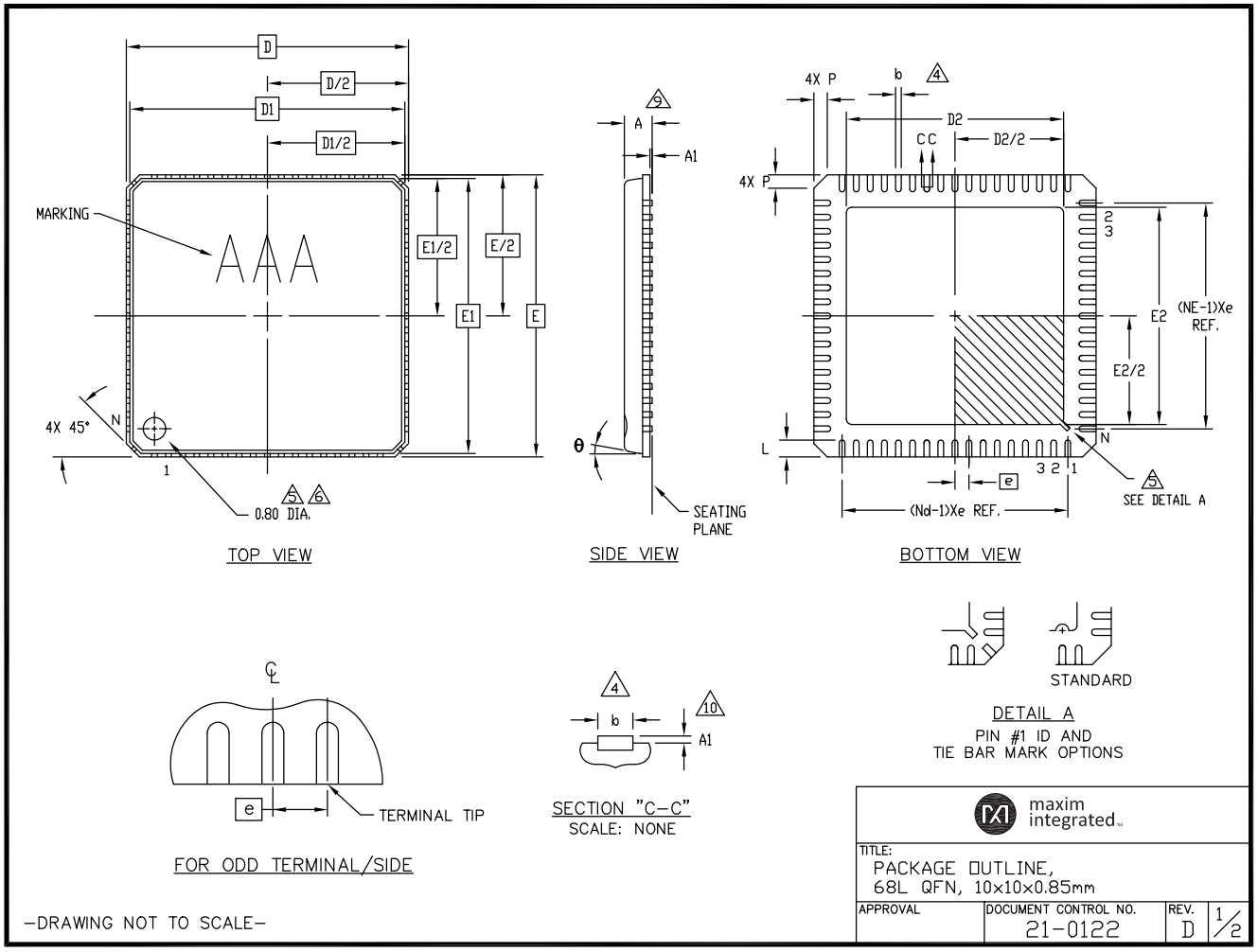
Pin Configuration



QFN-EP

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

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SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D	10.00 BSC			
D1	9.75 BSC			
e	0.50 BSC			
E	10.00 BSC			
E1	9.75 BSC			
L	0.50	0.60	0.65	
N	68			3
Nd	17			3
Ne	17			3
θ	0		12°	
P	0	0.42	0.60	

NOTES:

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.
12. MARKING SHOWN IS FOR PKG. ORIENTATION REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO LEADED (-) AND PbFREE (+) PKG. CODES.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

—DRAWING NOT TO SCALE—

maxim integrated

TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.85mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0122	D	2/2

Revision History

Pages changed at Rev 4: 2–5, 12, 13

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