USB4624

USB 2.0 HSIC Hi-Speed 4-Port Hub Controller

PRODUCT FEATURES

Datasheet

Highlights

- Hub Controller IC with 4 downstream ports
- High-Speed Inter-Chip (HSIC) support
  - Upstream port selectable between HSIC or USB 2.0
  - 2 downstream HSIC ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- Battery charging support for Apple® devices
- **FlexConnect**: Downstream port 1 able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB to I²C™/SPI bridge endpoint support
- USB Link Power Management (LPM) support
- SUSPEND pin for remote wakeup indication to host
- Start Of Frame (SOF) synchronized clock output pin
- Vendor Specific Messaging (VSM) support
- Enhanced OEM configuration options available through OTP or SMBus Slave Port
- Flexible power rail support
  - VBUS or VBAT only operation
  - 3.3V only operation
  - VBAT + 1.8V operation
  - 3.3V + 1.8V operation
- 48-pin (7x7mm) SQFN, RoHS compliant package

Target Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC mother boards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

Additional Features

- **MultiTRAK**™
  - Dedicated Transaction Translator per port
- **PortMap**
  - Configurable port mapping and disable sequencing
- **PortSwap**
  - Configurable differential intra-pair signal swapping
- **PHYBoost**™
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense**™
  - Programmable USB receiver sensitivity
- Low power operation
- Full Power Management with individual or ganged power control of each downstream port
- Built-in Self-Powered or Bus-Powered internal default settings provide flexibility in the quantity of USB expansion ports utilized without redesign
- Supports “Quad Page” configuration OTP flash
  - Four consecutive 200 byte configuration pages
- Fully integrated USB termination and Pull-up/Pull-down resistors
- On-chip Power On Reset (POR)
- Internal 3.3V and 1.2V voltage regulators
- On Board 24MHz Crystal Driver, Resonator, or External 24MHz clock input
- USB host/device speed indicator. Per-port 3-color LED drivers indicate the speed of USB host and device connection - hi-speed (480 Mbps), full-speed (12 Mbps), low-speed (1.5 Mbps)
- Environmental
  - Commercial temperature range support (0ºC to 70ºC)
  - Industrial temperature range support (-40ºC to 85ºC)

Order Number(s):

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
USB4624-1080HN	0°C to +70°C	48-pin SQFN
USB4624-1080HN-TR	0°C to +70°C	48-pin SQFN (Tape & Reel)
USB4624i-1080HN	-40°C to +85°C	48-pin SQFN
USB4624i-1080HN-TR	-40°C to +85°C	48-pin SQFN (Tape & Reel)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

The table above represents valid part numbers at the time of printing and may not represent parts that are currently available. For the latest list of valid ordering numbers for this product, please contact the nearest sales office.

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Chapter 1 General Description

The SMSC USB4624 is a low-power, OEM configurable, MTT (Multi-Transaction Translator) USB 2.0 hub controller with 4 downstream ports and advanced features for embedded USB applications. The USB4624 is fully compliant with the USB 2.0 Specification, USB 2.0 Link Power Management Addendum, High-Speed Inter-Chip (HSIC) USB Electrical Specification Revision 1.0, and will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The 4-port hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream (non-HSIC) ports. HSIC ports support only Hi-Speed operation.

The USB4624 has been specifically optimized for embedded systems where high performance, and minimal BOM costs are critical design requirements. Standby mode power has been minimized and reference clock inputs can be aligned to the customer's specific application. Flexible power rail options ease integration into energy efficient designs by allowing the USB4624 to be powered in a single-source (VBUS, VBAT, 3.3V) or a dual-source (VBAT + 1.8, 3.3V + 1.8) configuration. Additionally, all required resistors on the USB ports are integrated into the hub, including all series termination and pull-up/pull-down resistors on the D+ and D– pins.

The USB4624 supports both upstream battery charger detection and downstream battery charging. The USB4624 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. These circuits are used to detect the attachment and type of a USB charger and provide an interrupt output to indicate charger information is available to be read from the device's status registers via the serial interface. The USB4624 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The USB4624 provides an additional USB endpoint dedicated for use as a USB to I^2C/SPI interface, allowing external circuits or devices to be monitored, controlled, or configured via the USB interface. Additionally, the USB4624 includes many powerful and unique features such as:

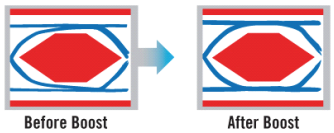
FlexConnect, which provides flexible connectivity options. The USB4624's downstream port 1 can be swapped with the upstream port, allowing master capable devices to control other devices on the hub.

MultiTRAK™ Technology, which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap, which provides flexible port mapping and disable sequences. The downstream ports of a USB4624 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB4624 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.



VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB4624 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range versions.

1.1 Block Diagram

Figure 1.1 details the internal block diagram of the USB4624.

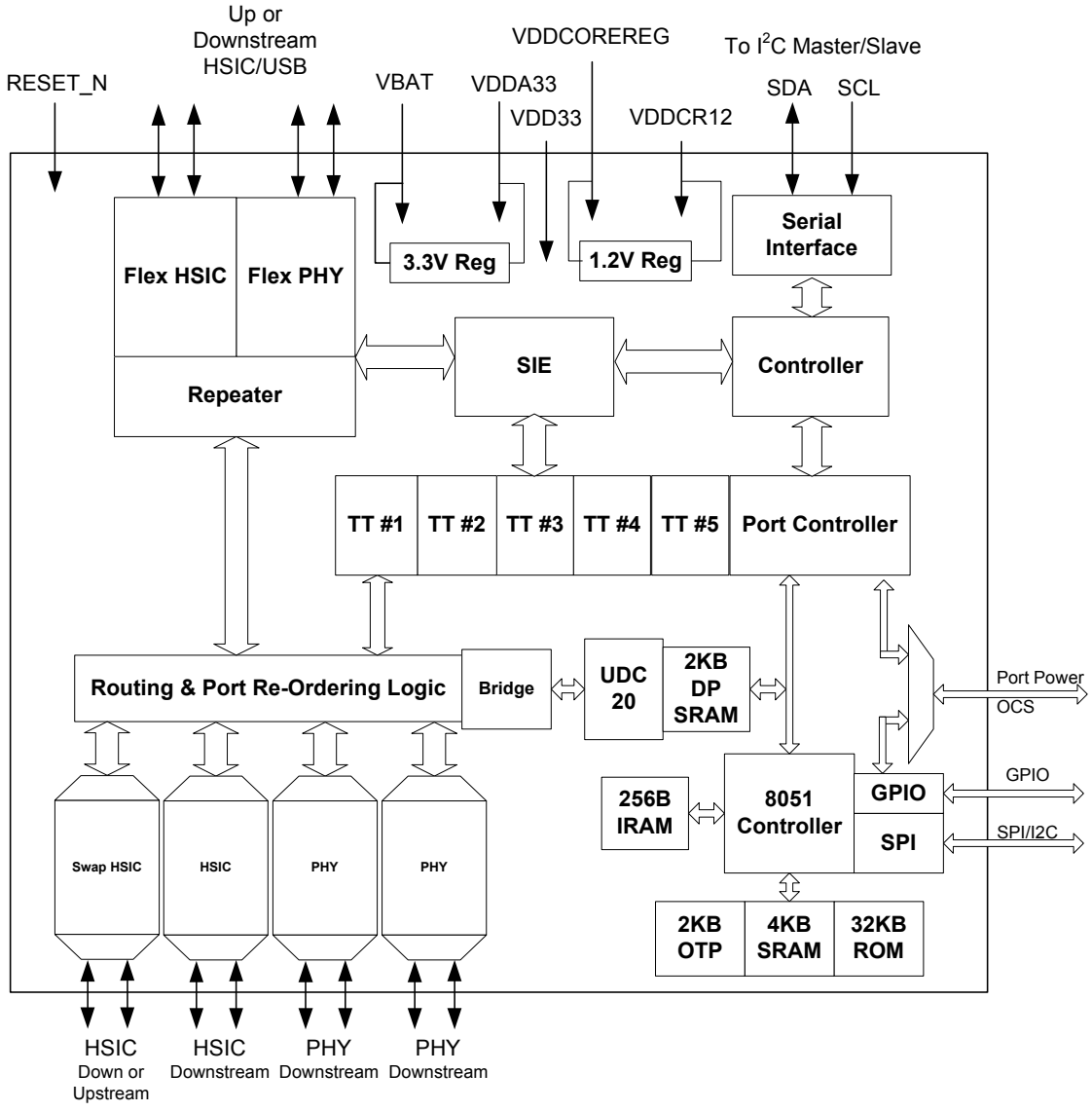


Figure 1.1 System Block Diagram

Chapter 2 Acronyms and Definitions

2.1 Acronyms

EOP: End of Packet

EP: Endpoint

FS: Full-Speed

GPIO: General Purpose I/O (that is input/output to/from the device)

HS: Hi-Speed

HSOS: High Speed Over Sampling

HSIC: High-Speed Inter-Chip

I^2C®: Inter-Integrated Circuit

LS: Low-Speed

OTP: One Time Programmable

PCB: Printed Circuit Board

PCS: Physical Coding Sublayer

PHY: Physical Layer

SMBus: System Management Bus

UUID: Universally Unique IDentification

2.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Specification*, Revision 2.0, April 27th, 2000, http://www.usb.org
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0, Sept. 23, 2007, http://www.usb.org
5. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
6. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

Chapter 3 Pin Descriptions

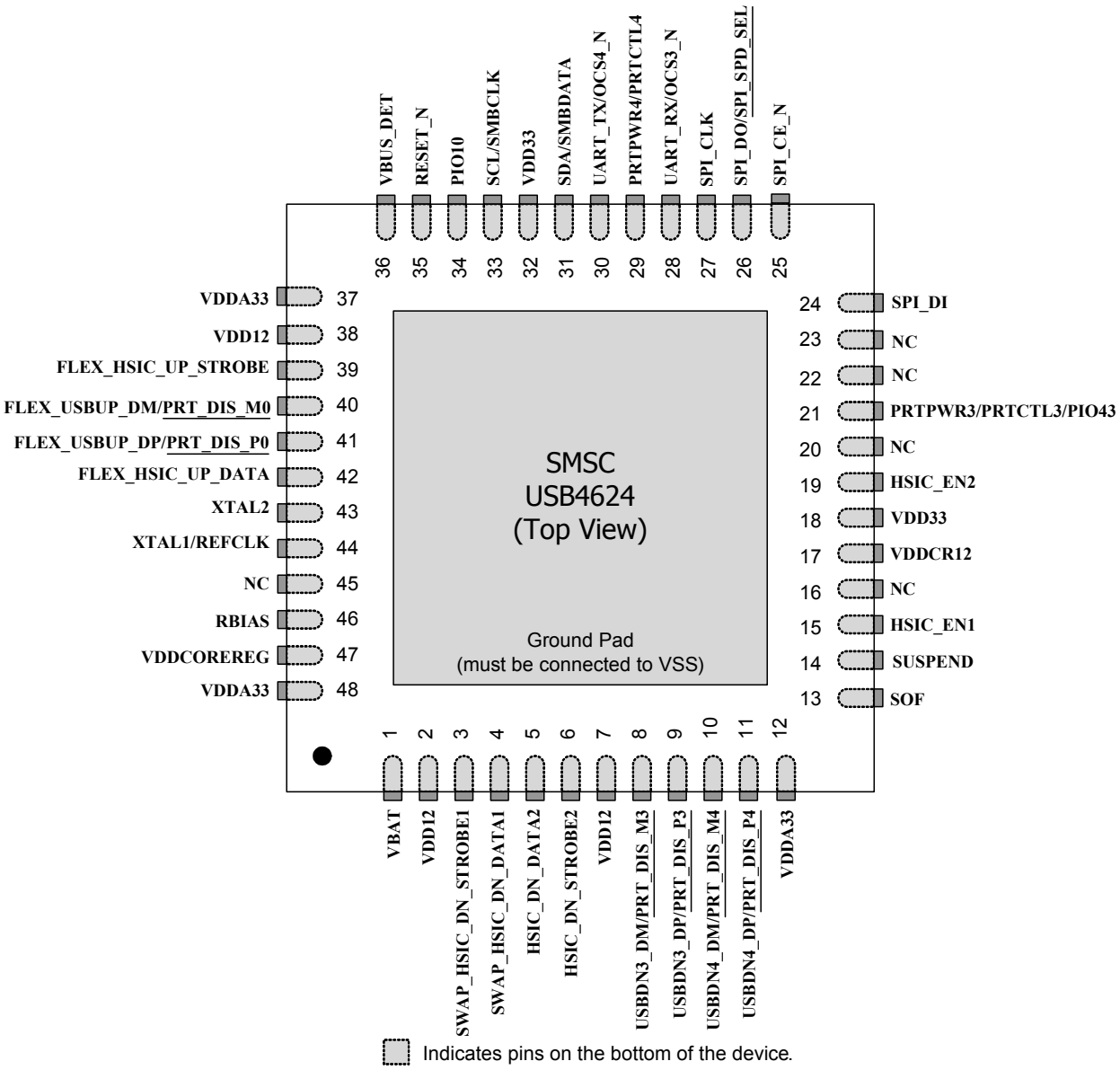


Figure 3.1 48-SQFN Pin Assignments

3.1 Pin Descriptions

This section provides a detailed description of each pin. The signals are arranged in functional groups according to their associated interface.

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column of Table 3.1. A description of the buffer types is provided in Section 3.3.

Table 3.1 Pin Descriptions

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
USB/HSIC INTERFACES				
1	Upstream USB D+ (Flex Port 0)	FLEX_USBUP_DP	AIO	Upstream USB Port 0 D+ data signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
	Port 0 D+ Disable Configuration Strap	PRT_DIS_P0	IS	This strap is used in conjunction with PRT_DIS_M0 to disable USB Port 0. 0 = Port 0 D+ Enabled 1 = Port 0 D+ Disabled **Note:** Both PRT_DIS_P0 and PRT_DIS_M0 must be tied to VDD33 at reset to place Port 0 into HSIC mode. See Note 3.3 for more information on configuration straps.
1	Upstream USB D- (Flex Port 0)	FLEX_USBUP_DM	AIO	Upstream USB Port 0 D- data signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
	Port 0 D- Disable Configuration Strap	PRT_DIS_M0	IS	This strap is used in conjunction with PRT_DIS_P0 to disable USB Port 0. 0 = Port 0 D- Enabled 1 = Port 0 D- Disabled **Note:** Both PRT_DIS_P0 and PRT_DIS_M0 must be tied to VDD33 at reset to place Port 0 into HSIC mode. See Note 3.3 for more information on configuration straps.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Upstream HSIC Data (Flex Port 0)	FLEX_HSIC_UP_DATA	HSIC	Upstream HSIC Port 0 DATA signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
1	Upstream HSIC Strobe (Flex Port 0)	FLEX_HSIC_UP_STROBE	HSIC	Upstream HSIC Port 0 STROBE signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
1	Downstream HSIC Data (Swap Port 1)	SWAP_HSIC_DN_DATA1	HSIC	Downstream HSIC Port 1 DATA signal. **Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals.
1	Downstream HSIC Strobe (Swap Port 1)	SWAP_HSIC_DN_STROBE1	HSIC	Downstream HSIC Port 1 STROBE signal. **Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals.
1	Downstream HSIC Data (Port 2)	HSIC_DN_DATA2	HSIC	Downstream HSIC Port 2 DATA signal.
1	Downstream HSIC Strobe (Port 2)	HSIC_DN_STROBE2	HSIC	Downstream HSIC Port 2 STROBE signal.
1	Downstream USB D+ (Port 3)	USBDN3_DP	AIO	Downstream USB Port 3 D+ data signal.
	Port 3 D+ Disable Configuration Strap	PRT_DIS_P3	IS	This strap is used in conjunction with PRT_DIS_M3 to disable USB Port 3. 0 = Port 3 D+ Enabled 1 = Port 3 D+ Disabled **Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Downstream USB D- (Port 3)	USBDN3_DM	AIO	Downstream USB Port 3 D- data signal.
	Port 3 D- Disable Configuration Strap	PRT_DIS_M3	IS	This strap is used in conjunction with PRT_DIS_P3 to disable USB Port 3. 0 = Port 3 D- Enabled 1 = Port 3 D- Disabled **Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
1	Downstream USB D+ (Port 4)	USBDN4_DP	AIO	Downstream USB Port 4 D+ data signal.
	Port 4 D+ Disable Configuration Strap	PRT_DIS_P4	IS	This strap is used in conjunction with PRT_DIS_M4 to disable USB Port 4. 0 = Port 4 D+ Enabled 1 = Port 4 D+ Disabled **Note:** Both PRT_DIS_P4 and PRT_DIS_M4 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
1	Downstream USB D- (Port 4)	USBDN4_DM	AIO	Downstream USB Port 4 D- data signal.
	Port 4 D- Disable Configuration Strap	PRT_DIS_M4	IS	This strap is used in conjunction with PRT_DIS_P4 to disable USB Port 4. 0 = Port 4 D- Enabled 1 = Port 4 D- Disabled **Note:** Both PRT_DIS_P4 and PRT_DIS_M4 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
I^2C/SMBUS INTERFACE				
1	I^2C Serial Clock Input	SCL	I_SMB	I^2C serial clock input
	SMBus Clock	SMBCLK	I_SMB	SMBus serial clock input

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	I^2C Serial Data	SDA	IS/OD8	I^2C bidirectional serial data
	SMBus Serial Data	SMBDATA	IS/OD8	SMBus bidirectional serial data
SPI MASTER INTERFACE				
1	SPI Chip Enable Output	SPI_CE_N	O12	Active-low SPI chip enable output. **Note:** If the SPI is enabled, this pin will be driven high in powerdown states.
1	SPI Clock Output	SPI_CLK	O12	SPI clock output
1	SPI Data Output	SPI_DO	O12	SPI data output
	SPI Speed Select Configuration Strap	SPI_SPD_SEL	IS (PD)	This strap is used to select the speed of the SPI. 0 = 30MHz (default) 1 = 60MHz **Note:** If the latched value on reset is 1, this pin is tri-stated when the chip is in the suspend state. If the latched value on reset is 0, this pin is driven low during a suspend state. See Note 3.3 for more information on configuration straps.
1	SPI Data Input	SPI_DI	IS (PD)	SPI data input
MISC.				
1	UART Receive Input	UART_RX	IS	Internal UART receive input **Note:** This is a 3.3V signal. For RS232 operation, an external 12V translator is required.
	Port 3 Over-Current Sense Input	OCS3_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 3.
1	UART Transmit Output	UART_TX	O8	Internal UART transmit output **Note:** This is a 3.3V signal. For RS232 operation, an external 12V driver is required.
	Port 4 Over-Current Sense Input	OCS4_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 4.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	System Reset Input	RESET_N	I_RST	This active-low signal allows external hardware to reset the device. **Note:** The active-low pulse must be at least 5us wide. Refer to Section 8.4.2, "External Chip Reset (RESET_N)," on page 53 for additional information.
1	Crystal Input	XTAL1	ICLK	External 24 MHz crystal input
	Reference Clock Input	REFCLK	ICLK	Reference clock input. The device may be alternatively driven by a single-ended clock oscillator. When this method is used, XTAL2 should be left unconnected.
1	Crystal Output	XTAL2	OCLK	External 24 MHz crystal output
1	External USB Transceiver Bias Resistor	RBIAS	AI	A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
1	Suspend Output	SUSPEND	PU	This signal is used to indicate that the entire hub has entered the USB suspend state and that VBUS current consumption should be reduced in accordance with the USB specification. Refer to Section 8.6, "Suspend (SUSPEND)," on page 54 for additional information. **Note:** SUSPEND must be enabled via the Protouch configuration tool.
1	SOF Synchronized 8KHz Clock Output	SOF	O8	This signal outputs an 8KHz clock synchronized with the USB Host SOF. **Note:** SOF output is controlled via the SOF_ENABLE bit in the UTIL_CONFIG1 register
1	Detect Upstream VBUS Power	VBUS_DET	IS	Detects state of upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50kΩ by 100kΩ) to provide 3.3V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3V or 5.0V through a resistor divider to provide 3.3V. In embedded applications, VBUS_DET may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 1 HSIC Enable	HSIC_EN1	O8/ OD8	Used to indicate the connection state to the downstream HSIC device attached to Port 1. 0 = Disconnect Port 1 HSIC 1 = Device ready to negotiate or sustain an HSIC connection on Port 1.
1	Port 2 HSIC Enable	HSIC_EN2	O8/ OD8	Used to indicate the connection state to the downstream HSIC device attached to Port 2. 0 = Disconnect Port 2 HSIC 1 = Device ready to negotiate or sustain an HSIC connection on Port 2.
1	Port 3 Power Output	PRTPWR3	O8	Enables power to a downstream USB device attached to Port 3. 0 = Power disabled on downstream Port 3 1 = Power enabled on downstream Port 3
	Port 3 Control	PRTCTL3	OD8/IS (PU)	When configured as PRTCTL3, this pin functions as both the Port 3 power enable output (PRTPWR3) and the Port 3 over-current sense input (OCS3_N). Refer to the PRTPWR3 and OCS3_N descriptions for additional information.
1	Port 4 Power Output	PRTPWR4	O8	Enables power to a downstream USB device attached to Port 4. 0 = Power disabled on downstream Port 4 1 = Power enabled on downstream Port 4
	Port 4 Control	PRTCTL4	OD8/IS (PU)	When configured as PRTCTL4, this pin functions as both the Port 4 power enable output (PRTPWR4) and the Port 4 over-current sense input (OCS4_N). Refer to the PRTPWR4 and OCS4_N descriptions for additional information.
5	No Connect	NC	-	This pin must be left floating for normal device operation.
POWER				
1	Battery Power Supply Input	VBAT	P	Battery power supply input. When VBAT is connected directly to a +3.3V supply from the system, the internal +3.3V regulator runs in dropout and regulator power consumption is eliminated. A 4.7 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 20 for power connection information.
3	+3.3V Analog Power Supply	VDDA33	P	+3.3V analog power supply. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 20 for power connection information.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
2	+3.3V Power Supply	VDD33	P	+3.3V power supply. These pins must be connected to VDDA33. Refer to Chapter 4, "Power Connections," on page 20 for power connection information.
1	+1.8-3.3V Core Power Supply Input	VDDCOREREG	P	+1.8-3.3V core power supply input to internal +1.2V regulator. This pin may be connected to VDD33 for single supply applications when VBAT equals +3.3V. Running in a dual supply configuration with VDDCOREREG at a lower voltage, such as +1.8V, may reduce overall system power consumption. In dual supply configurations, a 4.7 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 20 for power connection information.
1	+1.2V Core Power Supply	VDDCR12	P	+1.2V core power supply. In single supply applications or dual supply applications where 1.2V is not used, a 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 20 for power connection information.
3	+1.2V HSIC Power Supply Input	VDD12	P	+1.2V HSIC power supply input. Refer to Chapter 4, "Power Connections," on page 20 for power connection information.
Exposed Pad on package bottom (Figure 3.1)	Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

Note 3.2 When the device is configured to enable the HSIC upstream port, the USB Product ID (PID) will be 4624. When the device is configured to enable the USB upstream port, the USB PID will be 4524.

Note 3.3 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 6.3, "Device Configuration Straps," on page 29 for additional information.

3.2 Pin Assignments

Table 3.2 48-SQFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	VBAT	25	SPI_CE_N
2	VDD12	26	SPI_DO/SPI_SPD_SEL
3	HSIC_DN_STROBE1	27	SPI_CLK
4	HSIC_DN_DATA1	28	UART_RX/OCS3_N
5	HSIC_DN_DATA2	29	PRTPWR4/PRTCTL4
6	HSIC_DN_STROBE2	30	UART_TX/OCS4_N
7	VDD12	31	SDA/SMBDATA
8	USBDN3_DM/PRT_DIS_M3	32	VDD33
9	USBDN3_DP/PRT_DIS_P3	33	SCL/SMBCLK
10	USBDN4_DM/PRT_DIS_M4	34	NC
11	USBDN4_DP/PRT_DIS_P4	35	RESET_N
12	VDDA33	36	VBUS_DET
13	SOF	37	VDDA33
14	SUSPEND	38	VDD12
15	HSIC_EN1	39	FLEX_HSIC_UP_STROBE
16	NC	40	FLEX_USBUP_DM/PRT_DIS_M0
17	VDDCR12	41	FLEX_USBUP_DP/PRT_DIS_P0
18	VDD33	42	FLEX_HSIC_UP_DATA
19	HSIC_EN2	43	XTAL2
20	NC	44	XTAL1/REFCLK
21	PRTPWR3/PRTCTL3	45	NC
22	NC	46	RBIAS
23	NC	47	VDDCOREREG
24	SPI_DI	48	VDDA33

3.3 Buffer Type Descriptions

Table 3.3 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered input
I_RST	Reset Input
I_SMB	I^2C/SMBus Clock Input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
HSIC	*High-Speed Inter-Chip (HSIC) USB Specification, Version 1.0* compliant input/output
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Chapter 4 Power Connections

4.1 Integrated Power Regulators

The integrated 3.3V and 1.2V power regulators provide flexibility to the system in providing power the device. Several different configurations are allowed in order to align the power structure to supplies available in the system.

The regulators are controlled by RESET_N. When RESET_N is brought high, the 3.3V regulator will turn on. When RESET_N is brought low the 3.3V regulator will turn off.

4.1.1 3.3V Regulator

The device has an integrated regulator to convert from VBAT to 3.3V.

4.1.2 1.2V Regulator

The device has an integrated regulator to convert from a variable voltage input on VDDCOREREG to 1.2V. The 1.2V regulator is tolerant to the presence of low voltage (~0V) on the VDDCOREREG pin in order to support system power solutions where a supply is not always present in low power states.

The 1.2V regulator supports an input voltage range consistent with a 1.8V input in order to reduce power consumption in systems which provide multiple power supply levels. In addition, the 1.2V regulator supports an input voltage up to 3.3V for systems which provide only a single power supply. The device will support operation where the 3.3V regulator output can drive the 1.2V regulator input such that VBAT is the only required supply.

4.2 Power Configurations

The device supports operation with no back current when power is connected in each of the following configurations. Power connection diagrams for these configurations are included in Section 4.3, "Power Connection Diagrams," on page 22.

4.2.1 Single Supply Configurations

4.2.1.1 VBAT Only

VBAT must be tied to the VBAT system supply. VDD33, VDDA33, and VDDCOREREG must be tied together on the board. In this configuration the 3.3V and 1.2V regulators will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.2.1.2 3.3V Only

VBAT must be tied to the 3.3V system supply. VDD33, VDDA33, and VDDCOREREG must be tied together on the board. In this configuration the 3.3V regulator will operate in dropout mode and the 1.2V regulator will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.2.2 Dual Supply Configurations

4.2.2.1 VBAT + 1.8V

VBAT must be tied to the VBAT system supply. VDDCOREREG must be tied to the 1.8V system supply. In this configuration, the 3.3V regulator and the 1.2V regulator will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.2.2.2 3.3V + 1.8V

VBAT must be tied to the 3.3V system supply. VDDCOREREG must be tied to the 1.8V system supply. In this configuration the 3.3V regulator will operate in dropout mode and the 1.2V regulator will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.3 Power Connection Diagrams

Figure 4.1 illustrates the power connections for the USB4624 with various power supply configurations.

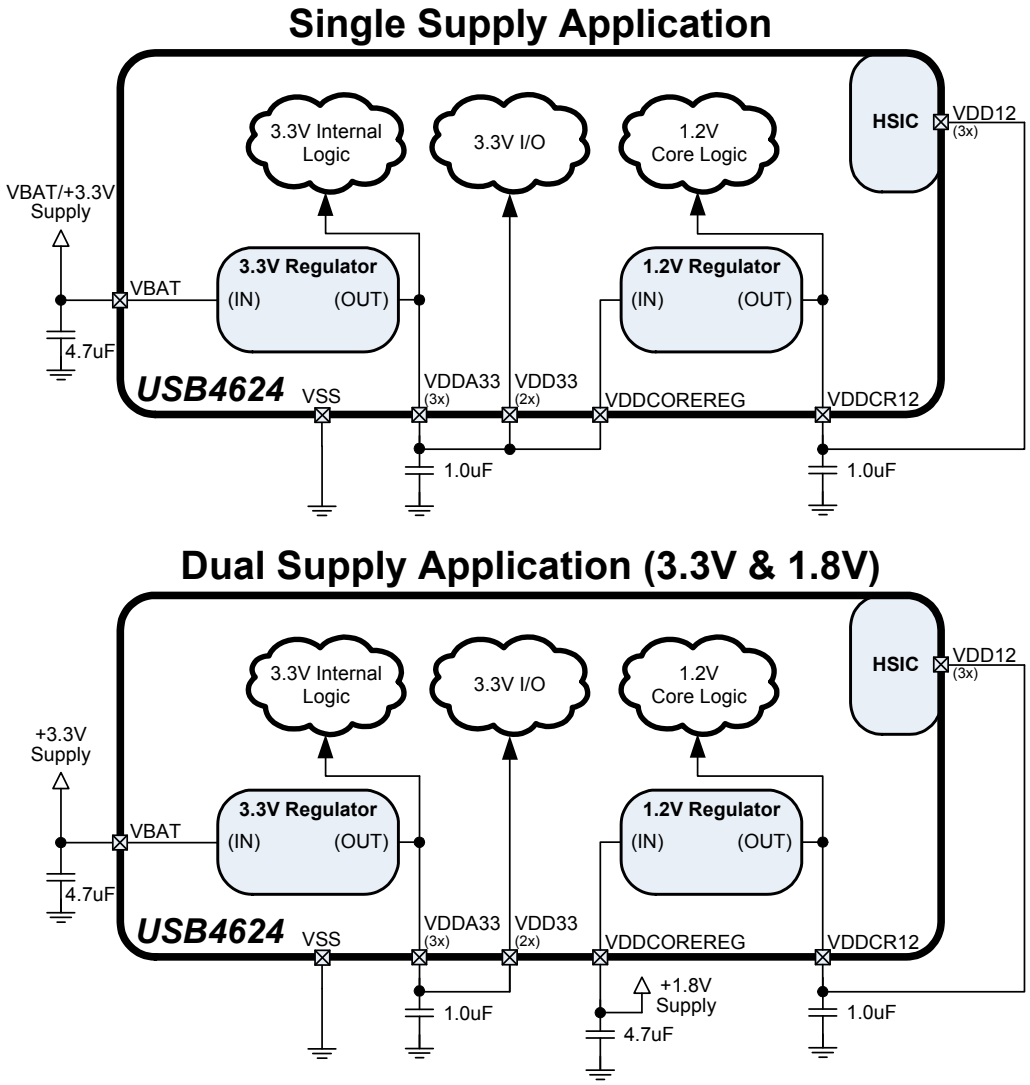


Figure 4.1 Power Connections

Note: To achieve the lowest power possible, tie the VDD12 pins to VDD12CR.

Chapter 5 Modes of Operation

The device provides two main modes of operation: Standby Mode and Hub Mode. The operating mode of the device is selected by setting values on primary inputs according to the table below.

Table 5.1 Controlling Modes of Operation

RESET_N INPUT	RESULTING MODE	SUMMARY
0	**Standby**	**Lowest Power Mode**: No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance. All regulators are powered off.
1	**Hub**	**Full Feature Mode**: Device operates as a configurable USB hub with battery charger detection. Power consumption is based on the number of active ports, their speed, and amount of data transferred.

Note: Refer to Section 8.4.2, "External Chip Reset (RESET_N)," on page 53 for additional information on RESET_N.

The flowchart in Figure 5.1 shows the modes of operation. It also shows how the device traverses through the Hub mode stages (shown in bold.) The flow of control is dictated by control register bits shown in italics as well as other events such as availability of a reference clock. The remaining sections in this chapter provide more detail on each stage and mode of operation.

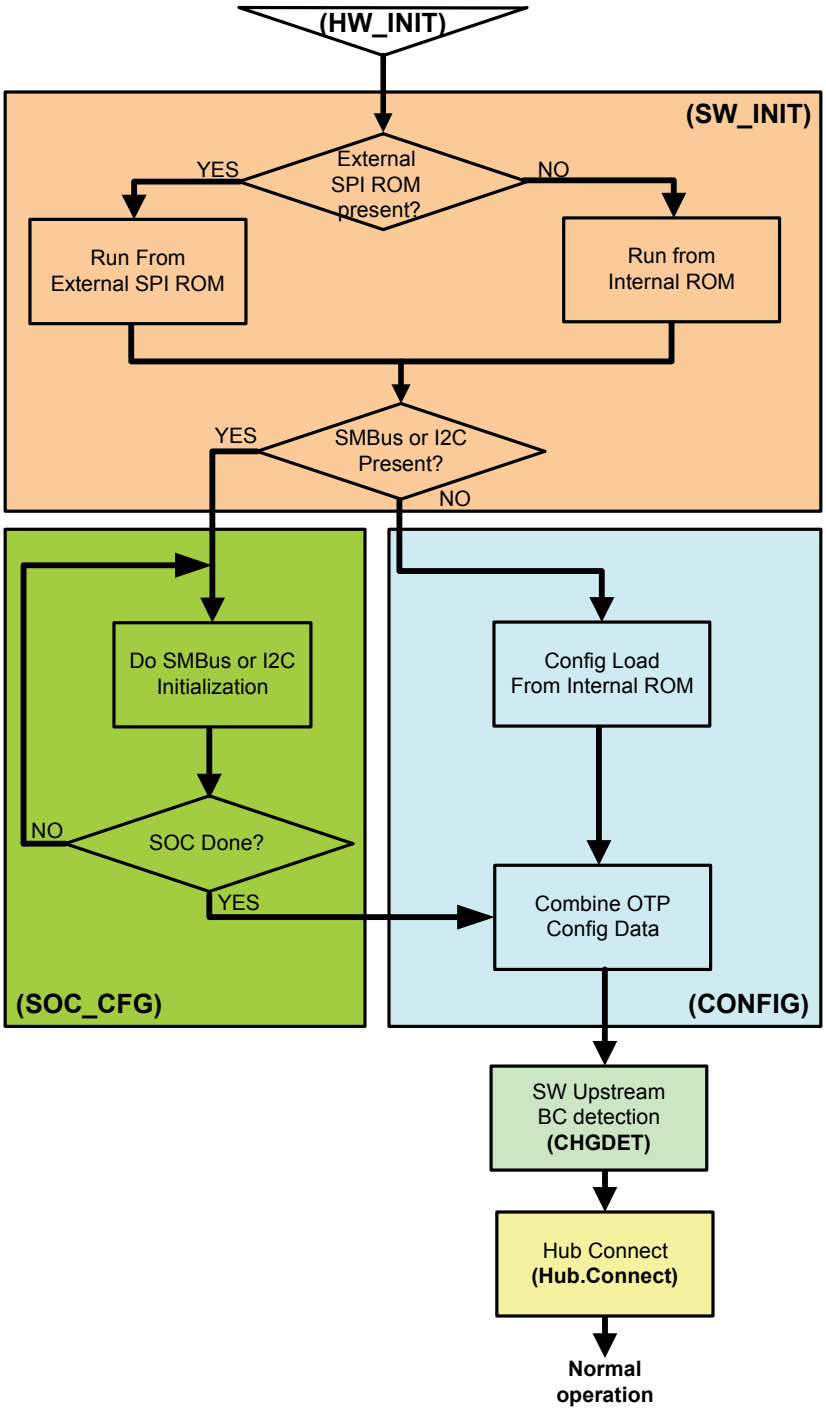


Figure 5.1 Hub Operational Mode Flowchart

5.1 Boot Sequence

5.1.1 Standby Mode

If the external hardware reset is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all internal regulators are powered off, the PLL is not running, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after RESET_N is negated high.

5.1.2 Hardware Initialization Stage (HW_INIT)

The first stage is the initialization stage and occurs on the negation of RESET_N. In this stage the 1.2V regulator is enabled and stabilizes, internal logic is reset, and the PLL locks if a valid REFCLK is supplied. Configuration registers are initialized to their default state and strap input values are latched. The device will complete initialization and automatically enter the next stage. Because the digital logic within the device is not yet stable, no communication with the device using the SMBus is possible. Configuration registers are initialized to their default state.

If there is a REFCLK present, the next state is SW_INIT.

5.1.3 Software Initialization Stage (SW_INIT)

Once the hardware is initialized, the firmware can begin to execute. The internal firmware checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of “2DFU” (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. SPI ROMs used with the device must be 1 Mbit and support either 30 MHz or 60 MHz. The frequency used is set using the SPI_SPD_SEL configuration strap. Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported. Refer to Section 6.3.2, "SPI Speed Select (SPI_SPD_SEL)," on page 30 for additional information on selection of the SPI speed.For all other configurations, the firmware checks for the presence of an external I^2C/SMBus. It does this by asserting two pull down resistors on the data and clock lines of the bus. The pull downs are typically 50Kohm. If there are 10Kohm pull-ups present, the device becomes aware of the presence of an external SMBus/I^2C bus. If a bus is detected, the firmware transitions to the SOC_CFG state.

5.1.4 SOC Configuration Stage (SOC_CFG)

In this stage, the SOC may modify any of the default configuration settings specified in the integrated ROM such as USB device descriptors, or port electrical settings, and control features such as upstream battery charging detection.

There is no time limit. In this stage the firmware will wait indefinitely for the SMBus/I^2C configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

5.1.5 Configuration Stage (CONFIG)

Once the SOC has indicated that it is done with configuration, then all the configuration data is combined. The default data, the SOC configuration data, the OTP data are all combined in the firmware and device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and upstream battery charging is enabled, the device will transition to the Battery Charger Detection Stage (CHGDET). If VBUS is present, and upstream battery charging is not enabled, the device will transitions to the Connect (Hub.Connect) stage.

5.1.6 Battery Charger Detection Stage (CHGDET)

After configuration, if enabled, the device enters the Battery Charger Detection Stage. If the battery charger detection feature was disabled during the CONFIG stage, the device will immediately transition to the Hub Connect (Hub.Connect) stage. If the battery charger detection feature remains enabled, the battery charger detection sequence is started automatically.

If the charger detection remains enabled, the device will transition to the Hub.Connect stage if using the hardware detection mechanism.

5.1.7 Hub Connect Stage (Hub.Connect)

Once the CHGDET stage is completed, the device enters the Hub.Connect stage.

5.1.8 Normal Mode

Lastly the SOC enters the Normal Mode of operation. In this stage, full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system. The only device registers accessible to the SOC are the run time registers described in Section 7.2.1, "SMBus Run Time Accessible Registers," on page 37.

If RESET_N is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated Hub stages. Asserting the soft disconnect on the upstream port will cause the Hub to return to the Hub.Connect stage until the soft disconnect is negated.

To save power, communication over the SMBus is not supported while in USB Suspend. The system can prevent the device from going to sleep by asserting the ClkSusp control bit of the Configure Portable Hub Register anytime before entering USB Suspend. While the device is kept awake during USB Suspend, it will provide the SMBus functionality at the expense of not meeting USB requirements for average suspend current consumption.

Chapter 6 Device Configuration

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface.

SMSC provides a comprehensive software programming tool, Pro-Touch, for configuring the USB4624 functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, contact your local SMSC sales representative.

6.1 Configuration Method Selection

The hub will interface to external memory depending on the configuration of the device pins associated with each interface type. The device will first check whether an external SPI ROM is present. If present, the device will operate entirely from the external ROM. When an external SPI ROM is not present, the device will check whether the SMBus is configured. When the SMBus is enabled, it can be used to configure the internal device registers via the XDATA address space, or to program the internal OTP memory. If no external options are detected, the device will operate using the internal default and configuration strap settings. The order in which device configuration is attempted is summarized below:

1. SPI (Reading the configuration from an SPI ROM)
2. SMBus (either writing the configuration registers in the XDATA address space, or to OTP)
3. Internal default settings (with or without configuration strap over-rides)

Note: Refer to Chapter 7, "Device Interfaces," on page 31 for detailed information on each device configuration interface.

6.2 Customer Accessible Functions

The following USB or SMBus accessible functions are available to the customer via the SMSC Pro-Touch Programming Tool.

Note: For additional programming details, refer to the SMSC Pro-Touch Programming Tool User Manual.

6.2.1 USB Accessible Functions

6.2.1.1 VSM commands over USB

By default, Vendor Specific Messaging (VSM) commands to the hub are enabled. The supported commands are:

- Enable Embedded Controller
- Disable Embedded Controller
- Enable Special Resume
- Disable Special Resume
- Reset Hub

6.2.1.2 SPI Access over USB

Access to an attached SPI device is performed as a pass-through operation from the USB Host. The device firmware has no knowledge of the operation of the attached SPI device. The supported commands are:

- Enable SPI pass through mode
- Disable SPI pass through mode
- SPI write
- SPI read

Note: Refer to Section 7.1, "SPI Interface," on page 31 for additional information on the SPI interface.

6.2.1.3 OTP Access over USB

The OTP ROM in the device is accessible via the USB bus. All OTP parameters can modified via the USB Host. The OTP operates in Single Ended mode. The supported commands are:

- Enable OTP reset
- Set OTP operating mode
- Set OTP read mode
- Program OTP
- Get OTP status
- Program OTP control parameters

6.2.1.4 Battery Charging Access over USB

The Battery charging behavior of the device can be dynamically changed by the USB Host when something other than the preprogrammed or OTP programmed behavior is desired. The supported commands are:

- Enable/Disable battery charging
- Upstream battery charging mode control
- Downstream battery charging mode control
- Battery charging timing parameters
- Download custom battery charging algorithm

6.2.1.5 Other Embedded Controller functions over USB

The following miscellaneous functions may be configured via USB:

- Enable/Disable Embedded controller enumeration
- Program Configuration parameters.
- Program descriptor fields:
  —Language ID
  —Manufacturer string
  —Product string
  —idVendor
  —idProduct
  —bcdDevice

6.2.2 SMBus Accessible Functions

6.2.2.1 OTP Access over SMBus

The device's OTP ROM is accessible over SMBus. All OTP parameters can modified via the SMbus Host. The OTP can be programmed to operate in Single-Ended, Differential, Redundant, or Differential Redundant mode, depending on the level of reliability required. The supported commands are:

- Enable OTP reset
- Set OTP operating mode
- Set OTP read mode
- Program OTP
- Get OTP Status
- Program OTP control parameters

6.2.2.2 Configuration Access over SMBus

The following functions are available over SMBus prior to the hub attaching to the USB host:

- Program Configuration parameters.
- Program descriptor fields:
  —Language ID
  —Manufacturer string
  —Product string
  —idVendor
  —idProduct
  —bcdDevice
- Program Control Register

6.2.2.3 Run time Access over SMBus

There is a limited number of registers that are accessible via the SMBus during run time operation of the device. Refer to Section 7.2.1, "SMBus Run Time Accessible Registers," on page 37 for details.

6.3 Device Configuration Straps

Configuration straps are multi-function pins that are driven as outputs during normal operation. During a Power-On Reset (POR) or an External Chip Reset (RESET_N), these outputs are tri-stated. The high or low state of the signal is latched following de-assertion of the reset and is used to determine the default configuration of a particular feature. Configuration straps are latched as a result of a Power-On Reset (POR) or a External Chip Reset (RESET_N). Configuration strap signals are noted in Chapter 3, "Pin Descriptions," on page 10 and are identified by an underlined symbol name. The following sub-sections detail the various configuration straps.

Configuration straps include internal resistors in order to prevent the signal from floating when unconnected. If a particular configuration strap is connected to a load, an external pull-up or pull-down should be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

Note: The system designer must guarantee that configuration straps meet the timing requirements specified in Section 9.5.2, "Reset and Configuration Strap Timing," on page 62 and Section 9.5.1, "Power-On Configuration Strap Valid Timing," on page 61. If configuration straps are not

at the correct voltage level prior to being latched, the device may capture incorrect strap values.

Note: Configuration straps must never be driven as inputs. If required, configuration straps can be augmented, or overridden with external resistors.

6.3.1 Port Disable (PRT_DIS_M*x*/PRT_DIS_P*x*)

These configuration straps disable the associated USB ports D- and D+ signals, respectively, where "*x*" is the USB port number. Both the negative "M" and positive "P" port disable configuration straps for a given USB port must be tied high at reset to disable the associated port.

Table 6.1 PRT_DIS_M*x*/PRT_DIS_P*x* Configuration Definitions

PRT_DIS_M*x*/PRT_DIS_P*x*	DEFINITION
'0'	Port *x* D-/D+ Signal is Enabled (Default)
'1'	Port *x* D-/D+ Signal is Disabled

6.3.2 SPI Speed Select (SPI_SPD_SEL)

This strap is used to select the speed of the SPI as follows:

Table 6.2 SPI_SPD_SEL Configuration Definitions

SPI_SPD_SEL	DEFINITION
'0'	30 MHz SPI Operation (Default)
'1'	60 MHz SPI Operation

Note: If the latched value on reset is 1, this pin is tri-stated when the chip is in the suspend state. If the latched value on reset is 0, this pin is driven low during a suspend state.

Chapter 7 Device Interfaces

The USB4624 provides multiple interfaces for configuration and external memory access. This chapter details the various device interfaces and their usage.

Note: For information on device configuration, refer to Chapter 6, "Device Configuration," on page 27.

7.1 SPI Interface

The device is capable of code execution from an external SPI ROM. On power up, the firmware looks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. The following sections describe the interface options to the external SPI ROM.

The SPI interface is always enabled after reset. It can be disabled by setting the SPI_DISABLE bit in the UTIL_CONFIG1 register.

Note: For SPI timing information, refer to Section 9.5.7, "SPI Timing," on page 63.

7.1.1 Operation of the Hi-Speed Read Sequence

The SPI controller will automatically handle code reads going out to the SPI ROM address. When the controller detects a read, the controller drives SPI_CE_N low, and outputs 0x0B, followed by the 24-bit address. The SPI controller outputs a DUMMY byte. The next eight clocks will clock-in the first byte. When the first byte is clocked-in, a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address is anything other than one more than the last address, the SPI controller will terminate the transaction by driving SPI_CE_N high. As long as the addresses are sequential, the SPI Controller will continue clocking data in.

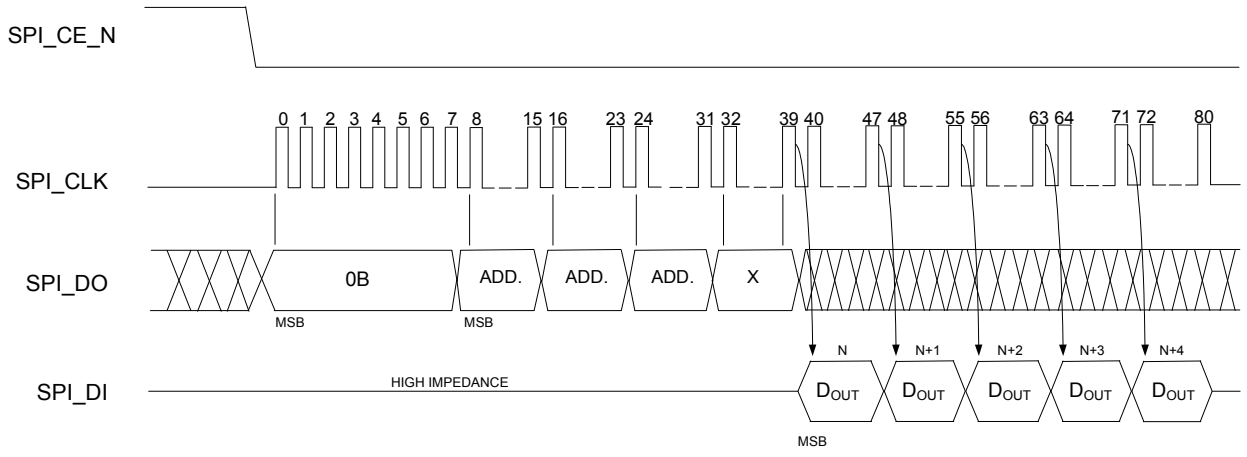


Figure 7.1 SPI Hi-Speed Read Sequence

7.1.2 Operation of the Dual High Speed Read Sequence

The SPI controller also supports dual data mode. When configured in dual mode, the SPI controller will automatically handle XDATA reads going out to the SPI ROM. When the controller detects a read, the controller drives SPI_CE_N low and outputs 0x3B (the value must be programmed into the SPI_FR_OPCODE Register) followed by the 24 bit address. Bits 23 through Bit 17 are forced to zero, and address bits 16 through 0 are directly from the XDATA address bus. Because it is in fast read mode, the SPI controller then outputs a DUMMY byte. The next four clocks will clock-in the first byte. The data appears two bits at a time on SPI_DO and SPI_DI. When the first byte is clocked in, a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by driving SPI_CE_N high. As long as the addresses are sequential, the SPI Controller will continue clocking data in.

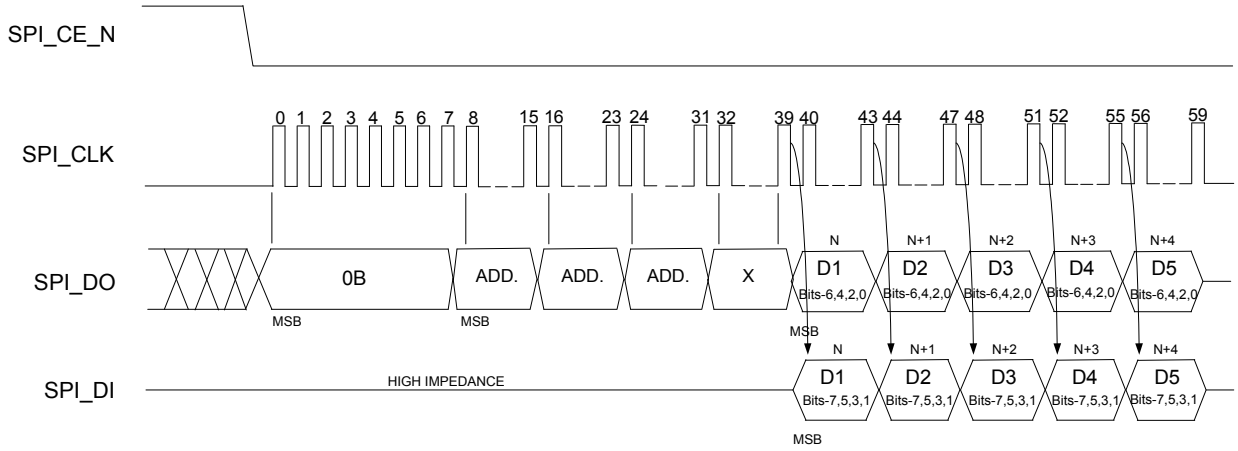


Figure 7.2 SPI Dual Hi-Speed Read Sequence

7.1.3 32 Byte Cache

There is a 32-byte pipeline cache with an associated base address pointer and length pointer. Once the SPI controller detects a jump, the base address pointer is initialized to that address. As each new sequential data byte is fetched, the data is written into the cache and the length is incremented. If the sequential run exceeds 32 bytes, the base address pointer is incremented to indicate the last 32 bytes fetched. If the firmware performs a jump, and the jump is in the cache address range, the fetch is done in 1 clock from the internal cache instead of an external access.

7.1.4 Interface Operation to the SPI Port When Not Performing Fast Reads

There is a 8-byte command buffer (SPI_CMD_BUF[7:0]), an 8-byte response buffer (SPI_RESP_BUF[7:0]), and a length register that counts out the number of bytes (SPI_CMD_LEN). Additionally, there is a self-clearing GO bit in the SPI_CTL register. Once the GO bit is set, device drives SPI_CE_N low and starts clocking. It will then output SPI_CMD_LEN x 8 number of clocks. After the first COMMAND byte has been sent out, the SPI_DI input is stored in the SPI_RESP buffer. If the SPI_CMD_LEN is longer than the SPI_CMD_BUF, don't cares are sent out on the SPI_DO output.

This mode is used for program execution out of internal RAM or ROM.

Automatic reads and writes happen when there is an external XDATA read or write, using the serial stream that has been previously discussed.

7.1.5 Erase Example

To perform a SCTR_ERASE, 32BLK_ERASE, or 64BLK_ERASE, the device writes 0x20, 0x52, or 0xD8, respectively to the first byte of the command buffer, followed by a 3-byte address. The length of the transfer is set to 4 bytes. To perform this, the device drives SPI_CE_N low, then counts out 8 clocks. It then outputs on SPI_DO the 8 bits of command, followed by 24 bits of address of the location to be erased. When the transfer is complete, SPI_CE_N goes high, while the SPI_DI line is ignored in this example.

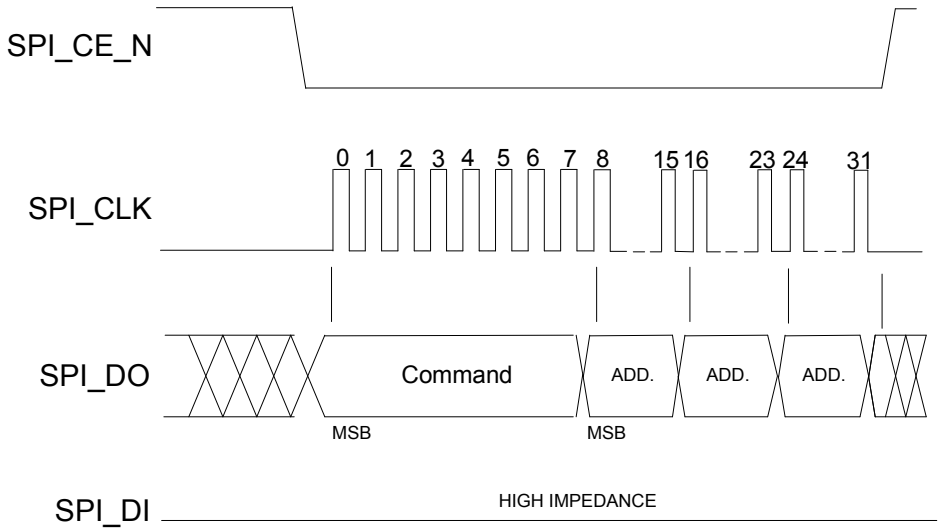


Figure 7.3 SPI Erase Sequence

7.1.6 Byte Program Example

To perform a Byte Program, the device writes 0x02 to the first byte of the command buffer, followed by a 3-byte address of the location that will be written to, and one data byte. The length of the transfer is set to 5 bytes. The device first drives SPI_CE_N low, then SPI_DO outputs 8 bits of command, followed by 24 bits of address, and one byte of data. SPI_DI is not used in this example.

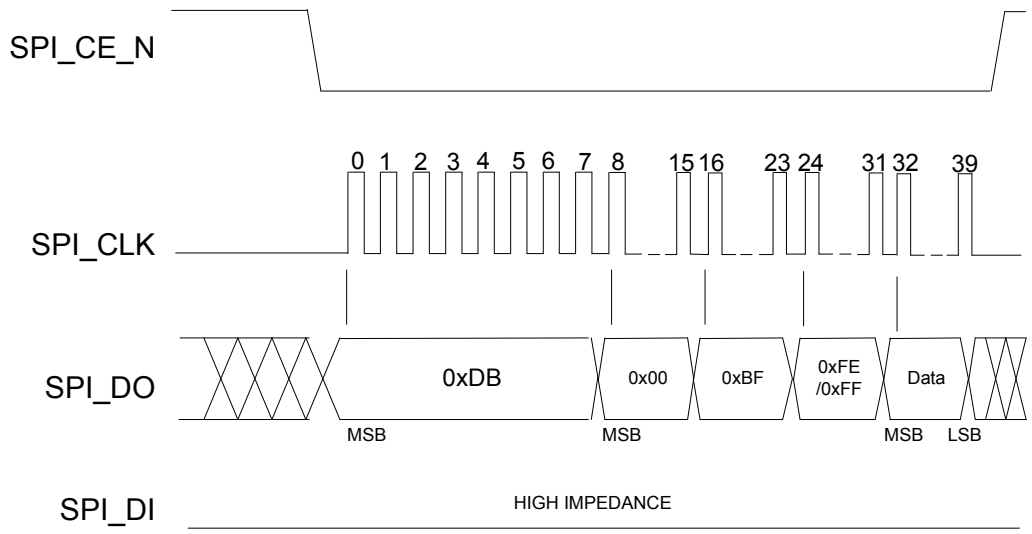


Figure 7.4 SPI Byte Program Sequence

7.1.7 Command Only Program Example

To perform a single byte command such as the following:

- WRDI
- WREN
- EWSR
- CHIP_ERASE
- EBSY
- DBSY

The device writes the opcode into the first byte of the SPI_CMD_BUF and the SPI_CMD_LEN is set to one. The device first drives SPI_CE_N low, then 8 bits of the command are clocked out on SPI_DO. SPI_DI is not used in this example.

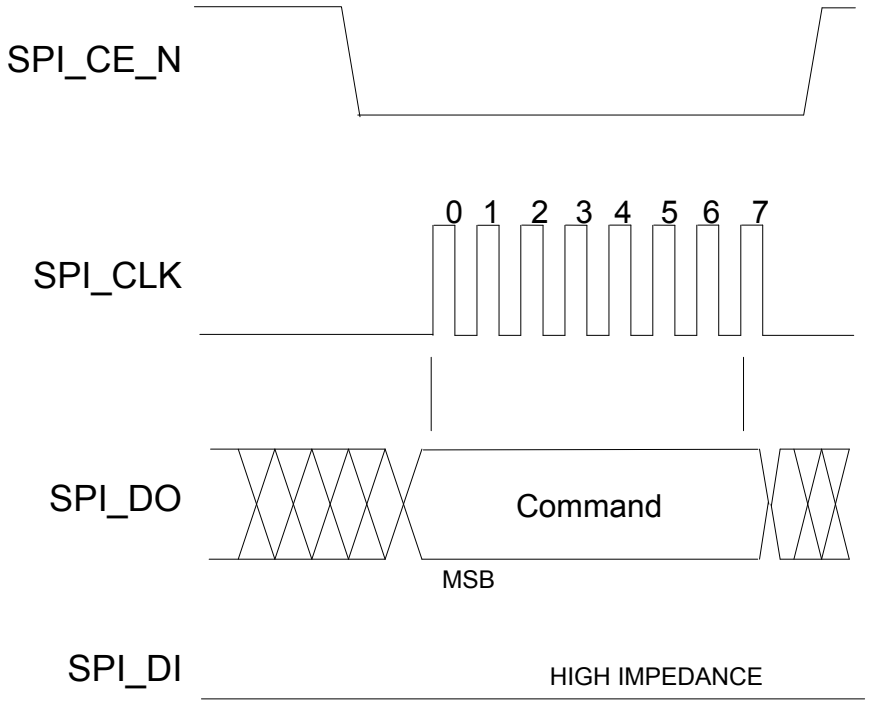


Figure 7.5 SPI Command Only Sequence

7.1.8 JEDEC-ID Read Example

To perform a JEDEC-ID command, the device writes 0x9F into the first byte of the SPI_CMD_BUF. The length of the transfer is 4 bytes. The device first drives SPI_CE_N low, then SPI_DO is output with 8 bits of the command, followed by the 24 bits of dummy bytes (due to the length being set to 4). When the transfer is complete, SPI_CE_N goes high. After the first byte, the data on SPI_DI is clocked into the SPI_RSP_BUF. At the end of the command, there are three valid bytes in the SPI_RSP_BUF. In this example, 0xBF, 0x25, 0x8E.

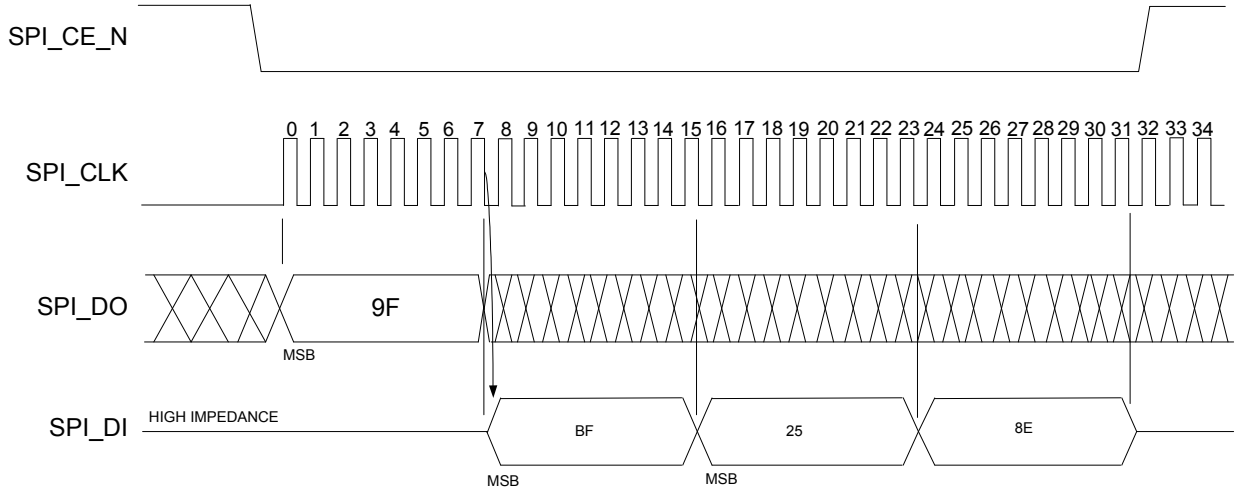


Figure 7.6 SPI JEDEC-ID Read Sequence

7.2 SMBus Slave Interface

The USB4624 includes an integrated SMBus slave interface, which can be used to access internal device run time registers or program the internal OTP memory. SMBus detection is accomplished by detection of pull-up resistors (10 KΩ recommended) on both the SMBDATA and SMBCLK signals. To disable the SMBus, a pull-down resistor of 10 KΩ must be applied to SMBDATA. The SMBus interface can be used to configure the device as detailed in Section 6.1, "Configuration Method Selection," on page 27.

Note: All device configuration must be performed via the SMSC Pro-Touch Programming Tool. For additional information on the Pro-Touch programming tool, contact your local SMSC sales representative.

7.2.1 SMBus Run Time Accessible Registers

Table 7.1 provides a summary of the SMBus accessible run time registers. Each register is detailed in the subsequent tables.

Note: The SMBus page register must be configured to allow the SOC to access the proper register space. Refer to Section 7.2.2, "Run Time SMBus Page Register," on page 48 for details.

Table 7.1 SMBus Accessible Run Time Registers

NAME	XDATA ADDR	
UP_BC_DET	0x30E2	Table 7.2, "Upstream Battery Charging Detection Control Register"
UP_CUST_BC_CTL	0x30E3	Table 7.3, "Upstream Custom Battery Charger Control Register"
UP_CUST_BC_STAT	0x30E4	Table 7.4, "Upstream Custom Battery Charger Status Register"
PORT_PWR_STAT	0x30E5	Table 7.5, "Port Power Status Register"
OCS_STAT	0x30E6	Table 7.6, "OCS Status Register"
BC_CHG_MODE	0x30EC	Table 7.7, "Upstream Battery Charger Mode Register"
CHG_DET_MSK	0x30ED	Table 7.8, "Charge Detect Mask Register"
CFGP	0x30EE	Table 7.9, "Configure Portable Hub Register"
PSELSUSP	0x318B	Table 7.10, "Port Select and Low-Power Suspend Register"
CONNECT_CFG	0x318E	Table 7.11, "Connect Configuration Register"
BC_CTL_1 (Upstream)	0x6100	Table 7.12, "Upstream (Port 0) Battery Charging Control 1 Register"
BC_CTL_2 (Upstream)	0x6101	Table 7.13, "Upstream (Port 0) Battery Charging Control 2 Register"
BC_CTL_RUN_TIME (Upstream)	0x6102	Table 7.14, "Upstream (Port 0) Battery Charging Run Time Control Register"
BC_CTL_DET (Upstream)	0x6103	Table 7.15, "Upstream (Port 0) Battery Charging Detect Register"

Table 7.2 Upstream Battery Charging Detection Control Register

UP_BC_DET (0x30E2 - RESET= 0x02)			UPSTREAM BATTERY CHARGING REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	CHARGER_TYPE	R/W	Read Only. This field indicates the result of the automatic charger detection. Values reported depend on EnhancedChrgDet bit setting in Upstream Battery Charger Mode Register. If EnhancedChrgDet = 1 000 = Charger Detection is not complete. 001 = DCP - Dedicated Charger Port 010 = CDP – Charging Downstream Port 011 = SDP – Standard Downstream Port 100 = Apple Low Current Charger 101 = Apple High Current Charger 110 = Apple Super High Current Charger 111 = Charger Detection Disabled If EnhancedChrgDet = 0 000 = Charger Detection is not complete. 001 = DCP/CDP – Dedicated Charger or Charging Downstream Port 010 = Reserved 011 = SDP – Standard Downstream Port 100 = Apple Low Current Charger 101 = Apple High Current Charger 110 = Apple Super High Current Charger 111 = Charger Detection Disabled
4	CHGDET_COMPLETE	R	Indicates Charger Detection has been run and is completed. This bit is negated when START_CHG_DET is asserted high.
3	Reserved	R/W	Reserved for debugging
2:1	CHG_DET[1:0]	R	Indicates encoded status of what chargers or status has been detected according to the settings in the Charge Detect Mask Register. It can be used to determine what current can be drawn from the upstream USB port. 00 = No selected Chargers or Status identified 01 = 100ma (VBUS detect without enumeration) 10 = 500ma (Device enumerated, Set Config seen) 11 = 1000+ma (Charger detected) The actual current amount for the charger will be system dependent
0	START_CHG_DET	R/W	Manually Initiates a USB battery charger detection sequence at the time of assertion. This bit must not be set while hub is in operation. This bit is cleared automatically when the manual battery charger detection sequence is completed. 0 = Write: No Effect / Read: Battery Charger Detection Sequence Completed or not run. 1 = Write: Start Battery Charger Detection / Read: Battery Charger Detection Sequence is running

Table 7.3 Upstream Custom Battery Charger Control Register

UP_CUST_BC_CTL (0x30E3 - RESET= 0x00)			UPSTREAM CUSTOM BATTERY CHARGING CONTROL
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	I2CControl	R/W	I^2C control 0: I^2C control disabled 1: I^2C control enabled
6	DmPulldownEn	R/W	DM 15K pull down resistor control 0: DM 15K pull down resistor disabled 1: DM 15K pull down resistor enabled
5	DpPulldownEn	R/W	DP 15K pull down resistor control 0: DP 15K pull down resistor disabled 1: DP 15K pull down resistor enabled
4	IdatSinkEn	R/W	Idat current sink control 0: Idat current sink disabled 1: Idat current sink enabled
3	HostChrgEn	R/W	Host charger detection swap control 0: Charger detection connections of DP and DM are not swapped (standard) 1: Charger detection connections of DP and DM are swapped. The USB signal path is not reversed.
2	VdatSrcEn	R/W	Vdat voltage source control 0: Vdat voltage source disabled 1: Vdat voltage source enabled
1	ContactDetectEn	R/W	Contact detect current source control 0: Contact detect current source disabled 1: Contact detect current source enabled
0	SeRxEn	R/W	Single-ended receiver control 0: Single-ended receiver disabled 1: Single-ended receiver enabled

Table 7.4 Upstream Custom Battery Charger Status Register

UP_CUST_BC_STAT (0x30E4 - RESET= 0x00)			UPSTREAM CUSTOM BATTERY CHARGING STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R	Reserved
3	RxHiCurr	R	DM high current Apple charger output 0: DM signal is not above the VSE_RXH threshold 1: DM signal is above the VSE_RXH threshold
2	DmSeRx	R	DM Single Ended Receiver Status
1	DpSeRx	R	DP Single Ended Receiver Status
0	VdatDet	R	Vdat detect 0: Vdat not detected 1: Vdat detect comparator output

Table 7.5 Port Power Status Register

PORT_PWR_STAT (0x30E5 - RESET= 0x00)			PORT POWER STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R	Reserved
4:1	PRTPWR[4:1]	R	Optional status to SOC indicating that power to the corresponding downstream port was enabled by the USB Host for the specified port. Not required for an embedded application. This is a read-only status bit. Actual control over port power is implemented by the USB Host, OCS Status Register and Downstream Battery Charging logic, if enabled. 0: USB Host has not enabled port to be powered or in downstream battery charging and corresponding OCS bit has been set 1: USB Host has enabled port to be powered
0	Reserved	R	Reserved

Table 7.6 OCS Status Register

OCS_STAT (0x30E6 - RESET= 0x00)			PORT POWER STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R	Reserved
4:1	OCS[4:1]	R	Optional control from SOC that indicates an over-current condition on the corresponding port for HUB status reporting to USB host. Also resets corresponding PRTPWR status bit in the Port Power Status Register. Not required for an embedded application. 0: No Over Current Condition 1: Over Current Condition
0	Reserved	R	Reserved

Table 7.7 Upstream Battery Charger Mode Register

BC_CHG_MODE (0x30EC - RESET= 0x00			UPSTREAM BATTERY CHARGER MODE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	Reserved	R	Reserved
5	HoldVdat	R/W	Dead Battery Vdat Detect voltage source enable 0: The charger detection state machine will turn off the Vdat Source at the end of the charger detection routine. 1: The charger detection state machine leave Vdat Source on during Hub.Connect stage when a SDP has been detected.
4	Reserved	R	Reserved
3	SE1ChrgDet	R/W	Apple type charger detection control 0: The charger detection routine will not look for the attachment of an Apple type charger. 1: The charger detection routine will look for the attachment of an Apple type charger.
2	EnhancedChrgDet	R/W	Enhanced charge detect control 0: The charger detection routine will not reverse Vdat SRC to differentiate between a CDP and a DCP. 1: The charger detection routine will reverse Vdat SRC to differentiate between a CDP and a DCP.
1:0	Reserved	R	Reserved

Table 7.8 Charge Detect Mask Register

CHG_DET_MSK (0x30ED - RESET= 0x1F)			CHARGE DETECT MASK
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	CONFIGURED	R/W	0: *battChg.chgDet* is not affected for this mask set when Hub is in a session and has been configured by the USB Host 1: *battChg.chgDet* indicates status for this mask set met when Hub is in a session and has been configured by the USB Host
6	CONNECTED	R/W	0: *battChg.chgDet* is not affected for this mask set when Hub has successfully connected with an upstream Host 1: *battChg.chgDet* indicates status for this mask set met when Hub has successfully connected with an upstream host.
5	SUSPENDED	R/W	0: *battChg.chgDet* is not affected for this mask set when Hub is in a session and has been suspended by the USB Host 1: *battChg.chgDet* indicates status for this mask set met when Hub is in a session and has been suspended by the USB Host
4	SE1SMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a Apple Super High Current Charger 1: *battChg.chgDet* indicates status for this mask set met when a SE1 (Apple) Super High Current Charger is detected
3	SE1HMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a Apple High Current Charger 1: *battChg.chgDet* indicates status for this mask set met when a Apple High Current Charger is detected
2	SE1LMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a Apple Low Current Charger 1: *battChg.chgDet* indicates status for this mask set met when a Apple Low Current Charger is detected
1	CDPMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a CDP Charger 1: *battChg.chgDet* indicates status for this mask set met when a CDP Charger is detected This mask bit should only be enabled if EnhancedChrgDet is asserted in the Upstream Battery Charger Mode Register. Without it, the charger detection is unable to identify a CDP.
0	DCPMask	R/W	0: *battChg.chgDet* is not affected for this mask set by detection of a DCP Charger 1: *battChg.chgDet* indicates status for this mask set met when a DCP Charger is detected

Table 7.9 Configure Portable Hub Register

CFGP (0x30EE - RESET= 0x10)			PORTABLE HUB CONFIGURATION REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	ClkSusp	R/W	0: Allow device to gate-off its internal clocks during suspend mode in order to meet USB suspend current requirements. 1: Force device to run internal clock even during USB suspend (will cause device to violate USB suspend current limit - intended for test or self-powered applications which require use of SMBus during USB session.)
6	Reserved	R	Always read ‘0’
5:1	DIS_CHP_PHY_CLK[5:1]	R/W	A ‘1’ disables the PHY clock of the corresponding port: Bit 5 - Downstream port 5 Bit 4 - Downstream port 4 Bit 3 - Downstream port 3 Bit 2 - Downstream port 2 Bit 1 - Downstream port 1
0	Reserved	R	Always read ‘0’

Table 7.10 Port Select and Low-Power Suspend Register

PSELSUSP (0x318B- RESET=0x00)			PORT SELECT AND LOW POWER SUSPEND REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	APortSel	R/W	Specifies which downstream USB port is associated with the PRTPWRA pin function. ‘00’ - Port 1 ‘01’ - Port 2 ‘10’ - Port 3 ‘11’ - Port 4
5:0	Reserved	R	Always read ‘0’

Note: This register should be assigned during the Hub.Config or Hub.Connect stages, and should not be dynamically updated during Hub.Communication stage or undefined behavior may result.

Table 7.11 Connect Configuration Register

CONNECT_CFG (0x318E- RESET=0x00)			CONNECT CONFIGURATION REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:2	Reserved	R	Reserved
1	EN_FLEX_MODE	R/W	Flex Connect mode enable 0: Flex Connect mode is disabled. (Normal hub operation with separate port power and OCS control) 1: Flex Connect mode is enabled
0	FLEXCONNECT	R/W	FlexConnect Control. When asserted the device changes its hub connections so that the Swap port (Physical Port 1) changes from it's default behavior of a downstream port to an upstream port. The Flex Port (Physical port 0) transitions from an upstream port to a downstream port. '0' - Flex Port = Upstream (Port 0) Swap Port= Downstream (Port 1) '1' - Flex Port= Downstream (Port 1) Swap Port= Upstream (Port 0) This setting can be used to select whether the Flex Port is an upstream or downstream port. The Flex Port provides both an HSIC and D+/D- connection, so the OEM can select whether this flexibility is provided on the upstream or downstream port. Another application for this setting is to allow a dual-role device on the Swap Port to assume a host role and communicate directly with other downstream hub ports, or to communicate through the Flex Port to a exposed connector to an external device. If a "private" communication channel is desired between embedded devices, any externally exposed ports should be disabled. Note: All port-specific settings such as VSNS, prtSp, sDiscon are specific to the logic port 0, 1, 2, 3. When FLEXCONNECT is asserted, these settings affect the newly assigned physical pins and PHY. Any settings which are specific to the physical Flex Port and Swap Port such as battery charger detection do not change with the setting of FLEXCONNECT.

Table 7.12 Upstream (Port 0) Battery Charging Control 1 Register

BC_CTL_1 (0x6100- RESET=0x00)			UPSTREAM (PORT 0) BATTERY CHARGING CONTROL 1 REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	USB2_IDP_SRC_EN	R/W	AFE 10uA I_{DP_SRC} current source Enable 0: Disabled (Hi Z) 1: Enabled
6	USB2_VDAT_SRC_EN	R/W	AFE 0.6V V_{DATA_SRC} voltage source Enable 0: Disabled (Hi Z) 1: Enabled
5	USB2_HOST_CHRG_EN	R/W	Enable charging host port mode 0: Portable Device 1: Charging Host port. When the charging host port is bit is set, the connections of V_{DATA_SRC}, I_{DAT_SINK}, I_{DP_SRC}, V_{DAT_DET} are reversed between DP and DM
4	USB2_IDAT_SINK_EN	R/W	AFE 100uA current sink and the V_{DAT_DET} comparator Enable 0: Disabled (Hi Z) 1: Enabled
3	USB2_VDAT_DET	R	V_{DAT_DET} comparator output 0: No voltage detected 1: Voltage detected (a possible charger or a device)
2	USB2_BC_DP_RDIV_EN	R/W	AFE Battery Charging Resistor Divider Enable – DP. 0: Disables resistor divider on DP. 1: Enables 2.7V voltage reference on DP through use of 9.7K/48.5K resistor divider.
1	USB2_BC_DM_RDIV_EN	R/W	AFE Battery Charging Resistor Divider Enable – DM. 0: Disables resistor divider on DM. 1: Enables 2.0V voltage reference on DM through use of 29.1K/48.5K resistor divider.
0	USB2_DP_DM_SHORT_EN	R/W	Sets the port into China battery charger mode.

Table 7.13 Upstream (Port 0) Battery Charging Control 2 Register

BC_CTL_2 (0x6101- RESET=0x00)			UPSTREAM (PORT 0) BATTERY CHARGING CONTROL 2 REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	BC_10_125K_PU_DP	R/W	Setting this bit enables a 125K pull-up to VDD33 on DP. This is used for USB battery charging in 1.0 mode detection only.
6	BC_10_125K_PU_DM	R/W	Setting this bit enables a 125K pull-up to VDD33 on DM. This is used for USB battery charging in 1.0 mode detection only.
5	LINESTATE_DP	R	This is the direct value of the Full-Speed USB line state Data Plus. It is used for battery charging detection. This line is not valid in HS mode and should only be used in battery charging detection.
4	LINESTATE_DM	R	This is the direct value of the Full-Speed USB line state Data Minus. It is used for battery charging detection. This line is not valid in HS mode and should only be used for battery charging detection.
3	USB2_FS_DP	R	This is the raw Full-Speed single ended receiver output for Data Plus
2	USB2_FS_DM	R	This is the raw Full-Speed single ended receiver output for Data Minus
1:0	Reserved	R	Always read ‘0’

Table 7.14 Upstream (Port 0) Battery Charging Run Time Control Register

BC_CTL_RUN_TIME (0x6102- RESET=0x00)			UPSTREAM (PORT 0) BATTERY CHARGING RUN TIME CONTROL REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	Reserved	R	Always read ‘0
6	SUSPENDN	R/W	Suspend enable. Forces upstream port into suspend 0: Suspend disabled 1: Suspend enabled
5	RESET	R/W	Reset enable. Forces upstream port into reset 0: Reset disabled 1: Reset enabled
4	USB2_FS_OEB	R/W	Output Enable (OE). Forces upstream port into output enable 0: OE disabled 1: OE enabled
3	RPD_DP_EN	R/W	Data plus resistor pull-down enable 0: Data plus pull-down disabled 1: Data plus pull-down enabled
2	RPD_DM_EN	R/W	Data minus resistor pull-down enable 0: Data minus pull-down disabled 1: Data minus pull-down enabled
1:0	XCVRSELECT	R/W	Transceiver Select. This field selects between the LS, FS and HS transceivers. 2'b00: HS mode 2'b01: FS mode 2'b10: LS mode 2'b11: LS data-rate with FS rise/fall times (and EOP/IDLE) **Note:** Note: XCVRSELECT must change state only when the device is not actively transmitting or receiving

Table 7.15 Upstream (Port 0) Battery Charging Detect Register

BC_CTL_DET (0x6103- RESET=0x00)			UPSTREAM (PORT 0) BATTERY CHARGING DETECT REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Always read ‘0
2	USB2_BC_RXHI_EN	R/W	Enable pin for the Apple high current battery charger detection.
1	USB2_BC_RXHI_DET	R	Output pin for the Apple high current battery charger detection. When disabled this output will be low.
0	USB2_BC_BIAS_EN	R/W	When enabling USB2_IDAT_SINK_EN or USB2_VDAT_SRC_EN of the Upstream (Port 0) Battery Charging Control 1 Register, this register bit must be set to enable the required current source.

7.2.2 Run Time SMBus Page Register

The following run time SMBus page register is located at 0xFF and must be programmed to allow the SOC to page through different pages of the register space.

Table 7.16 SMBus Page Register

SMBUS_PAGE (0xFF(I2C) - RESET= 0x00)			SMBUS PAGE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	PAGE_SEL	R/W	From the I^2C side, this field allows the I^2C to select the accessible address space: 000 = Select registers in the 3000 space (0x30e2 - 0x30ee) 010 = Select registers in the 3100 space (0x318b,0x318e) 110 = Select register in the 6100 space (0x6100,0x6101,0x6102)
5:0	Reserved	R	Reserved. **Note:** Software must never write a ‘1’ to these bits

Chapter 8 Functional Descriptions

This chapter provides additional functional descriptions of key device features.

8.1 Battery Charger Detection & Charging

The USB4624 supports both upstream battery charger detection and downstream battery charging. The integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. These circuits are used to detect the attachment and type of a USB charger and provide an interrupt output to indicate charger information is available to be read from the device's status registers via the serial interface. The USB4624 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The following sub-sections detail the upstream battery charger detection and downstream battery charging features.

8.1.1 Upstream Battery Charger Detection

Battery charger detection is available on the upstream facing port. The detection sequence is intended to identify chargers which conform to the Chinese battery charger specification, chargers which conform to the USB-IF Battery Charger Specification 1.2, and most Apple devices.

In order to detect the charger, the device applies and monitors voltages on the upstream DP and DM pins. If a voltage within the specified range is detected, the will be updated to reflect the proper status.

The device includes the circuitry required to implement battery charging detection using the Battery Charging Specification. When enabled, the device will automatically perform charger detection upon entering the Hub.ChgDet stage in Hub Mode. The device includes a state machine to provide the detection of the USB chargers listed in the table below. The type of charger detected is returned in the CHARGER_TYPE field of the .

Table 8.1 Chargers Compatible with Upstream Detection

USB ATTACH TYPE	DP/DM PROFILE	CHARGERTYPE
DCP (Dedicated Charging Port)	Shorted < 200ohm	001
CDP (Charging Downstream Port)	VDP reflected to VDM	010 (EnhancedChrgDet = 1)
SDP (Standard Downstream Port) USB Host or downstream hub port	15Kohm pull-down on DP and DM	011
Apple Low Current Charger	Apple	100
Apple High Current Charger	Apple	101
Apple Super High Current Charger	DP=2.7V DM=2.0V	110

Table 8.1 Chargers Compatible with Upstream Detection (continued)

USB ATTACH TYPE	DP/DM PROFILE	CHARGERTYPE
Apple Charger Low Current Charger (500mA)	DP=2.0V DM=2.0V	100
Apple Charger High Current Charger (1000mA)	DP=2.0V DM=2.7V	101

If a custom charger detection algorithm is desired, the SMBus registers can also be used to control the charger detection block to implement a custom charger detection algorithm. In order to avoid negative interactions with automatic battery charger detection or normal hub operation, the user should only attempt Custom battery charger detection during the Hub.Config stage or Hub.Connect stage. No logic is implemented to disable custom detection at other times - it is up to the user software to observe this restriction.

There is a possibility that the system is not running the reference clock when battery charger detection is required (for example if the battery is dead or missing). During the Hub.WaitRefClk stage the battery charger detection sequence can be configured to be followed regardless of the activity of REFCLK by relying on the operation of the internal oscillator.

Note: Battery charger detection is not available when utilizing HSIC on the upstream port.

8.1.2 Downstream Battery Charging

The device can be configured by an OEM to have any of the downstream ports to support battery charging. The Hub's role in battery charging is to provide an acknowledge to a device's query as to if the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided as externally by the OEM.

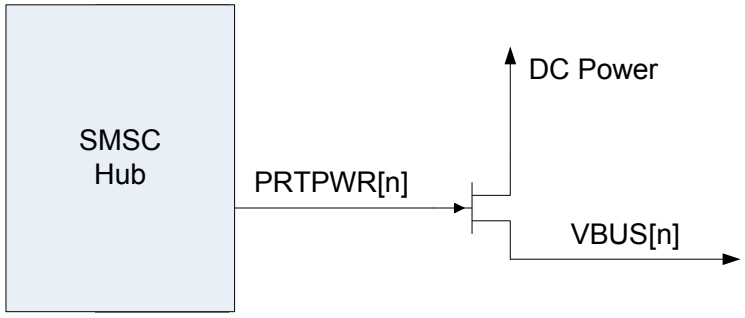


Figure 8.1 Battery Charging External Power Supply

If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply to the device. This indication, via the PRTPWR[1:4] output pins, is on a per/port basis. For example, the OEM can configure two ports to support battery charging through high current power FET's and leave the other two ports as standard USB ports.

Note: Battery charging is not available on downstream HSIC ports.

8.1.2.1 Downstream Battery Charging Modes

In the terminology of the USB Battery Charging Specification, if a port is configured to support battery charging, the downstream port is a considered a CDP (Charging Downstream Port) if connected to a USB host, or a DCP (Dedicated Charging Port) if not connected to a USB host. If the port is not configured to support battery charging, the port is considered an SDP (Standard Downstream Port). All charging ports have electrical characteristics different from standard non-charging ports.

A downstream port will behave as a CDP, DCP, or SDP depending on the port's configuration and mode of operation. The port will not switch between a CDP/DCP or SDP at any time after initial power-up and configuration. A downstream port can be in one of three modes shown in the table below.

Table 8.2 Downstream Port Types

USB ATTACH TYPE	DP/DM PROFILE
DCP (Dedicated Charging Port)	Apple charging mode or China Mode (Shorted < 200ohm) or SMSC custom mode
CDP (Charging Downstream Port)	VDP reflected to VDM
SDP (Standard Downstream Port) USB Host or downstream hub port	15Kohm pull-down on DP and DM

8.1.2.2 Downstream Battery Charging Configuration

Configuration of ports to support battery charging is performed via USB configuration, SMBus configuration, or OTP. The Battery Charging Enable Register provides per port battery charging configuration. Starting from bit 1, this register enables battery charging for each down stream port when asserted. Bit 1 represents port 1 and so on. Each port with battery charging enabled asserts the corresponding PRTPWR register bit.

8.1.2.3 Downstream Over-Current Management

It is the devices responsibility to manage over-current conditions. Over-Current Sense (OCS) is handled according to the USB specification. For battery charging ports, PRTPWR is driven high (asserted) after hardware initialization. If an OCS event occurs, the PRTPWR is negated. PRTPWR will be negated for all ports in a ganged configuration. Only the respective PRTPWR will be negated in the individual configuration.

If there is an over-current event in DCP mode, the port is turned off for one second and is then re-enabled. If the OCS event persists, the cycle is repeated for a total or three times. If after three attempts, the OCS still persists, the cycle is still repeated, but with a retry interval of ten seconds. This retry persists for indefinitely. The indefinite retry prevents a defective device from permanently disabling the port.

In CDP or SDP mode, the port power and over-current events are controlled by the USB host. The OCS event does not have to be registered. When and if the hub is connected to a host, the host will initialize the hub and enable its port power. If the over current still exists, it will be notified at that point.

8.2 SOF Clock Output

The USB4624 provides an 8Khz clock output synchronized to the USB host SOFs. The SOF output is generated from the previous SOF packet on the USB line. The device includes an internal free running frame counter to generate internal start of frame and end of frame events. The internal counter is re-synchronized every time a successful packet is received and decoded. The internal counter is advanced to compensate for the packet decode time. If the incoming SOF jitters early or late, the jitter will be visible in the next frame SOF output clock rising edge.

If one or two SOFs are missing, the SOF output will continue based on the internal frame counter. If more than two SOF are missing, the SOF output signal will stop. The clock is guaranteed to stop in a low state. When enabled or disabled, there will never be a short cycle.

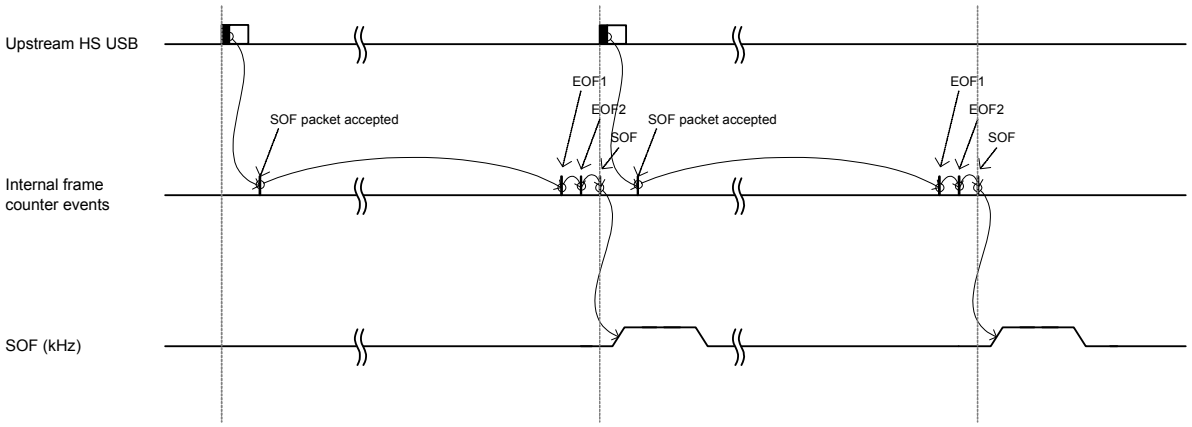


Figure 8.2 SOF Output Timing

8.3 Flex Connect

This feature allows the upstream port to be swapped with downstream physical port 1. Only downstream port 1 can be swapped physically. Using port remapping, any logical port (number assignment) can be swapped with the upstream port (non-physical).

Flex Connect is enabled/disabled via two control bits in the Connect Configuration Register. The FLEXCONNECT configuration bit switches the port, and EN_FLEX_MODE enables the mode.

8.3.1 Port Control

Once EN_FLEX_MODE bit is set, the functions of certain pins change, as outlined below.

If EN_FLEX_MODE is set and FLEXCONNECT is not set:

1. PRTPWR1 enters combined mode, becoming PRTPWR1/OCS1_N
2. SUSPEND outputs ‘0’ to keep any upstream power controller off

If EN_FLEX_MODE is set and FLEXCONNECT is set:

1. The normal upstream VBUS pin becomes a don’t care
2. PRTPWR1 is forced to a ‘1’ in combined mode, keeping the port power on to the application processor.
3. SUSPEND becomes PRTPWR1/OCS1_N for the port power controller for the connector port

8.4 Resets

The device has the following chip level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

8.4.1 Power-On Reset (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 9.5.1, "Power-On Configuration Strap Valid Timing," on page 61.

8.4.2 External Chip Reset (RESET_N)

A valid hardware reset is defined as assertion of RESET_N, after all power supplies are within operating range, per the specifications in Section 9.5.2, "Reset and Configuration Strap Timing," on page 62. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of RESET_N causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.
6. The HSIC Strobe and Data pins are driven low.

Note: All power supplies must have reached the operating levels mandated in Section 9.2, "Operating Conditions**," on page 56, prior to (or coincident with) the assertion of RESET_N.

8.4.3 USB Bus Reset

In response to the upstream port signaling a reset to the device, the device performs the following:

Note: The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to: Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The host then configures the device in accordance with the USB Specification.

8.5 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states per the USB 2.0 Link Power Management Addendum. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 8.3. For additional information, refer to the USB 2.0 Link Power Management Addendum.

Table 8.3 LPM State Definitions

STATE	DESCRIPTION	ENTRY/EXIT TIME TO L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms
L1	Sleep	Entry: ~65 us Exit: ~100 us
L0	Fully Enabled (On)	-

Note: State change timing is approximate and is measured by change in power consumption.

Note: System clocks are stopped only in suspend mode or when power is removed from the device.

8.6 Suspend (SUSPEND)

When enabled, the SUSPEND signal can be used to indicate that the entire hub has entered the USB suspend state and that VBUS current consumption should be reduced in accordance with the USB specification. Selective suspend set by the host on downstream hub ports have no effect on this signal because there is no requirement to reduce current consumption from the upstream VBUS. Suspend can be used by the system to monitor and dynamically adjust how much current the PMIC draws from VBUS to charge the battery in the system during a USB session. Because it is a level indication, it will assert or negate to reflect the current status of suspend without any interaction through the SMBus.

A negation of this signal indicates no level suspend interrupt and device has been configured by the USB Host. The full configured current can be drawn from the USB VBUS pin on the USB connector for charging - up to 500mA - depending on descriptor settings. When asserted, this signal indicates a suspend interrupt or that the device has not yet been configured by USB Host. The current draw can be limited by the system according to the USB specification. The USB specification limits current to 100mA before configuration, and up to 12.5mA in USB suspend mode.

Chapter 9 Operational Characteristics

9.1 Absolute Maximum Ratings*

VBAT Supply Voltage (Note 9.1). . . . . 0 V to +5.5 V

VDDCOREREG Supply Voltage (Note 9.1) . . . . . 0 V to +3.6 V

, Positive voltage on input signal pins, with respect to ground (Note 9.2) . . . . . 3.6 V

Negative voltage on input signal pins, with respect to ground (Note 9.3). . . . . -0.5 V

Positive voltage on XTAL1/REFCLK, with respect to ground VDDCR12

Positive voltage on HSIC signals, with respect to ground. . . . . 1.32 V

Positive voltage on USB DP/DM signals, with respect to ground (Note 9.4) . . . . . 5.5 V

Storage Temperature. . . . . .-55°C to +150°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . .JEDEC Class 3A

Note 9.1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 9.2 This rating does not apply to the following signals: All USB DM/DP pins, XTAL1/REFCLK, XTAL2, and all HSIC signals.

Note 9.3 This rating does not apply to the HSIC signals.

Note 9.4 This rating applies only when VDD33 is powered.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 9.2, "Operating Conditions**", Section 9.4, "DC Specifications", or any other applicable section of this specification is not implied. Note, device signals are NOT 5 volt tolerant unless specified otherwise.

9.2 Operating Conditions**

VBAT Supply Voltage . . . . . +3.0 V to +5.5 V

VDDCOREREG Supply Voltage . . . . . Note 9.5

Power Supply Rise Time . . . . . Note 9.6

Ambient Operating Temperature in Still Air (T_A). . . . . Note 9.7

Note 9.5 +1.6 V to +2.0 V when VDDCOREREG is connected to an external +1.8V power supply, +3.0 V to +3.6 V when VDDCOREREG is connected to VDD33.

Note 9.6 The power supply rise time requirements vary dependent on the usage of the external reset (RESET_N). If RESET_N is asserted at power-on, the power supply rise time must be 10mS or less ($t_{RT(max)}$ = 10mS). If RESET_N is not used at power-on (tied high), the power supply rise time must be 1mS or less ($t_{RT(max)}$ = 1mS). Higher voltage supplies must always be at an equal or higher voltage than lower voltage supplies. Figure 9.1 illustrates the supply rise time requirements.

Note 9.7 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

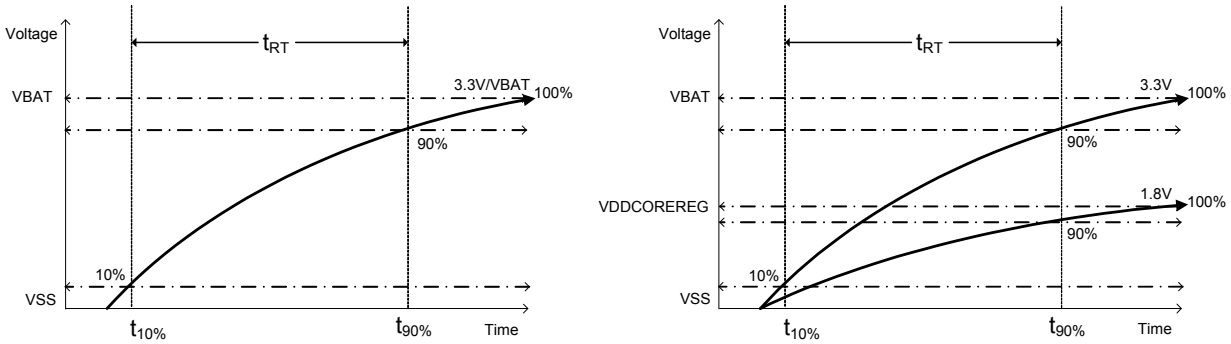


Figure 9.1 Single/Dual Supply Rise Time Models

9.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

9.3.1 Operational / Unconfigured

9.3.1.1 HSIC Upstream

Table 9.1 Operational/Unconfigured Power Consumption (HSIC Upstream)

	TYPICAL (mA)		MAXIMUM (mA)	
	VBAT	**VDDCOREREG (Note 9.8)**	**VBAT**	**VDDCOREREG (Note 9.8)**
HS Host / 1 HSIC Device	10	45	15	50
HS Host / 2 HSIC Devices	15	55	15	60
HS Host / 2 HSIC, 2 HS Devices	50	70	55	80
Unconfigured	10	20	-	-

Note 9.8 Includes VDD12 current.

9.3.1.2 USB Upstream

Table 9.2 Operational/Unconfigured Power Consumption (USB Upstream)

	TYPICAL (mA)		MAXIMUM (mA)	
	VBAT	**VDDCOREREG (Note 9.9)**	**VBAT**	**VDDCOREREG (Note 9.9)**
HS Host / 1 HSIC Device	15	50	20	55
HS Host / 2 HSIC Devices	15	60	20	65
HS Host / 2 HSIC, 2 HS Devices	55	70	65	80
Unconfigured	10	20	-	-

Note 9.9 Includes VDD12 current.

9.3.2 Suspend / Standby

9.3.2.1 Single Supply

The following tables detail the device power consumption when configured with a single VBAT supply and an externally supplied VDD12 for HSIC For additional information on power connections, refer to Chapter 4, "Power Connections," on page 20.

9.3.2.1.1 USB UPSTREAM

Table 9.3 Single Supply Suspend/Standby Power Consumption (USB Upstream)

MODE	SYMBOL	TYPICAL @ 25°C	COMMERCIAL MAX	INDUSTRIAL MAX	UNIT
Suspend	I_{VBAT}	330	1200	1750	uA
	I_{VDD12}	5	550	800	uA
Standby	I_{VBAT}	0.2	2.0	2.4	uA

Note: Typical values measured with VBAT = 4.2V, VDD12 = 1.2V. Maximum values measured with VBAT = 5.5V, VDD12 = 1.32V.

9.3.2.1.2 HSIC UPSTREAM

Table 9.4 Single Supply Suspend/Standby Power Consumption (HSIC Upstream)

MODE	SYMBOL	TYPICAL @ 25°C	COMMERCIAL MAX	INDUSTRIAL MAX	UNIT
Suspend	I_{VBAT}	120	1200	1450	uA
	I_{VDD12}	5	600	800	uA
Standby	I_{VBAT}	0.2	1.9	2.3	uA

Note: Typical values measured with VBAT = 4.2V, VDD12 = 1.2V. Maximum values measured with VBAT = 5.5V, VDD12 = 1.32V.

9.3.2.2 Dual Supply

The following tables detail the device power consumption when configured with a dual supply (VBAT and 1.8V VDDCOREREG) and an externally supplied VDD12 for HSIC For additional information on power connections, refer to Chapter 4, "Power Connections," on page 20.

9.3.2.2.1 USB UPSTREAM

Table 9.5 Dual Supply Suspend/Standby Power Consumption (USB Upstream)

MODE	SYMBOL	TYPICAL @ 25°C	COMMERCIAL MAX	INDUSTRIAL MAX	UNIT
Suspend	$I_{VDDCOREREG}$	90	1000	1550	uA
	I_{VBAT}	230	300	700	uA
	I_{VDD12}	6.5	700	1000	uA
Standby	$I_{VDDCOREREG}$	0.1	1.4	2.5	uA
	I_{VBAT}	0.4	2.1	2.5	uA

Note: Typical values measured with VBAT = 4.2V, VDDCOREREG = 1.8V, VDD12 = 1.2V. Maximum values measured with VBAT = 5.5V, VDDCOREREG = 2.0V, VDD12 = 1.32V.

9.3.2.2.2 HSIC UPSTREAM

Table 9.6 Dual Supply Suspend/Standby Power Consumption (USB Upstream)

MODE	SYMBOL	TYPICAL @ 25°C	COMMERCIAL MAX	INDUSTRIAL MAX	UNIT
Suspend	$I_{VDDCOREREG}$	90	900	1300	uA
	I_{VBAT}	30	550	750	uA
	I_{VDD12}	6.5	700	1100	uA
Standby	$I_{VDDCOREREG}$	0.1	1.2	2.5	uA
	I_{VBAT}	2.0	2.1	2.5	uA

Note: Typical values measured with VBAT = 4.2V, VDDCOREREG = 1.8V, VDD12 = 1.2V. Maximum values measured with VBAT = 5.5V, VDDCOREREG = 2.0V, VDD12 = 1.32V.

9.4 DC Specifications

Table 9.7 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
IS Type Input Buffer						
Low Input Level	V_{IL}	-0.3		0.8	V	
High Input Level	V_{IH}	2.0		3.6	V	
I_RST Type Input Buffer						
Low Input Level	V_{IL}	-0.3		0.4	V	
High Input Level	V_{IH}	1.25		3.6	V	
I_SMB Type Input Buffer						
Low Input Level	V_{IL}	-0.3		0.35	V	
High Input Level	V_{IH}	1.25		3.6	V	
O8 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	VDD33 - 0.4			V	I_{OH} = -8 mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
O12 Type Buffers						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	VDD33 - 0.4			V	I_{OH} = -12 mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
HSIC Type Buffers						
Low Input Level	V_{IL}	-0.3		0.35*VDD12	V	
High Input Level	V_{IH}	0.65*VDD12		VDD12+0.3	V	
Low Output Level	V_{OL}			0.25*VDD12	V	
High Output Level	V_{OH}	0.75*VDD12			V	
ICLK Type Buffer (XTAL1/REFCLK Input)						Note 9.10
Low Input Level	V_{IL}	-0.3		0.35	V	
High Input Level	V_{IH}	0.8		VDDCR12	V	

Note 9.10 XTAL2 can optionally be driven from a 24 MHz single-ended clock oscillator (REFCLK).

9.5 AC Specifications

This section details the various AC timing specifications of the device.

9.5.1 Power-On Configuration Strap Valid Timing

Figure 9.1 illustrates the configuration strap timing requirements, in relation to power-on, for applications where RESET_N is not used at power-on. The operational levels (V_{opp}) for the external power supplies are detailed in Section 9.2, "Operating Conditions**," on page 56.

Note: For RESET_N configuration strap timing requirements, refer to Section 9.5.2, "Reset and Configuration Strap Timing," on page 62.

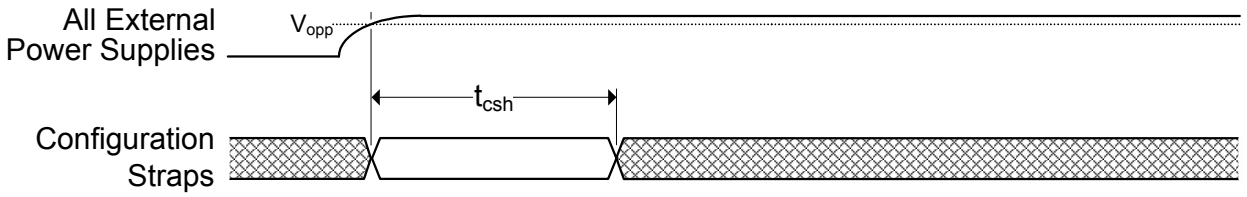


Figure 9.1 Power-On Configuration Strap Valid Timing

Table 9.8 Power-On Configuration Strap Valid Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{csh}	Configuration strap hold after external power supplies at operational levels	1			ms

9.5.2 Reset and Configuration Strap Timing

Figure 9.2 illustrates the RESET_N timing requirements and its relation to the configuration strap signals. Assertion of RESET_N is not a requirement. However, if used, it must be asserted for the minimum period specified.

Refer to Section 8.4, "Resets," on page 53 for additional information on resets. Refer to Section 6.3, "Device Configuration Straps," on page 29 for additional information on configuration straps.

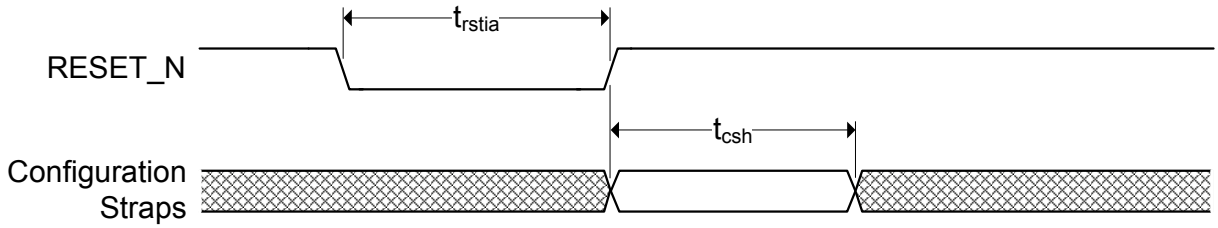


Figure 9.2 RESET_N Configuration Strap Timing

Table 9.9 RESET_N Configuration Strap Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{rstia}	RESET_N input assertion time	5			us
t_{csh}	Configuration strap hold after RESET_N deassertion	1			ms

9.5.3 USB Timing

All device USB signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Specification*. Please refer to the *Universal Serial Bus Specification*, Revision 2.0, available at http://www.usb.org.

9.5.4 HSIC Timing

All device HSIC signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *High-Speed Inter-Chip USB Electrical Specification*. Please refer to the *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0, available at http://www.usb.org.

9.5.5 SMBus Timing

All device SMBus signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification*. Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

9.5.6 I^2C Timing

All device I^2C signals conform to the 100KHz Standard Mode (Sm) voltage, power, and timing characteristics/specifications as set forth in the *I^2C-Bus Specification*. Please refer to the *I^2C-Bus Specification*, available at http://www.nxp.com.

9.5.7 SPI Timing

The following specifies the SPI timing requirements for the device.

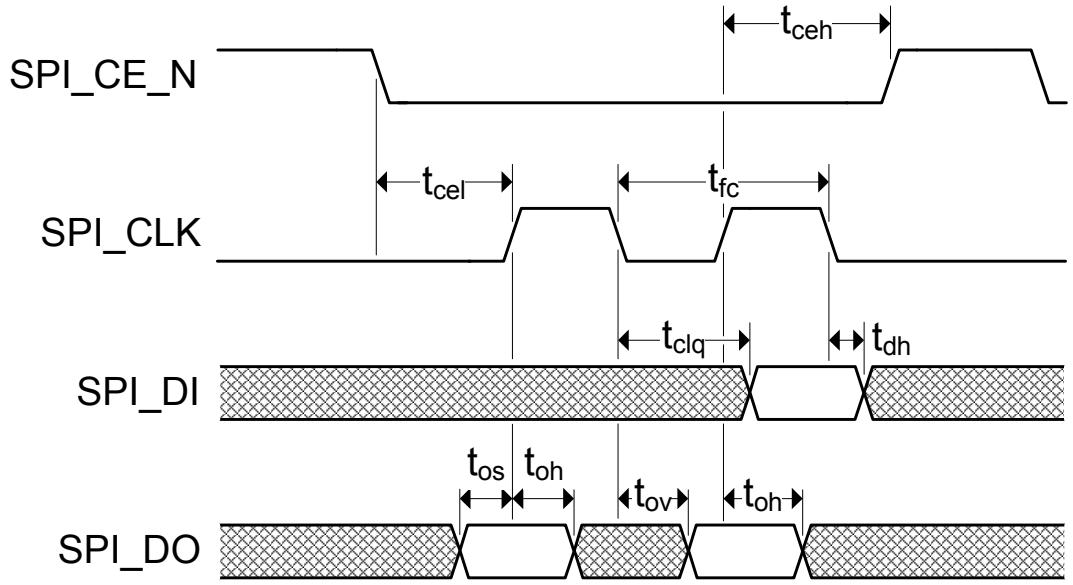


Figure 9.3 SPI Timing

Note: The SPI can be configured for 30 MHz or 60 MHz operation via the SPI_SPD_SEL configuration strap. 30 MHz operation timing values are shown in Table 9.10. 60 MHz operation timing values are shown in Table 9.11.

Table 9.10 SPI Timing Values (30 MHz Operation)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{fc}	Clock frequency			30	MHz
t_{ceh}	Chip enable (SPI_CE_EN) high time	100			ns
t_{clq}	Clock to input data			13	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (SPI_CE_EN) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (SPI_CE_EN) high	12			ns

Table 9.11 SPI Timing Values (60 MHz Operation)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{fc}	Clock frequency			60	MHz
t_{ceh}	Chip enable (SPI_CE_EN) high time	50			ns
t_{clq}	Clock to input data			9	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (SPI_CE_EN) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (SPI_CE_EN) high	12			ns

9.6 Clock Specifications

The device can accept either a 24 MHz crystal or a 24 MHz single-ended clock oscillator input. If the single-ended clock oscillator method is implemented, XTAL1 should be left unconnected and REFCLK should be driven with a clock that adheres to the specifications outlined in Section 9.6.2, "External Reference Clock (REFCLK)".

9.6.1 Oscillator/Crystal

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTAL1I/XTAL2). See Table 9.12 for the recommended crystal specifications.

Table 9.12 Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	24.000	-	MHz	
Total Allowable PPM Budget		-	-	+/-350	PPM	
Operating Temperature Range		Note 9.11	-	Note 9.12	^{o}C	

Note 9.11 0^{o}C for commercial version, -40^{o}C for industrial version.

Note 9.12 +70^{o}C for commercial version, +85^{o}C for industrial version.

9.6.2 External Reference Clock (REFCLK)

The following input clock specifications are suggested:

- 50% duty cycle ± 10%
- 24 MHz ± 350 PPM

Note: The external clock is recommended to conform to the signalling levels designated in the JEDEC specification on 1.2V CMOS Logic. XTAL2 should be treated as a no connect when an external clock is supplied.

Chapter 10 Package Outline

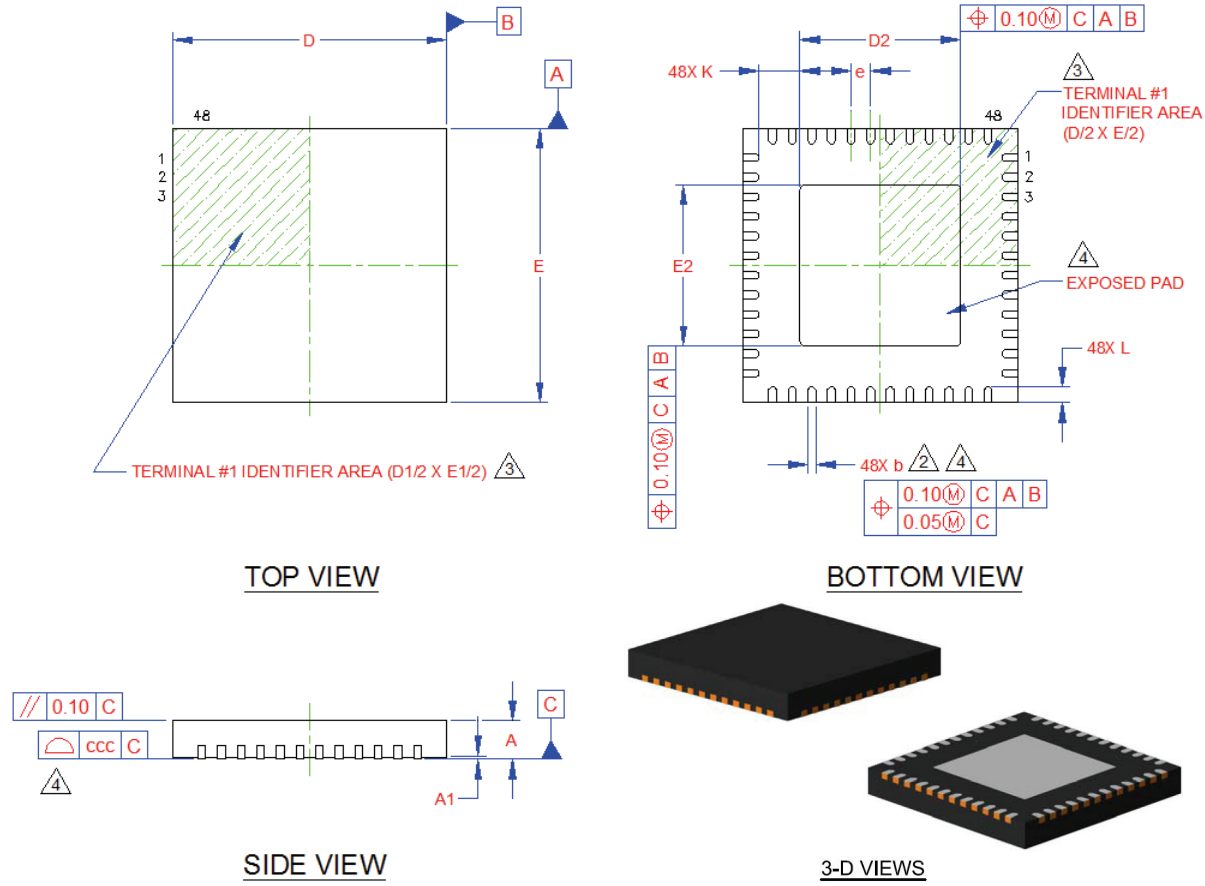


Figure 10.1 48-SQFN Package Drawing

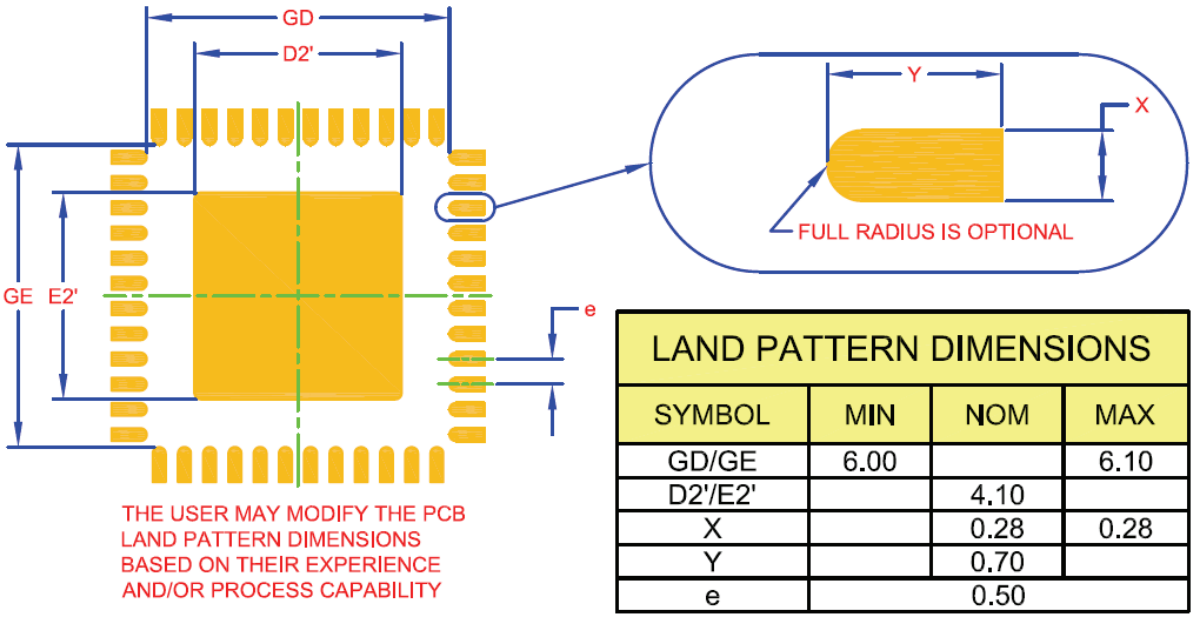
Table 10.1 48-SQFN Package Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.80	0.90	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
D/E	6.90	7.00	7.10	X/Y Body Size
D2/E2	4.00	4.10	4.20	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
k	0.95	1.05	-	Terminal to Exposed Pad Clearance
ccc	-	-	0.08	Coplanarity
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.

3. The pin 1 identifier may vary, but is always located within the zone indicated.
4. Coplanarity zone applies to exposed pad and terminals.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.00		6.10
D2'/E2'		4.10	
X		0.28	0.28
Y		0.70	
e		0.50	

Figure 10.2 48-SQFN Package Recommended Land Pattern

Chapter 11 Datasheet Revision History

Table 11.1 Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 (06-17-13)	Initial Release	

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Microchip:

USB4624-1080HN