



BUK7K32-100E

Dual N-channel 100 V, 27.5 mΩ standard level MOSFET

2 September 2015

Product data sheet

1. General description

Dual Standard level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ rating of greater than 1 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-----|------|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 100 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$ | - | - | 29 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}; \text{Fig. 1}$ | - | - | 64 | W |
| Static characteristics FET1 and FET2 | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$ | - | 21.5 | 27.5 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 5\text{ A}; V_{DS} = 80\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$ | - | 12.9 | - | nC |

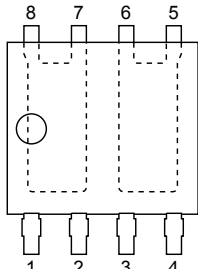
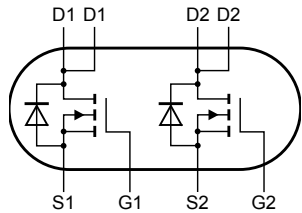


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5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|---|
| 1 | S1 | source1 |  <p>LFPAK56D (SOT1205)</p> |  <p>mbk725</p> |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|----------|--|---------|
| | Name | Description | Version |
| BUK7K32-100E | LFPAK56D | Plastic single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| BUK7K32-100E | 73210E |

8. Limiting values

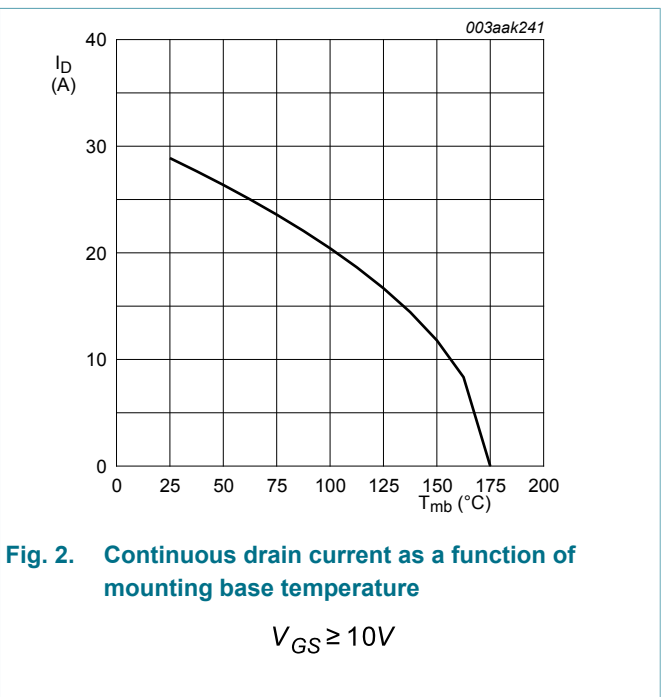
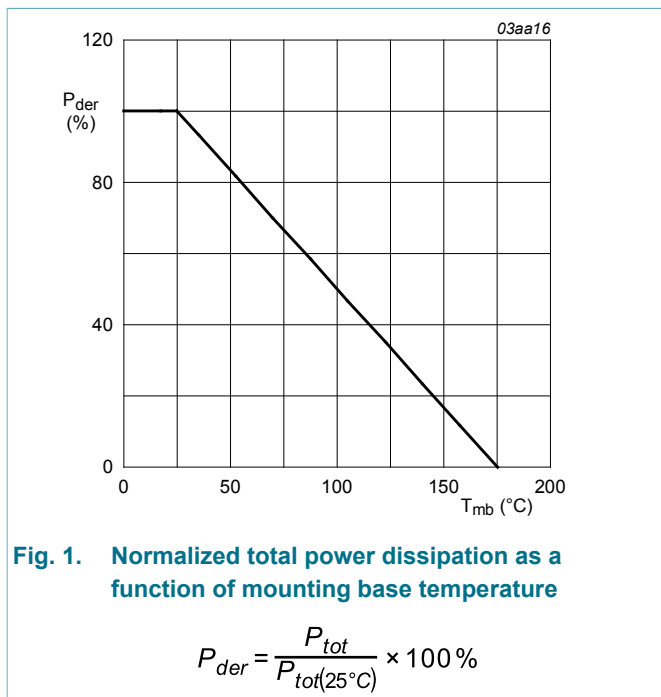
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-----|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | 100 | V |
| V_{DGR} | drain-gate voltage | $R_{GS} = 20\text{ k}\Omega$ | - | 100 | V |
| V_{GS} | gate-source voltage | $T_j \leq 175\text{ °C}$; DC | -20 | 20 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | 64 | W |
| I_D | drain current | $T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2 | - | 29 | A |
| | | $T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2 | - | 20.4 | A |
| I_{DM} | peak drain current | $T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3 | - | 116 | A |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|--|--|--------|-----|-------|
| T _{stg} | storage temperature | | -55 | 175 | °C |
| T _j | junction temperature | | -55 | 175 | °C |
| T _{slid(M)} | peak soldering temperature | | - | 260 | °C |
| Source-drain diode FET1 and FET2 | | | | | |
| I _S | source current | T _{mb} = 25 °C | - | 29 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C | - | 116 | A |
| Avalanche Ruggedness FET1 and FET2 | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | I _D = 29 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4 | [1][2] | - | 67 mJ |

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



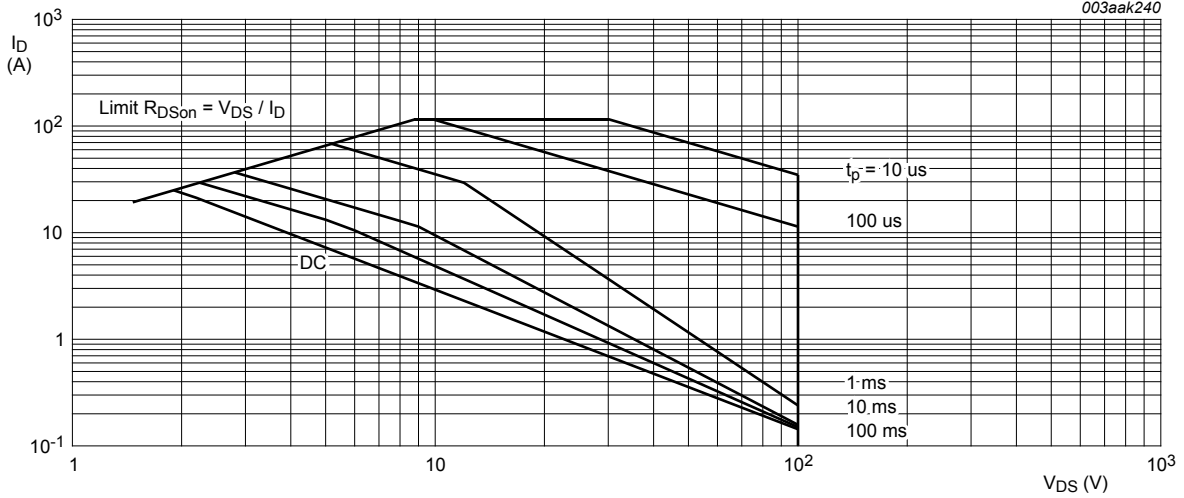


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

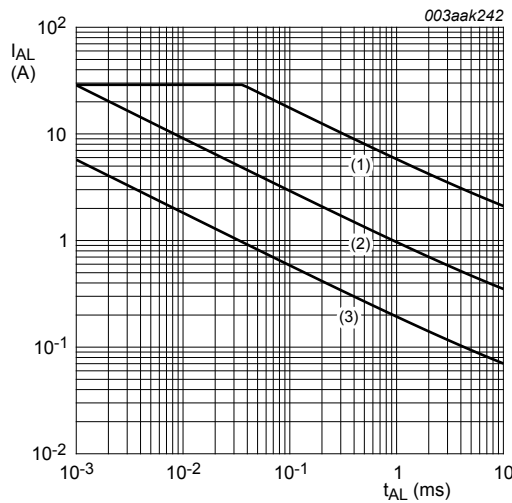


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25^\circ C$; (2) $T_{j(init)} = 150^\circ C$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | - | 2.36 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 95 | - | K/W |

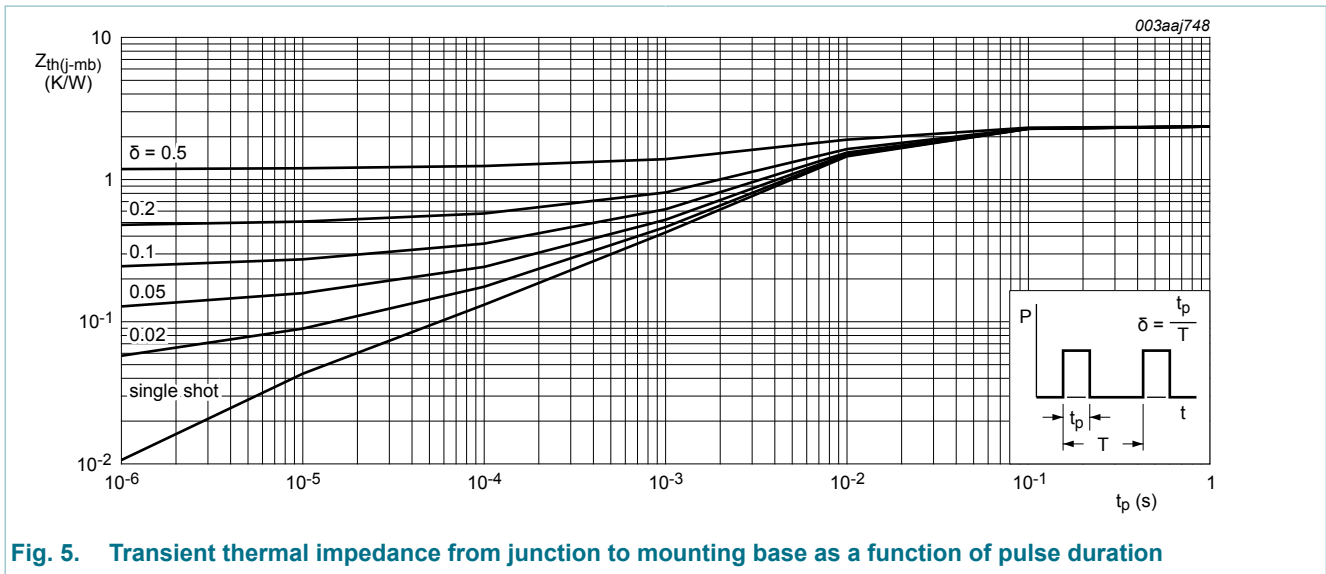


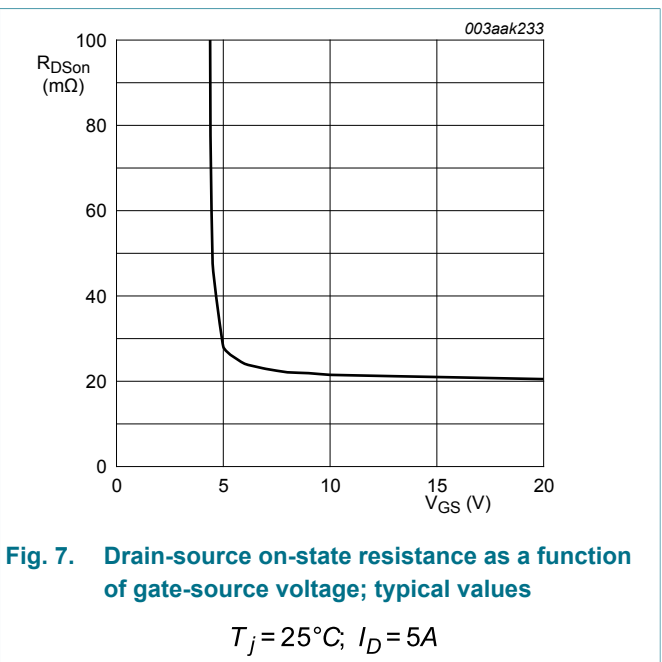
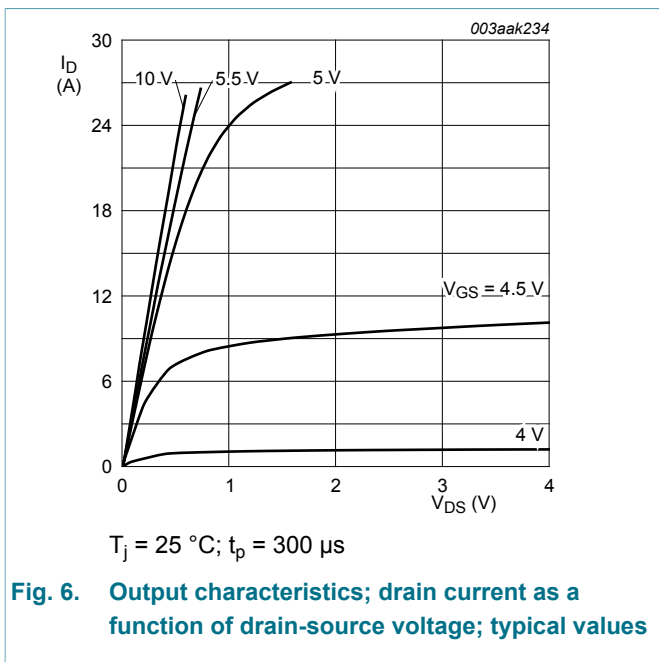
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|---|-----|------|------|---------|
| Static characteristics FET1 and FET2 | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 90 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 100 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10 | 2.4 | 3 | 4 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10 | 1 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10 | - | - | 4.5 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 1 | μA |
| | | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| | | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 11 | - | 21.5 | 27.5 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 11; Fig. 12 | - | 55 | 76 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 5 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14 | - | 34 | - | nC |
| Q_{GS} | gate-source charge | | - | 6.5 | - | nC |
| Q_{GD} | gate-drain charge | | - | 12.9 | - | nC |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|------------------------------|--|-----|------|------|------|
| C_{iss} | input capacitance | $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ | - | 1603 | 2137 | pF |
| C_{oss} | output capacitance | $T_j = 25\text{ °C};$ Fig. 15 | - | 164 | 196 | pF |
| C_{rss} | reverse transfer capacitance | | - | 109 | 150 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 80\text{ V}; R_L = 15\text{ }\Omega; V_{GS} = 10\text{ V};$ | - | 7.8 | - | ns |
| t_r | rise time | $R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ °C}$ | - | 10.9 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 24.2 | - | ns |
| t_f | fall time | | - | 13.8 | - | ns |
| Source-drain diode FET1 and FET2 | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ Fig. 16 | - | 0.78 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ | - | 35.9 | - | ns |
| Q_r | recovered charge | $V_{DS} = 50\text{ V}; T_j = 25\text{ °C}$ | - | 52.8 | - | nC |



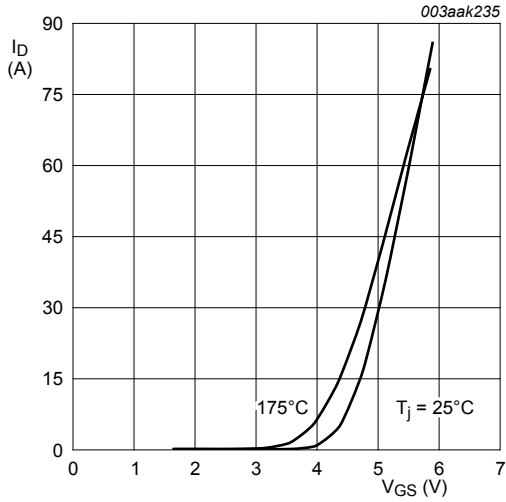


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

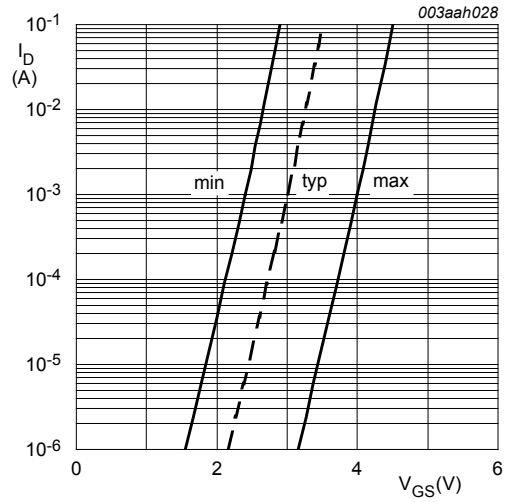


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5V$

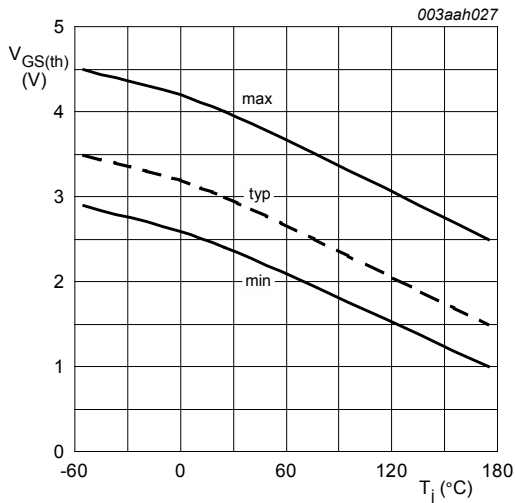


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

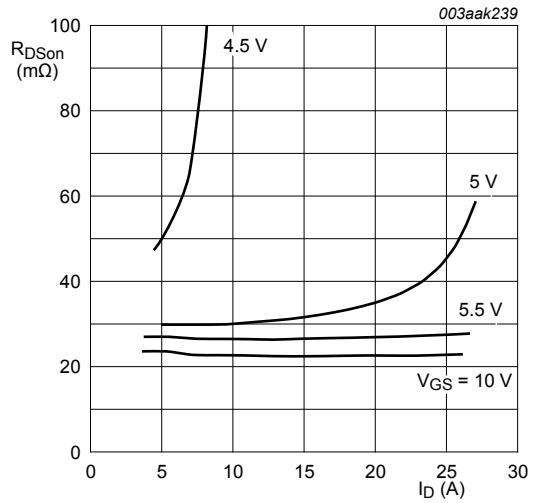


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C; t_p = 300 \mu s$

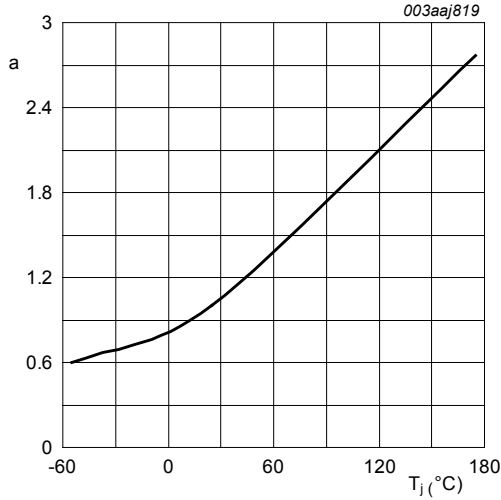


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

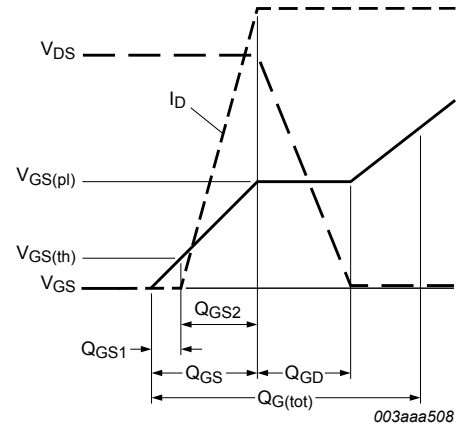


Fig. 13. Gate charge waveform definitions

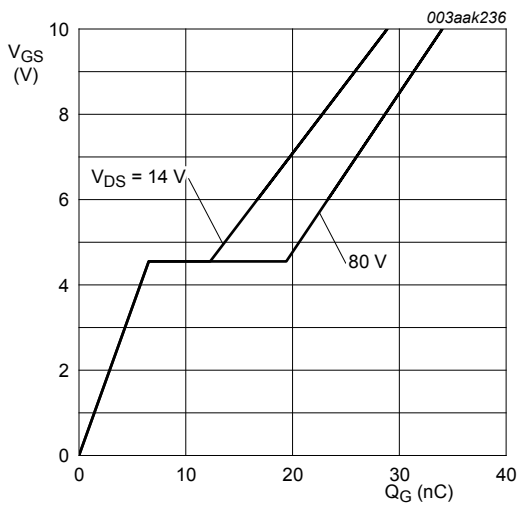


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}C; I_D = 5A$

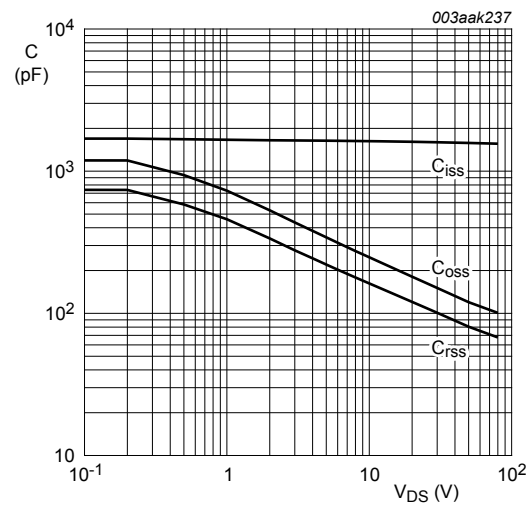


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

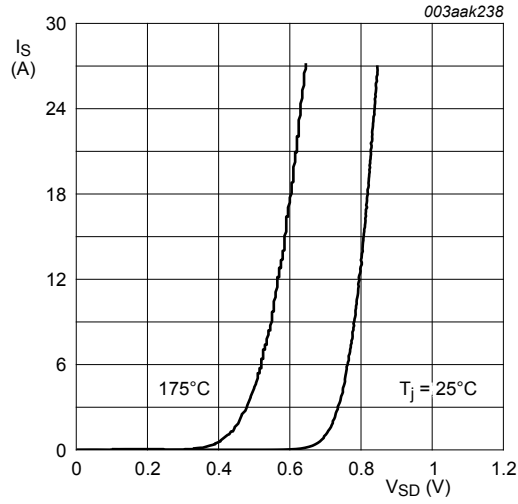


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

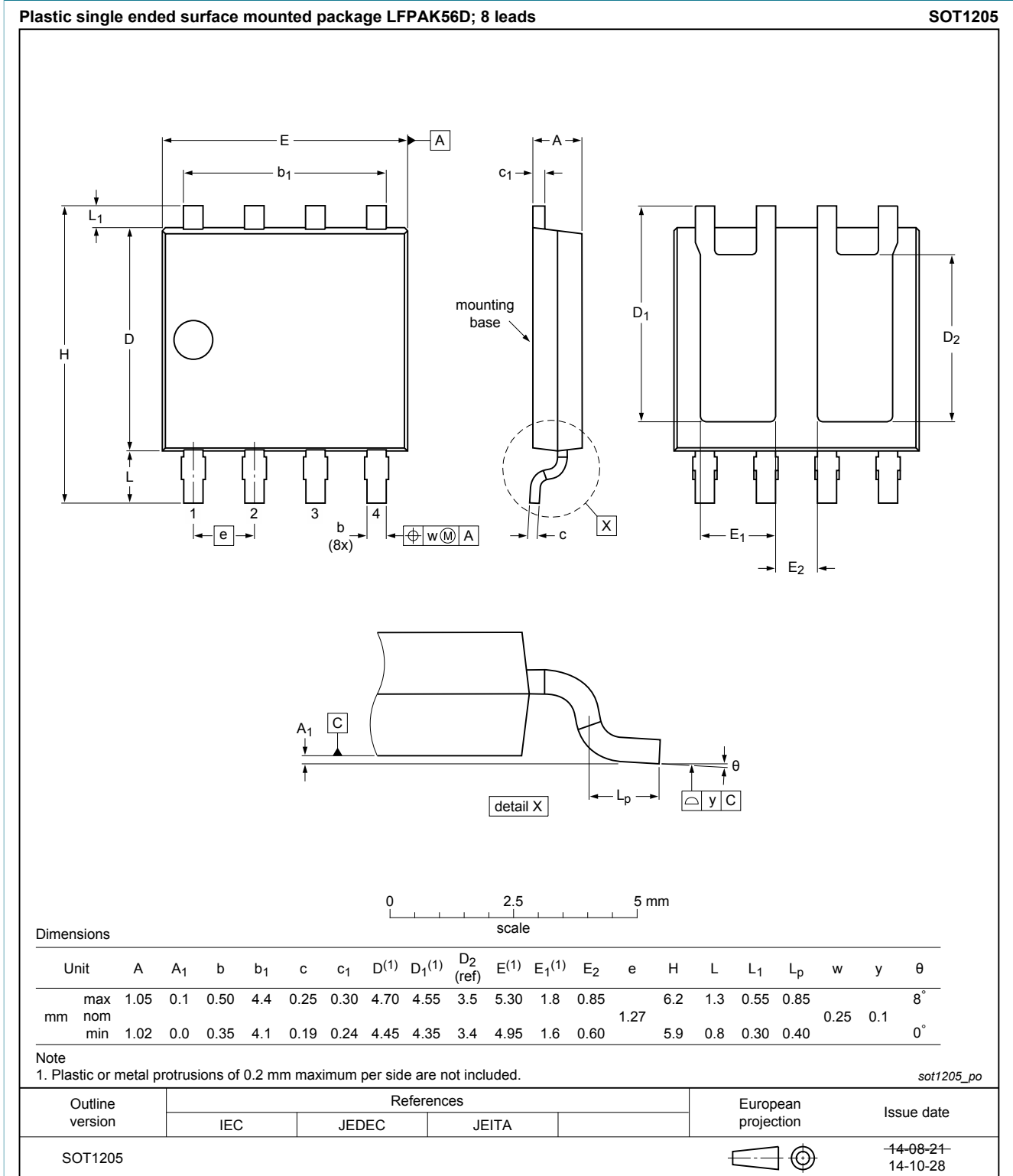


Fig. 17. Package outline LFPAK56D (SOT1205)

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|--------------------------------|--------------------|---|
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