



LPC122x

32-bit ARM Cortex-M0 microcontroller; up to 128 kB flash and 8 kB SRAM

Rev. 2 — 26 August 2011

Product data sheet

1. General description

The LPC122x extend NXP's 32-bit ARM microcontroller continuum and target a wide range of industrial applications in the areas of factory and home automation. Benefitting from the ARM Cortex-M0 Thumb instruction set, the LPC122x have up to 50 % higher code density compared to common 8/16-bit microcontroller performing typical tasks. The LPC122x also feature an optimized ROM-based divide library for Cortex-M0, which offers several times the arithmetic performance of software-based libraries, as well as highly deterministic cycle time combined with reduced flash code size. The ARM Cortex-M0 efficiency also helps the LPC122x achieve lower average power for similar applications.

The LPC122x operate at CPU frequencies of up to 45 MHz. They offer a wide range of flash memory options, from 32 kB to 128 kB. The small 512-byte page erase of the flash memory brings multiple design benefits, such as finer EEPROM emulation, boot-load support from any serial interface and ease of in-field programming with reduced on-chip RAM buffer requirements.

The peripheral complement of the LPC122x includes a 10-bit ADC, two comparators with output feedback loop, two UARTs, one SSP/SPI interface, one I²C-bus interface with Fast-mode Plus features, a Windowed Watchdog Timer, a DMA controller, a CRC engine, four general purpose timers, a 32-bit RTC, a 1 % internal oscillator for baud rate generation, and up to 55 General Purpose I/O (GPIO) pins.

2. Features and benefits

- Processor core
 - ◆ ARM Cortex-M0 processor, running at frequencies of up to 45 MHz (one wait state from flash) or 30 MHz (zero wait states from flash). The LPC122x have a high score of over 45 in CoreMark CPU performance benchmark testing, equivalent to 1.51/MHz.
 - ◆ ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
 - ◆ Serial Wire Debug (SWD).
 - ◆ System tick timer.
- Memory
 - ◆ Up to 8 kB SRAM.
 - ◆ Up to 128 kB on-chip flash programming memory.
 - ◆ In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
 - ◆ Includes ROM-based 32-bit integer division routines.
- Clock generation unit



- ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- ◆ 12 MHz Internal RC (IRC) oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- ◆ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
- ◆ Clock output function with divider that can reflect the system oscillator clock, IRC clock, main clock, and Watchdog clock.
- ◆ Real-Time Clock (RTC).
- Digital peripherals
 - ◆ Micro DMA controller with 21 channels.
 - ◆ CRC engine.
 - ◆ Two UARTs with fractional baud rate generation and internal FIFO. One UART with RS-485 and modem support and one standard UART with IrDA.
 - ◆ SSP/SPI controller with FIFO and multi-protocol capabilities.
 - ◆ I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode. I²C-bus pins have programmable glitch filter.
 - ◆ Up to 55 General Purpose I/O (GPIO) pins with programmable pull-up resistor, open-drain mode, programmable digital input glitch filter, and programmable input inverter.
 - ◆ Programmable output drive on all GPIO pins. Four pins support high-current output drivers.
 - ◆ All GPIO pins can be used as edge and level sensitive interrupt sources.
 - ◆ Four general purpose counter/timers with four capture inputs and four match outputs (32-bit timers) or two capture inputs and two match outputs (16-bit timers).
 - ◆ Windowed WatchDog Timer (WWDG); IEC-60335 Class B certified.
- Analog peripherals
 - ◆ One 8-channel, 10-bit ADC.
 - ◆ Two highly flexible analog comparators. Comparator outputs can be programmed to trigger a timer match signal or can be used to emulate 555 timer behavior.
- Power
 - ◆ Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
 - ◆ Processor wake-up from Deep-sleep mode via start logic using 12 port pins.
 - ◆ Processor wake-up from Deep-power down and Deep-sleep modes via the RTC.
 - ◆ Brownout detect with three separate thresholds each for interrupt and forced reset.
 - ◆ Power-On Reset (POR).
 - ◆ Integrated PMU (Power Management Unit).
- Unique device serial number for identification.
- 3.3 V power supply.
- Available as 64-pin and 48-pin LQFP package.

3. Applications

- eMetering
- Lighting
- Industrial networking
- Alarm systems
- White goods

4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|------------------|---------|--|----------|
| | Name | Description | Version |
| LPC1227FBD64/301 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1226FBD64/301 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1225FBD64/321 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1225FBD64/301 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1224FBD64/121 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1224FBD64/101 | LQFP64 | LQFP64: plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |
| LPC1227FBD48/301 | LQFP48 | LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1226FBD48/301 | LQFP48 | LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1225FBD48/321 | LQFP48 | LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1225FBD48/301 | LQFP48 | LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1224FBD48/121 | LQFP48 | LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |
| LPC1224FBD48/101 | LQFP48 | LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm | SOT313-2 |

4.1 Ordering options

Table 2. Ordering options for LPC122x

| Type number | Flash | Total SRAM | UART | I ² C/ FM+ | SSP/ SPI | ADC channels | GPIO | Package |
|------------------|--------|------------|------|--------------------------|-------------|--------------|------|---------|
| LPC1227 | | | | | | | | |
| LPC1227FBD64/301 | 128 kB | 8 kB | 2 | 1 | 1 | 8 | 55 | LQFP64 |
| LPC1227FBD48/301 | 128 kB | 8 kB | 2 | 1 | 1 | 8 | 39 | LQFP48 |
| LPC1226 | | | | | | | | |
| LPC1226FBD64/301 | 96 kB | 8 kB | 2 | 1 | 1 | 8 | 55 | LQFP64 |
| LPC1226FBD48/301 | 96 kB | 8 kB | 2 | 1 | 1 | 8 | 39 | LQFP48 |
| LPC1225 | | | | | | | | |
| LPC1225FBD64/321 | 80 kB | 8 kB | 2 | 1 | 1 | 8 | 55 | LQFP64 |
| LPC1225FBD64/301 | 64 kB | 8 kB | 2 | 1 | 1 | 8 | 55 | LQFP64 |
| LPC1225FBD48/321 | 80 kB | 8 kB | 2 | 1 | 1 | 8 | 39 | LQFP48 |
| LPC1225FBD48/301 | 64 kB | 8 kB | 2 | 1 | 1 | 8 | 39 | LQFP48 |
| LPC1224 | | | | | | | | |
| LPC1224FBD64/121 | 48 kB | 4 kB | 2 | 1 | 1 | 8 | 55 | LQFP64 |
| LPC1224FBD64/101 | 32 kB | 4 kB | 2 | 1 | 1 | 8 | 55 | LQFP64 |
| LPC1224FBD48/121 | 48 kB | 4 kB | 2 | 1 | 1 | 8 | 39 | LQFP48 |
| LPC1224FBD48/101 | 32 kB | 4 kB | 2 | 1 | 1 | 8 | 39 | LQFP48 |

5. Block diagram

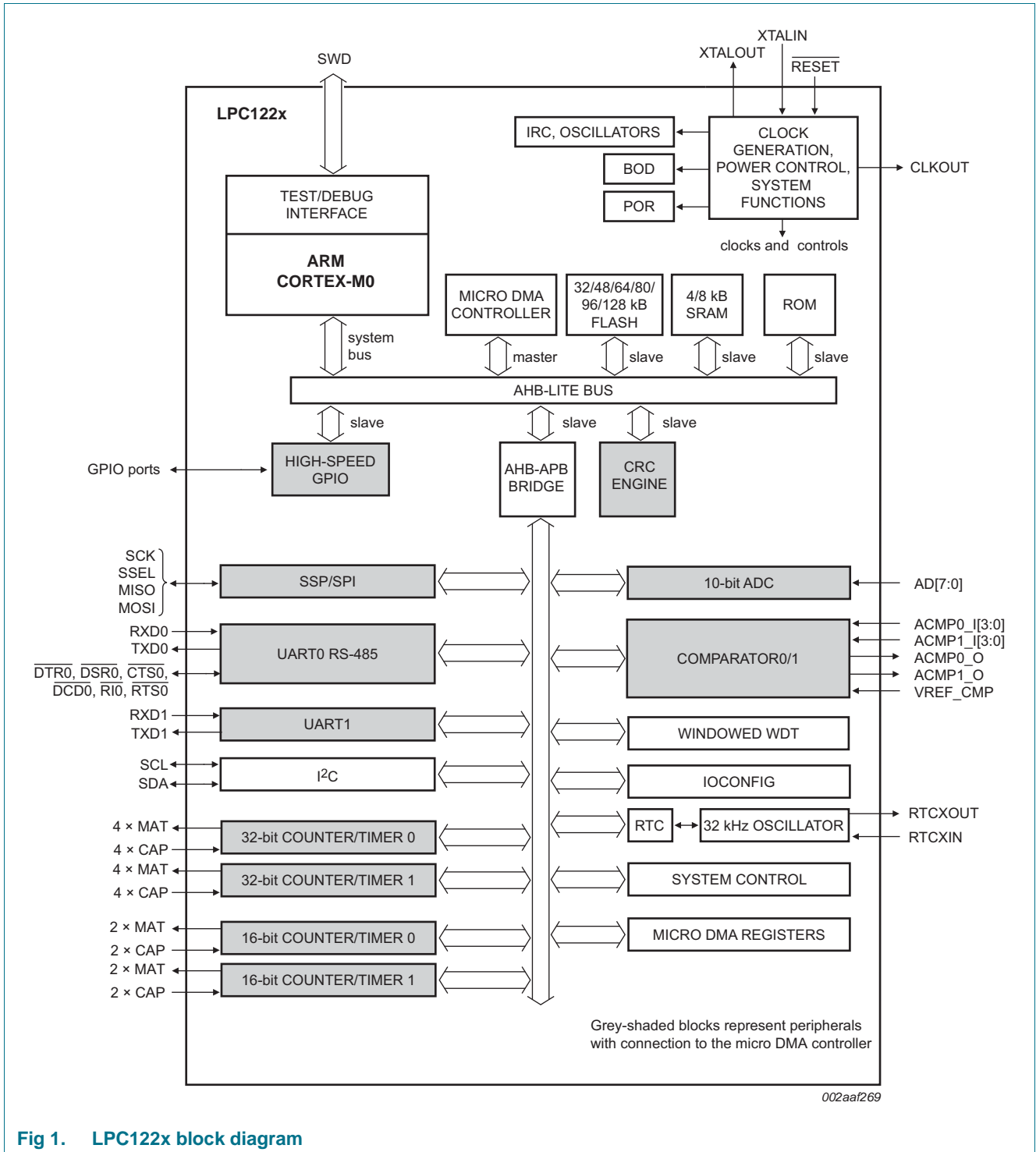
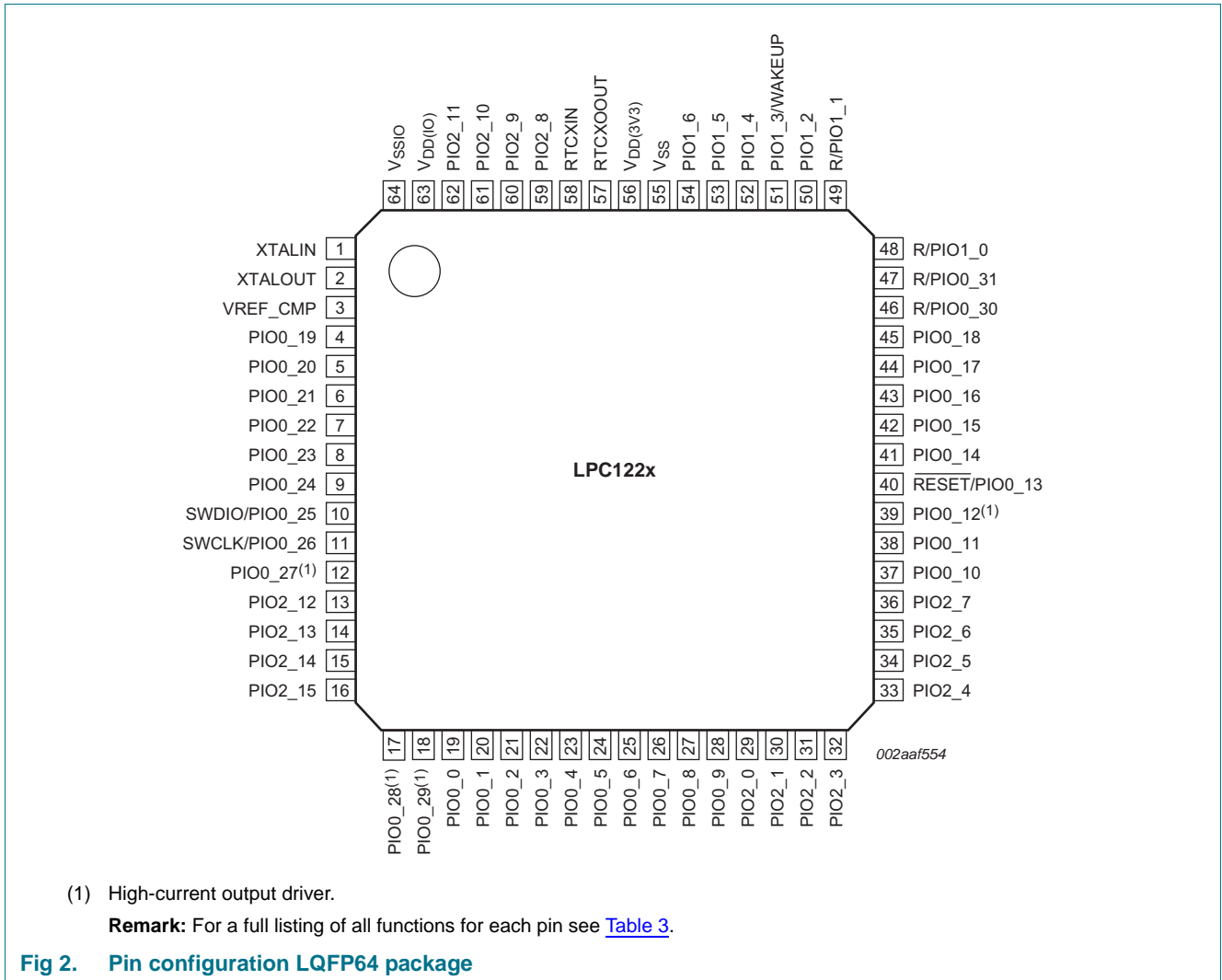
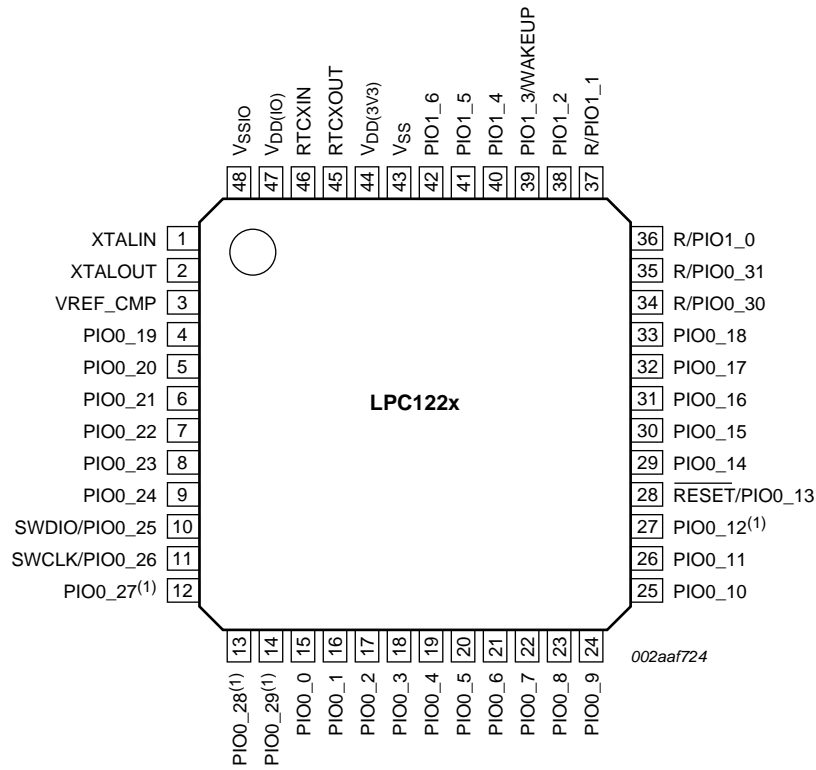


Fig 1. LPC122x block diagram

6. Pinning information

6.1 Pinning





(1) High-current output driver.

Remark: For a full listing of all functions for each pin see [Table 3](#).

Fig 3. Pin configuration LQFP48 package

6.2 Pin description

All pins except the supply pins can have more than one function as shown in [Table 3](#). The pin function is selected through the pin's IOCON register in the IOCONFIG block. The multiplexed functions (see [Table 4](#)) include the counter/timer inputs and outputs, the UART receive, transmit, and control functions, and the serial wire debug functions.

For each pin, the default function is listed first together with the pin's reset state.

Table 3. LPC122x pin description

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state [1] | Description |
|--|------------|---|-------------------|------|---------------------------------|---|
| PIO0_0 to PIO0_31 | | | | I/O | | Port 0 — Port 0 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block. |
| PIO0_0/ <u>RTS0</u> | 15 | 19 [2] [3] | yes | I/O | I; PU | PIO0_0 — General purpose digital input/output pin. RTS0 — Request To Send output for UART0. |
| PIO0_1/ <u>RXD0</u> / CT32B0_CAP0/ CT32B0_MAT0 | 16 | 20 [2] [3] | yes | I/O | I; PU | PIO0_1 — General purpose digital input/output pin. RXD0 — Receiver input for UART0. CT32B0_CAP0 — Capture input, channel 0 for 32-bit timer 0. CT32B0_MAT0 — Match output, channel 0 for 32-bit timer 0. |
| PIO0_2/ <u>TXD0</u> / CT32B0_CAP1/ CT32B0_MAT1 | 17 | 21 [2] [3] | yes | I/O | I; PU | PIO0_2 — General purpose digital input/output pin. TXD0 — Transmitter output for UART0. CT32B0_CAP1 — Capture input, channel 1 for 32-bit timer 0. CT32B0_MAT1 — Match output, channel 1 for 32-bit timer 0. |
| PIO0_3/ <u>DTR0</u> / CT32B0_CAP2/ CT32B0_MAT2 | 18 | 22 [2] [3] | yes | I/O | I; PU | PIO0_3 — General purpose digital input/output pin. DTR0 — Data Terminal Ready output for UART0. CT32B0_CAP2 — Capture input, channel 2 for 32-bit timer 0. CT32B0_MAT2 — Match output, channel 2 for 32-bit timer 0. |
| PIO0_4/ <u>DSR0</u> / CT32B0_CAP3/ CT32B0_MAT3 | 19 | 23 [2] [3] | yes | I/O | I; PU | PIO0_4 — General purpose digital input/output pin. DSR0 — Data Set Ready input for UART0. CT32B0_CAP3 — Capture input, channel 3 for 32-bit timer 0. CT32B0_MAT3 — Match output, channel 3 for 32-bit timer 0. |
| PIO0_5/ <u>DCD0</u> | 20 | 24 [2] [3] | yes | I/O | I; PU | PIO0_5 — General purpose digital input/output pin. DCD0 — Data Carrier Detect input for UART0. |
| PIO0_6/ <u>RI0</u> / CT32B1_CAP0/ CT32B1_MAT0 | 21 | 25 [2] [3] | yes | I/O | I; PU | PIO0_6 — General purpose digital input/output pin. RI0 — Ring Indicator input for UART0. CT32B1_CAP0 — Capture input, channel 0 for 32-bit timer 1. CT32B1_MAT0 — Match output, channel 0 for 32-bit timer 1. |

Table 3. LPC122x pin description ...continued

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state [1] | Description |
|--|------------|------------|--|------|---------------------------------|---|
| PIO0_7/CTS0/ CT32B1_CAP1/ CT32B1_MAT1 | 22 | 26 | [2] [3] | yes | I/O | I; PU PIO0_7 — General purpose digital input/output pin. |
| | | | | I | - | CTS0 — Clear To Send input for UART0. |
| | | | | I | - | CT32B1_CAP1 — Capture input, channel 1 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT1 — Match output, channel 1 for 32-bit timer 1. |
| PIO0_8/RXD1/ CT32B1_CAP2/ CT32B1_MAT2 | 23 | 27 | [2] [3] | yes | I/O | I; PU PIO0_8 — General purpose digital input/output pin. |
| | | | | I | - | RXD1 — Receiver input for UART1. |
| | | | | I | - | CT32B1_CAP2 — Capture input, channel 2 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT2 — Match output, channel 2 for 32-bit timer 1. |
| PIO0_9/TXD1/ CT32B1_CAP3/ CT32B1_MAT3 | 24 | 28 | [2] [3] | yes | I/O | I; PU PIO0_9 — General purpose digital input/output pin. |
| | | | | O | - | TXD1 — Transmitter output for UART1. |
| | | | | I | - | CT32B1_CAP3 — Capture input, channel 3 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT3 — Match output, channel 3 for 32-bit timer 1. |
| PIO0_10/SCL | 25 | 37 | [4] | yes | I/O | I; IA PIO0_10 — General purpose digital input/output pin. |
| | | | | I/O | - | SCL — I ² C-bus clock input/output. |
| PIO0_11/SDA/ CT16B0_CAP0/ CT16B0_MAT0 | 26 | 38 | [4] | yes | I/O | I; IA PIO0_11 — General purpose digital input/output pin. |
| | | | | I/O | - | SDA — I ² C-bus data input/output. |
| | | | | I | - | CT16B0_CAP0 — Capture input, channel 0 for 16-bit timer 0. |
| | | | | O | - | CT16B0_MAT0 — Match output, channel 0 for 16-bit timer 0. |
| PIO0_12/CLKOUT/ CT16B0_CAP1/ CT16B0_MAT1 | 27 | 39 | [9] | no | I/O | I; PU PIO0_12 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. High-current output driver. |
| | | | | O | - | CLKOUT — Clock out pin. |
| | | | | I | - | CT16B0_CAP1 — Capture input, channel 1 for 16-bit timer 0. |
| | | | | O | - | CT16B0_MAT1 — Match output, channel 1 for 16-bit timer 0. |
| RESET/PIO0_13 | 28 | 40 | [5] [3] | no | I | I; PU RESET — External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. |
| | | | | I/O | - | PIO0_13 — General purpose digital input/output pin. |
| PIO0_14/SCK | 29 | 41 | [2] [3] | no | I/O | I; PU PIO0_14 — General purpose digital input/output pin. |
| | | | | I/O | - | SCK — Serial clock for SSP/SPI. |
| PIO0_15/SSEL/ CT16B1_CAP0/ CT16B1_MAT0 | 30 | 42 | [2] [3] | no | I/O | I; PU PIO0_15 — General purpose digital input/output pin. |
| | | | | I/O | - | SSEL — Slave select for SSP/SPI. |
| | | | | I | - | CT16B1_CAP0 — Capture input, channel 0 for 16-bit timer 1. |
| | | | | O | - | CT16B1_MAT0 — Match output, channel 0 for 16-bit timer 1. |
| PIO0_16/MISO/ CT16B1_CAP1/ CT16B1_MAT1 | 31 | 43 | [2] [3] | no | I/O | I; PU PIO0_16 — General purpose digital input/output pin. |
| | | | | I/O | - | MISO — Master In Slave Out for SSP/SPI. |
| | | | | I | - | CT16B1_CAP1 — Capture input, channel 1 for 16-bit timer 1. |
| | | | | O | - | CT16B1_MAT1 — Match output, channel 1 for 16-bit timer 1. |

Table 3. LPC122x pin description ...continued

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state | Description |
|--|------------|------------|-------------------|------|-------------|---|
| PIO0_17/MOSI | 32 | 44 | no | I/O | I; PU | PIO0_17 — General purpose digital input/output pin. |
| | | | | I/O | - | MOSI — Master Out Slave In for SSP/SPI. |
| PIO0_18/SWCLK/ CT32B0_CAP0/ CT32B0_MAT0 | 33 | 45 | no | I/O | I; PU | PIO0_18 — General purpose digital input/output pin. |
| | | | | I | - | SWCLK — Serial wire clock, alternate location. |
| | | | | I | - | CT32B0_CAP0 — Capture input, channel 0 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT0 — Match output, channel 0 for 32-bit timer 0. |
| PIO0_19/ACMP0_I0/ CT32B0_CAP1/ CT32B0_MAT1 | 4 | 4 | no | I/O | I; PU | PIO0_19 — General purpose digital input/output pin. |
| | | | | I | - | ACMP0_I0 — Input 0 for comparator 0. |
| | | | | I | - | CT32B0_CAP1 — Capture input, channel 1 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT1 — Match output, channel 1 for 32-bit timer 0. |
| PIO0_20/ACMP0_I1/ CT32B0_CAP2/ CT32B0_MAT2 | 5 | 5 | no | I/O | I; PU | PIO0_20 — General purpose digital input/output pin. |
| | | | | I | - | ACMP0_I1 — Input 1 for comparator 0. |
| | | | | I | - | CT32B0_CAP2 — Capture input, channel 2 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT2 — Match output, channel 2 for 32-bit timer 0. |
| PIO0_21/ACMP0_I2/ CT32B0_CAP3/ CT32B0_MAT3 | 6 | 6 | no | I/O | I; PU | PIO0_21 — General purpose digital input/output pin. |
| | | | | I | - | ACMP0_I2 — Input 2 for comparator 0. |
| | | | | I | - | CT32B0_CAP3 — Capture input, channel 3 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT3 — Match output, channel 3 for 32-bit timer 0. |
| PIO0_22/ACMP0_I3 | 7 | 7 | no | I/O | I; PU | PIO0_22 — General purpose digital input/output pin. |
| | | | | I | - | ACMP0_I3 — Input 3 for comparator 0. |
| PIO0_23/ ACMP1_I0/ CT32B1_CAP0/ CT32B1_MAT0 | 8 | 8 | no | I/O | I; PU | PIO0_23 — General purpose digital input/output pin. |
| | | | | I | - | ACMP1_I0 — Input 0 for comparator 1. |
| | | | | I | - | CT32B1_CAP0 — Capture input, channel 0 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT0 — Match output, channel 0 for 32-bit timer 1. |
| PIO0_24/ACMP1_I1/ CT32B1_CAP1/ CT32B1_MAT1 | 9 | 9 | no | I/O | I; PU | PIO0_24 — General purpose digital input/output pin. |
| | | | | I | - | ACMP1_I1 — Input 1 for comparator 1. |
| | | | | I | - | CT32B1_CAP1 — Capture input, channel 1 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT1 — Match output, channel 1 for 32-bit timer 1. |
| SWDIO/ACMP1_I2/ CT32B1_CAP2/ CT32B1_MAT2/ PIO0_25 | 10 | 10 | no | I/O | I; PU | SWDIO — Serial wire debug input/output, default location. |
| | | | | I | - | ACMP1_I2 — Input 2 for comparator 1. |
| | | | | I | - | CT32B1_CAP2 — Capture input, channel 2 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT2 — Match output, channel 2 for 32-bit timer 1. |
| | | | | I/O | - | PIO0_25 — General purpose digital input/output pin. |
| SWCLK/ACMP1_I3/ CT32B1_CAP3/ CT32B1_MAT3/ PIO0_26 | 11 | 11 | no | I | I; PU | SWCLK — Serial wire clock, default location. |
| | | | | I | - | ACMP1_I3 — Input 3 for comparator 1. |
| | | | | I | - | CT32B1_CAP3 — Capture input, channel 3 or 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT3 — Match output, channel 3 for 32-bit timer 1. |
| | | | | I/O | - | PIO0_26 — General purpose digital input/output pin. |

Table 3. LPC122x pin description ...continued

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state | Description |
|---|------------|------------|-------------------|------|-------------|---|
| PIO0_27/ACMP0_O | 12 | 12 | no | I/O | I; PU | PIO0_27 — General purpose digital input/output pin (high-current output driver). |
| | | | | O | - | ACMP0_O — Output for comparator 0. |
| PIO0_28/ACMP1_O/ CT16B0_CAP0/ CT16B0_MAT0 | 13 | 17 | no | I/O | I; PU | PIO0_28 — General purpose digital input/output pin (high-current output driver). |
| | | | | O | - | ACMP1_O — Output for comparator 1. |
| | | | | I | - | CT16B0_CAP0 — Capture input, channel 0 for 16-bit timer 0. |
| PIO0_29/ROSC/ CT16B0_CAP1/ CT16B0_MAT1 | 14 | 18 | no | I/O | I; PU | PIO0_29 — General purpose digital input/output pin (high-current output driver). |
| | | | | I/O | - | ROSC — Relaxation oscillator for 555 timer applications. |
| | | | | I | - | CT16B0_CAP1 — Capture input, channel 1 for 16-bit timer 0. |
| R/PIO0_30/AD0 | 34 | 46 | no | I | I; PU | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | - | PIO0_30 — General purpose digital input/output pin. |
| | | | | I | - | AD0 — A/D converter, input 0. |
| R/PIO0_31/AD1 | 35 | 47 | no | I | I; PU | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | - | PIO0_31 — General purpose digital input/output pin. |
| | | | | I | - | AD1 — A/D converter, input 1. |
| PIO1_0 to PIO1_6 | | | | I/O | | Port 1 — Port 1 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block. Pins PIO1_7 through PIO1_31 are not available. |
| R/PIO1_0/AD2 | 36 | 48 | no | O | I; PU | R — Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | | I/O | - | PIO1_0 — General purpose digital input/output pin. |
| | | | | I | - | AD2 — A/D converter, input 2. |
| R/PIO1_1/AD3 | 37 | 49 | no | I | I; PU | R — Reserved. Configure for an alternate function in the IOCONFIG block. Do not pull this pin LOW at reset. |
| | | | | I/O | - | PIO1_1 — General purpose digital input/output pin. |
| | | | | I | - | AD3 — A/D converter, input 3. |
| PIO1_2/SWDIO/AD4 | 38 | 50 | no | I/O | I; PU | PIO1_2 — General purpose digital input/output pin. |
| | | | | I/O | - | SWDIO — Serial wire debug input/output, alternate location. |
| | | | | I | - | AD4 — A/D converter, input 4. |
| PIO1_3/AD5/WAKEUP | 39 | 51 | no | I/O | I; PU | PIO1_3 — General purpose digital input/output pin. |
| | | | | I | - | AD5 — A/D converter, input 5. |
| | | | | I | - | WAKEUP — Deep power-down mode wake-up pin. |
| PIO1_4/AD6 | 40 | 52 | no | I/O | I; PU | PIO1_4 — General purpose digital input/output pin. |
| | | | | I | - | AD6 — A/D converter, input 6. |

Table 3. LPC122x pin description ...continued

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state [1] | Description |
|---|------------|------------|--|------|--|---|
| PIO1_5/AD7/ CT16B1_CAP0/ CT16B1_MAT0 | 41 | 53 | [2] [3] | no | I/O | I; PU PIO1_5 — General purpose digital input/output pin. |
| | | | | I | - | AD7 — A/D converter, input 7. |
| | | | | I | - | CT16B1_CAP0 — Capture input, channel 0 for 16-bit timer 1. |
| | | | | O | - | CT16B1_MAT0 — Match output, channel 0 for 16-bit timer 1. |
| PIO1_6/ CT16B1_CAP1/ CT16B1_MAT1 | 42 | 54 | [2] [3] | no | I/O | I; PU PIO1_6 — General purpose digital input/output pin. |
| | | | | I | - | CT16B1_CAP1 — Capture input, channel 1 for 16-bit timer 1. |
| | | | | O | - | CT16B1_MAT1 — Match output, channel 1 for 16-bit timer 1. |
| PIO2_0 to PIO2_15 | | | | I/O | Port 2 — Port 2 is a 32-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_16 through PIO2_31 are not available. | |
| PIO2_0/ CT16B0_CAP0/ CT16B0_MAT0/ RTS0 | - | 29 | [2] [3] | no | I/O | I; PU PIO2_0 — General purpose digital input/output pin. |
| | | | | I | - | CT16B0_CAP0 — Capture input, channel 0 for 16-bit timer 0. |
| | | | | O | - | CT16B0_MAT0 — Match output, channel 0 for 16-bit timer 0. |
| | | | | O | - | RTS0 — Request To Send output for UART0. |
| PIO2_1/ CT16B0_CAP1/ CT16B0_MAT1/RXD0 | - | 30 | [2] [3] | no | I/O | I; PU PIO2_1 — General purpose digital input/output pin. |
| | | | | I | - | CT16B0_CAP1 — Capture input, channel 1 for 16-bit timer 0. |
| | | | | O | - | CT16B0_MAT1 — Match output, channel 1 for 16-bit timer 0. |
| | | | | I | - | RXD0 — Receiver input for UART0. |
| PIO2_2/ CT16B1_CAP0/ CT16B1_MAT0/TXD0 | - | 31 | [2] [3] | no | I/O | I; PU PIO2_2 — General purpose digital input/output pin. |
| | | | | I | - | CT16B1_CAP0 — Capture input, channel 0 for 16-bit timer 1. |
| | | | | O | - | CT16B1_MAT0 — Match output, channel 0 for 16-bit timer 1. |
| | | | | O | - | TXD0 — Transmitter output for UART0. |
| PIO2_3/ CT16B1_CAP1/ CT16B1_MAT1/DTR0 | - | 32 | [2] [3] | no | I/O | I; PU PIO2_3 — General purpose digital input/output pin. |
| | | | | I | - | CT16B1_CAP1 — Capture input, channel 1 for 16-bit timer 1. |
| | | | | O | - | CT16B1_MAT1 — Match output, channel 1 for 16-bit timer 1. |
| | | | | O | - | DTR0 — Data Terminal Ready output for UART0. |
| PIO2_4/ CT32B0_CAP0/ CT32B0_MAT0/CTS0 | - | 33 | [2] [3] | no | I/O | I; PU PIO2_4 — General purpose digital input/output pin. |
| | | | | I | - | CT32B0_CAP0 — Capture input, channel 0 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT0 — Match output, channel 0 for 32-bit timer 0. |
| | | | | I | - | CTS0 — Clear To Send input for UART0. |
| PIO2_5/ CT32B0_CAP1/ CT32B0_MAT1/RI0 | - | 34 | [2] [3] | no | I/O | I; PU PIO2_5 — General purpose digital input/output pin. |
| | | | | I | - | CT32B0_CAP1 — Capture input, channel 1 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT1 — Match output, channel 1 for 32-bit timer 0. |
| | | | | I | - | RI0 — Ring Indicator input for UART0. |

Table 3. LPC122x pin description ...continued

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state [1] | Description |
|--|------------|---|-------------------|------|---------------------------------|---|
| PIO2_6/ CT32B0_CAP2/ CT32B0_MAT2/DCD0 | - | 35 [2] [3] | no | I/O | I; PU | PIO2_6 — General purpose digital input/output pin. |
| | | | | I | - | CT32B0_CAP2 — Capture input, channel 2 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT2 — Match output, channel 2 for 32-bit timer 0. |
| | | | | I | - | DCD0 — Data Carrier Detect input for UART0. |
| PIO2_7/ CT32B0_CAP3/ CT32B0_MAT3/DSR0 | - | 36 [2] [3] | no | I/O | I; PU | PIO2_7 — General purpose digital input/output pin. |
| | | | | I | - | CT32B0_CAP3 — Capture input, channel 3 for 32-bit timer 0. |
| | | | | O | - | CT32B0_MAT3 — Match output, channel 3 for 32-bit timer 0. |
| | | | | I | - | DSR0 — Data Set Ready input for UART0. |
| PIO2_8/ CT32B1_CAP0/ CT32B1_MAT0 | - | 59 [2] [3] | no | I/O | I; PU | PIO2_8 — General purpose digital input/output pin. |
| | | | | I | - | CT32B1_CAP0 — Capture input, channel 0 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT0 — Match output, channel 0 for 32-bit timer 1. |
| PIO2_9/ CT32B1_CAP1/ CT32B1_MAT1 | - | 60 [2] [3] | no | I/O | I; PU | PIO2_9 — General purpose digital input/output pin. |
| | | | | I | - | CT32B1_CAP1 — Capture input, channel 1 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT1 — Match output, channel 1 for 32-bit timer 1. |
| PIO2_10/ CT32B1_CAP2/ CT32B1_MAT2/TXD1 | - | 61 [2] [3] | no | I/O | I; PU | PIO2_10 — General purpose digital input/output pin. |
| | | | | I | - | CT32B1_CAP2 — Capture input, channel 2 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT2 — Match output, channel 2 for 32-bit timer 1. |
| | | | | O | - | TXD1 — Transmitter output for UART1. |
| PIO2_11/ CT32B1_CAP3/ CT32B1_MAT3/RXD1 | - | 62 [2] [3] | no | I/O | I; PU | PIO2_11 — General purpose digital input/output pin. |
| | | | | I | - | CT32B1_CAP3 — Capture input, channel 3 for 32-bit timer 1. |
| | | | | O | - | CT32B1_MAT3 — Match output, channel 3 for 32-bit timer 1. |
| | | | | I | - | RXD1 — Receiver input for UART1. |
| PIO2_12/RXD1 | - | 13 [2] [3] | no | I/O | I; PU | PIO2_12 — General purpose digital input/output pin. |
| | | | | I | - | RXD1 — Receiver input for UART1. |
| PIO2_13/TXD1 | - | 14 [2] [3] | no | I/O | I; PU | PIO2_13 — General purpose digital input/output pin. |
| | | | | O | - | TXD1 — Transmitter output for UART1. |
| PIO2_14 | - | 15 [2] [3] | no | I/O | I; PU | PIO2_14 — General purpose digital input/output pin. |
| PIO2_15 | - | 16 [2] [3] | no | I/O | I; PU | PIO2_15 — General purpose digital input/output pin. |
| RTCXIN | 46 | 58 [10] | - | I | - | Input to the 32 kHz oscillator circuit. |
| RTCXOUT | 45 | 57 [10] | - | O | - | Output from the 32 kHz oscillator amplifier. |
| XTALIN | 1 | 1 | - | I | - | Input to the system oscillator circuit and internal clock generator circuits. |
| XTALOUT | 2 | 2 | - | O | - | Output from the system oscillator amplifier. |
| VREF_CMP | 3 | 3 | - | I | - | Reference voltage for comparator. |

Table 3. LPC122x pin description ...continued

| Symbol | Pin LQFP48 | Pin LQFP64 | Start logic input | Type | Reset state [1] | Description |
|----------------------|------------|------------|-------------------|------|---------------------------------|---|
| V _{DD(I/O)} | 47 | 63 | - | I | - | Input/output supply voltage. |
| V _{DD(3V3)} | 44 | 56 | - | I | - | 3.3 V supply voltage to the internal regulator and the ADC. Also used as the ADC reference voltage. |
| V _{SSIO} | 48 | 64 | - | I | - | Ground. |
| V _{SS} | 43 | 55 | - | I | - | Ground. |

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled.
- [2] 3.3 V tolerant, digital I/O pin; default: pull-up enabled, no hysteresis.
- [3] If set to output, this normal-drive pin is in low mode by default.
- [4] I²C-bus pins; 5 V tolerant; open-drain; default: no pull-up/pull-down; no hysteresis.
- [5] 3.3 V tolerant, digital I/O pin with $\overline{\text{RESET}}$ function; default: pull-up enabled, no hysteresis. An external pull-up resistor is required on this pin for the Deep power-down mode.
- [6] 3.3 V tolerant, digital I/O pin with analog function; default: pull-up enabled, no hysteresis.
- [7] If set to output, this normal-drive pin is in high mode by default.
- [8] 3.3 V tolerant, digital I/O pin with analog function and WAKEUP function; default: pull-up enabled, no hysteresis.
- [9] 3.3 V tolerant, high-drive digital I/O pin; default: pull-up enabled, no hysteresis.
- [10] If the RTC is not used, RTCXIN and RTCXOUT can be left floating.

To enable a peripheral function, find the corresponding port pin, or select a port pin if the function is multiplexed, and program the port pin's IOCONFIG register to enable that function. The primary SWD functions and $\overline{\text{RESET}}$ are the default functions on their pins after reset.

Table 4. Pin multiplexing

| Peripheral | Function | Type | Available on ports: | | |
|--------------------|----------|------|---------------------|---|---|
| Analog comparators | ROSC | I/O | PIO0_29 | - | - |
| | ACMP0_I0 | I | PIO0_19 | - | - |
| | ACMP0_I1 | I | PIO0_20 | - | - |
| | ACMP0_I2 | I | PIO0_21 | - | - |
| | ACMP0_I3 | I | PIO0_22 | - | - |
| | ACMP0_O | O | PIO0_27 | - | - |
| | ACMP1_I0 | I | PIO0_23 | - | - |
| | ACMP1_I1 | I | PIO0_24 | - | - |
| | ACMP1_I2 | I | PIO0_25 | - | - |
| | ACMP1_I3 | I | PIO0_26 | - | - |
| | ACMP1_O | O | PIO0_28 | - | - |

Table 4. Pin multiplexing

| Peripheral | Function | Type | Available on ports: | | |
|------------|--------------------------|------|---------------------|---------|---------|
| ADC | AD0 | I | PIO0_30 | - | - |
| | AD1 | I | PIO0_31 | - | - |
| | AD2 | I | PIO1_0 | - | - |
| | AD3 | I | PIO1_1 | - | - |
| | AD4 | I | PIO1_2 | - | - |
| | AD5 | I | PIO1_3 | - | - |
| | AD6 | I | PIO1_4 | - | - |
| | AD7 | I | PIO1_5 | - | - |
| CT16B0 | CT16B0_CAP0 | I | PIO0_11 | PIO0_28 | PIO2_0 |
| | CT16B0_CAP1 | I | PIO0_12 | PIO0_29 | PIO2_1 |
| | CT16B0_MAT0 | O | PIO0_11 | PIO0_28 | PIO2_0 |
| | CT16B0_MAT1 | O | PIO0_12 | PIO0_29 | PIO2_1 |
| CT16B1 | CT16B1_CAP0 | I | PIO0_15 | PIO1_5 | PIO2_2 |
| | CT16B1_CAP1 | I | PIO0_16 | PIO1_6 | PIO2_3 |
| | CT16B1_MAT0 | O | PIO0_15 | PIO1_5 | PIO2_2 |
| | CT16B1_MAT1 | O | PIO0_16 | PIO1_6 | PIO2_3 |
| CT32B0 | CT32B0_CAP0 | I | PIO0_1 | PIO0_18 | PIO2_4 |
| | CT32B0_CAP1 | I | PIO0_2 | PIO0_19 | PIO2_5 |
| | CT32B0_CAP2 | I | PIO0_3 | PIO0_20 | PIO2_6 |
| | CT32B0_CAP3 | I | PIO0_4 | PIO0_21 | PIO2_7 |
| | CT32B0_MAT0 | O | PIO0_1 | PIO0_18 | PIO2_4 |
| | CT32B0_MAT1 | O | PIO0_2 | PIO0_19 | PIO2_5 |
| | CT32B0_MAT2 | O | PIO0_3 | PIO0_20 | PIO2_6 |
| | CT32B0_MAT3 | O | PIO0_4 | PIO0_21 | PIO2_7 |
| CT32B1 | CT32B1_CAP0 | I | PIO0_6 | PIO0_23 | PIO2_8 |
| | CT32B1_CAP1 | I | PIO0_7 | PIO0_24 | PIO2_9 |
| | CT32B1_CAP2 | I | PIO0_8 | PIO0_25 | PIO2_10 |
| | CT32B1_CAP3 | I | PIO0_9 | PIO0_26 | PIO2_11 |
| | CT32B1_MAT0 | O | PIO0_6 | PIO0_23 | PIO2_8 |
| | CT32B1_MAT1 | O | PIO0_7 | PIO0_24 | PIO2_9 |
| | CT32B1_MAT2 | O | PIO0_8 | PIO0_25 | PIO2_10 |
| | CT32B1_MAT3 | O | PIO0_9 | PIO0_26 | PIO2_11 |
| UART0 | RXD0 | I | PIO0_1 | PIO2_1 | - |
| | TXD0 | O | PIO0_2 | PIO2_2 | - |
| | $\overline{\text{CTS0}}$ | I | PIO0_7 | PIO2_4 | - |
| | $\overline{\text{DCD0}}$ | I | PIO0_5 | PIO2_6 | - |
| | $\overline{\text{DSR0}}$ | I | PIO0_4 | PIO2_7 | - |
| | $\overline{\text{DTR0}}$ | O | PIO0_3 | PIO2_3 | - |
| | $\overline{\text{RI0}}$ | I | PIO0_6 | PIO2_5 | - |
| | $\overline{\text{RTS0}}$ | O | PIO0_0 | PIO2_0 | - |

Table 4. Pin multiplexing

| Peripheral | Function | Type | Available on ports: | | |
|--------------|----------------------|------|---------------------|---------|---------|
| UART1 | RXD1 | I | PIO0_8 | PIO2_11 | PIO2_12 |
| | TXD1 | O | PIO0_9 | PIO2_10 | PIO2_13 |
| SSP/SPI | SCK | I/O | PIO0_14 | - | - |
| | MISO | I/O | PIO0_16 | - | - |
| | MOSI | I/O | PIO0_17 | - | - |
| | SSEL | I/O | PIO0_15 | - | - |
| I2C | SCL | I/O | PIO0_10 | - | - |
| | SDA | I/O | PIO0_11 | - | - |
| SWD | SWCLK ^[1] | I | PIO0_18 | PIO0_26 | - |
| | SWDIO ^[1] | I/O | PIO0_25 | PIO1_2 | - |
| Reset | RESET | I | PIO0_13 | - | - |
| Clockout pin | CLKOUT | O | PIO0_12 | - | - |

[1] After reset, the SWD functions are selected by default on pins PIO0_26 and PIO0_25.

7. Functional description

7.1 ARM Cortex-M0 processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption.

7.1.1 System tick timer

The ARM Cortex-M0 includes a System Tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

7.2 On-chip flash program memory

The LPC122x contain up to 128 kB of on-chip flash memory.

7.3 On-chip SRAM

The LPC122x contain a total of up to 8 kB on-chip static RAM memory.

7.4 Memory map

The LPC122x incorporates several distinct memory regions, shown in the following figures. [Figure 4](#) shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 megabyte in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kilobytes of space. This allows simplifying the address decoding for each peripheral.

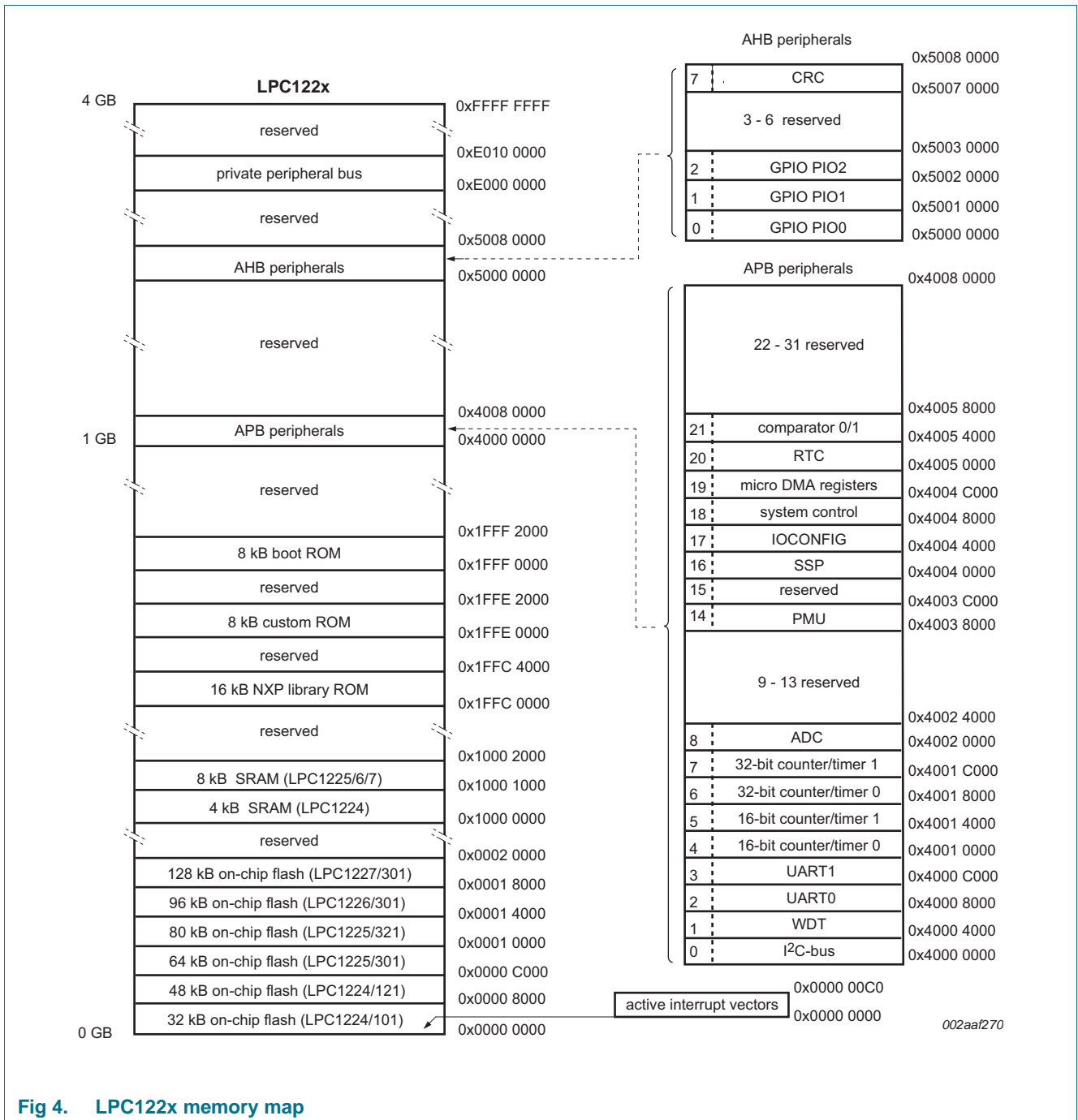


Fig 4. LPC122x memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- In the LPC122x, the NVIC supports 32 vectored interrupts. In addition, up to 12 of the individual GPIO inputs are NVIC-vector capable.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.
- Non-maskable Interrupt (NMI) can be programmed to use any of the peripheral interrupts. The NMI is not available on an external pin.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 55 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, a rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.6.1 Features

- Programmable pull-up resistor.
- Programmable digital glitch filter.
- Programmable input inverter.
- Programmable drive current.
- Programmable open-drain mode.

7.7 Micro DMA controller

The micro DMA controller enables memory-to-memory, memory-to-peripheral, and peripheral-to-memory data transfers. The supported peripherals are: UART0 (transmit and receive), UART1 (transmit and receive), SSP/SPI (transmit and receive), ADC, RTC, 32-bit counter/timer 0 (match output channels 0 and 1), 32-bit counter/timer 1 (match output channels 0 and 1), 16-bit counter/timer 0 (match output channel 0), 16-bit counter/timer 1 (match output channel 0), comparator 0, comparator 1, GPIO0 to GPIO2.

7.7.1 Features

- Single AHB-Lite master for transferring data using a 32-bit address bus and 32-bit data bus.
- 21 DMA channels.
- Handshake signals and priority level programmable for each channel.
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel number.

- Supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers.
- Supports multiple DMA cycle types and multiple DMA transfer widths.
- Performs all DMA transfers using the single AHB-Lite burst type.

7.8 CRC engine

The Cyclic Redundancy Check (CRC) engine with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.8.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
 - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
 - CRC-16: $x^{16} + x^{15} + x^2 + 1$
 - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU programmed I/O or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
 - 8-bit write: 1-cycle operation
 - 16-bit write: 2-cycle operation (8-bit \times 2-cycle)
 - 32-bit write: 4-cycle operation (8-bit \times 4-cycle)

7.9 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

7.9.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.

7.10 UARTs

The LPC122x contains two UARTs. UART0 supports full modem control and RS-485/9-bit mode and allows both software address detection and automatic hardware address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- 16-byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode (UART0).
- Support for modem control (UART0).

7.11 SSP/SPI serial I/O controller

The LPC122x contain one SSP/SPI controller. The SSP/SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I²C-bus serial I/O controller

The LPC122x contain one I²C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.12.1 Features

- The I²C-interface is a standard I²C-compliant bus interface with open-drain pins and supports I²C Fast-mode Plus with bit rates of up to 1 Mbit/s.
- Programmable digital glitch filter providing a 60 ns to 1 μ s input filter.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.

- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 10-bit ADC

The LPC122x contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to $V_{DD(3V3)}$.
- 10-bit conversion time of 257 kHz.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or counter/timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.14 Comparator block

The comparator block consists of two analog comparators.

7.14.1 Features

- Up to six selectable external sources per comparator; fully configurable on either positive or negative comparator input channels.
- BOD 0.9 V internal reference voltage selectable on both comparators; configurable on either positive or negative comparator input channels.
- 32-stage voltage ladder internal reference voltage selectable on both comparators; configurable on either positive or negative comparator input channels.
- Voltage ladder source voltage is selectable from an external pin or an internal 3.3 V voltage rail if external power source is not available.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Relaxation oscillator circuitry output for a feedback 555-style timer application.
- Common interrupt connected to NVIC.
- Comparator outputs selectable as synchronous or asynchronous.

- Comparator outputs connect to two timers, allowing for the recording of comparison event time stamps.

7.15 General purpose external event counter/timers

The LPC122x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes up to four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.15.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to four capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
 - Set LOW on match.
 - Set HIGH on match.
 - Toggle on match.
 - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Supports timed DMA requests.

7.16 Windowed WatchDog timer (WWDG)

The purpose of the watchdog is to reset the microcontroller within a windowed amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

7.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Safe operation: can be locked by software to be always on.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

- Selectable time period from $(T_{cy(WDCLK)} \times 256 \times 4)$ to $(T_{cy(WDCLK)} \times 2^{24} \times 4)$ in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC) or the Watchdog oscillator. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Real-time clock (RTC)

The RTC provides a basic alarm function or can be used as a long time base counter. The RTC generates an interrupt after counting for a programmed number of cycles of the RTC clock input.

7.17.1 Features

- Uses dedicated 32 kHz ultra low-power oscillator.
- Selectable clock inputs: RTC oscillator (1 Hz, delayed 1 Hz, or 1 kHz clock) or main clock with programmable clock divider.
- 32-bit counter.
- Programmable 32-bit match/compare register.
- Software maskable interrupt when counter and compare registers are identical.
- Generates wake-up from Deep-sleep and Deep power-down modes.

7.18 Clocking and power control

7.18.1 Crystal oscillators

The LPC122x include four independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), the RTC 32 kHz oscillator (for the RTC only), and the Watchdog oscillator. Except for the RTC oscillator, each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC122x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See [Figure 5](#) for an overview of the LPC122x clock generation.

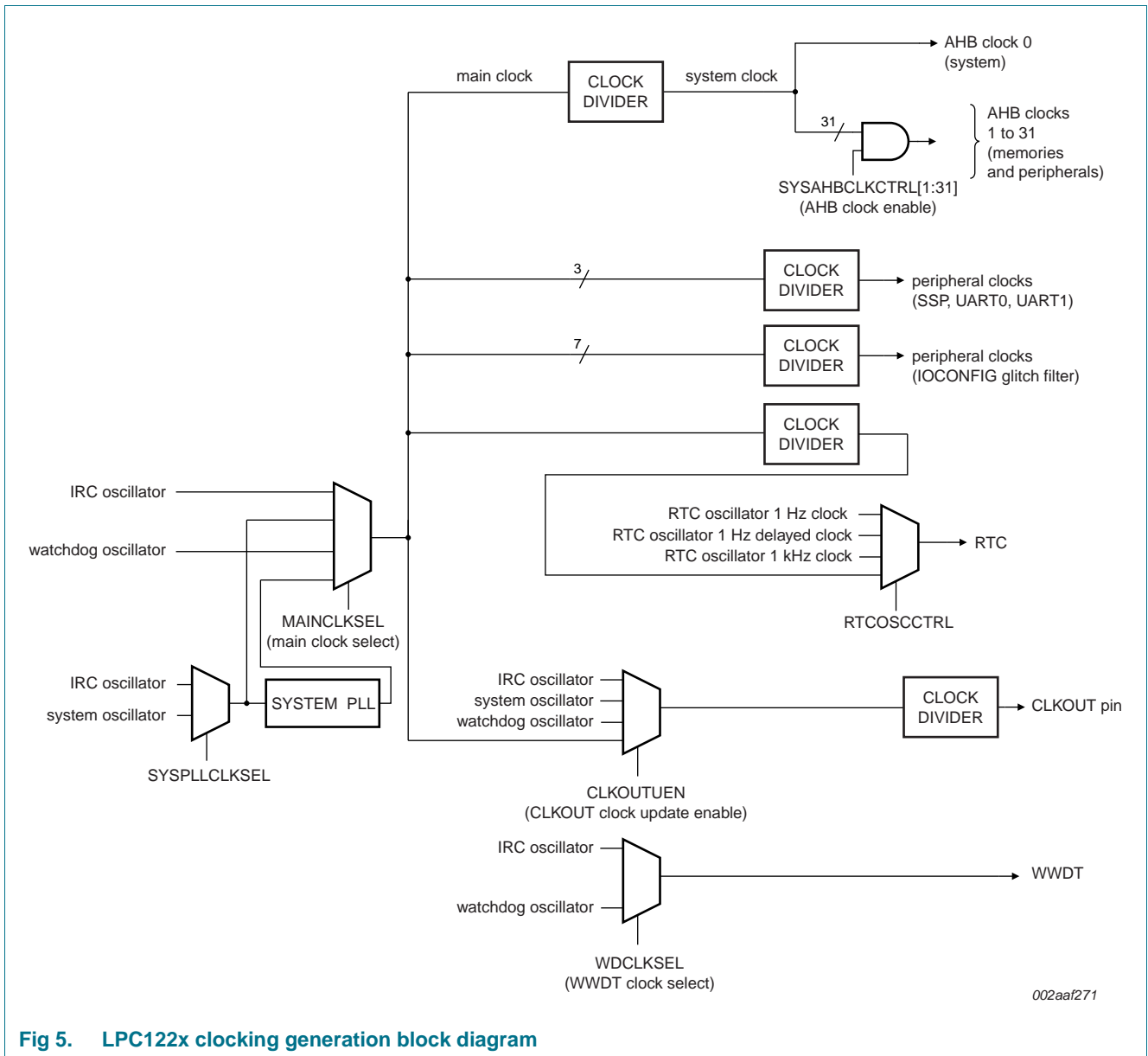


Fig 5. LPC122x clocking generation block diagram

7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC122x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL. The ARM processor clock frequency is referred to as CCLK elsewhere in this document.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is $\pm 40\%$.

7.18.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

7.18.3 Clock output

The LPC122x features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC122x begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5 Power control

The LPC122x support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.2 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

The GPIO pins PIO0_0 to PIO0_11 (up to 12 pins total) and the RTC match interrupt can serve as a wake-up input to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.18.5.3 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the Real Time Clock, the four general-purpose registers, and the WAKEUP pin. The LPC122x can wake up from Deep power-down mode via the WAKEUP pin or the RTC match interrupt.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.19 System control

7.19.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in [Table 3](#) as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.19.2 Reset

Reset has four sources on the LPC122x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.19.3 Brownout detection

The LPC122x includes four levels for monitoring the voltage on the $V_{\text{DD}(3\text{V3})}$ pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

7.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC122x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_12 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION



If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_12 for valid user code can be disabled.

7.19.5 APB interface

The APB peripherals are located on one APB bus.

7.19.6 AHB-Lite

The AHB-Lite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.19.7 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug is supported.

7.21 Integer division routines

The LPC122x contain performance-optimized integer division routines with support for up to 32-bit width in the numerator and denominator. Routines for signed and unsigned division and division with remainder are available. The integer division routines are ROM-based to reduce code-size.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---------------------------------------|---|----------------------|-------|------------------|
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | | 3.0 | 3.6 | V |
| $V_{DD(I/O)}$ | input/output supply voltage | | 3.0 | 3.6 | V |
| V_I | input voltage | on all digital pins | ^[2] -0.5 | +3.6 | V |
| | | on pins PIO0_10 and PIO0_11 (I ² C-bus pins) | 0 | 5.5 | V |
| I_{DD} | supply current | per supply pin | ^[3] - | 100 | mA |
| I_{SS} | ground current | per ground pin | ^[3] - | 100 | mA |
| I_{latch} | I/O latch-up current | $-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125\text{ }^\circ\text{C}$ | - | 100 | mA |
| T_{stg} | storage temperature | | ^[4] -65 | +150 | $^\circ\text{C}$ |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | - | 1.5 | W |
| V_{ESD} | electrostatic discharge voltage | human body model; all pins | ^[5] -8000 | +8000 | V |

[1] The following applies to the limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Dependent on package type.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.

9. Thermal characteristics

9.1 Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 6. Thermal characteristics

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C unless otherwise specified.}$

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---|-------------------------------|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC test board; no air flow | - | | | |
| | | LQFP64 package | | 61 | - | °C/W |
| | | LQFP48 package | | 86 | - | °C/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | JEDEC test board | - | | | |
| | | LQFP64 package | | 19 | - | °C/W |
| | | LQFP48 package | | 36 | - | °C/W |
| $T_{j(max)}$ | maximum junction temperature | | - | - | 150 | °C |

10. Static characteristics

Table 7. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|-----------------------------|--|---|--------------------|---------------|---------------|
| $V_{DD(I/O)}$ | input/output supply voltage | on pin $V_{DD(I/O)}$ | 3.0 | 3.3 | 3.6 | V |
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | | 3.0 | 3.3 | 3.6 | V |
| I_{DD} | supply current | Active mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; code while(1){} executed from flash | | | | |
| | | all peripherals disabled: | | | | |
| | | CCLK = 12 MHz | - | 4.6 | - | mA |
| | | CCLK = 24 MHz | - | 9 | - | mA |
| | | CCLK = 33 MHz | - | 12.2 | - | mA |
| | | all peripherals enabled: | | | | |
| | | CCLK = 12 MHz | - | 6.6 | - | mA |
| | | CCLK = 24 MHz | - | 10.9 | - | mA |
| | | CCLK = 33 MHz | - | 14.1 | - | mA |
| | | Sleep mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; all peripherals disabled | | | | |
| | | CCLK = 12 MHz | - | 1.8 | - | mA |
| | | CCLK = 24 MHz | - | 3.3 | - | mA |
| | | CCLK = 33 MHz | - | 4.4 | - | mA |
| | | Deep-sleep mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 30 | - | μA |
| | | Deep power-down mode; $V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 720 | - | nA |
| Normal-drive output pins (Standard port pins, RESET) | | | | | | |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$; | - | - | 100 | nA |
| I_{IH} | HIGH-level input current | $V_I = V_{DD(I/O)}$; | - | - | 100 | nA |
| I_{OZ} | OFF-state output current | $V_O = 0\text{ V}$; $V_O = V_{DD(I/O)}$; | - | - | 100 | nA |
| V_I | input voltage | pin configured to provide a digital function | [2] [3] [4] 0 | - | $V_{DD(I/O)}$ | V |
| V_O | output voltage | output active | 0 | - | $V_{DD(I/O)}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(I/O)}$ | - | - | V |

Table 7. Static characteristics ...continued
T_{amb} = -40 °C to +85 °C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|---|---|---------------------------------------|--------------------|-------------------------|------|
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{DD(I/O)} | V |
| V _{hys} | hysteresis voltage | | - | 0.4 | - | V |
| V _{OH} | HIGH-level output voltage | low mode; I _{OH} = -2 mA | V _{DD(I/O)} - 0.4 | - | - | V |
| | | high mode; I _{OH} = -4 mA | V _{DD(I/O)} - 0.4 | - | - | V |
| V _{OL} | LOW-level output voltage | low mode; I _{OL} = 2 mA | - | - | 0.4 | V |
| | | high mode; I _{OL} = 4 mA | - | - | 0.4 | V |
| I _{OH} | HIGH-level output current | low mode; V _{OH} = V _{DD(I/O)} - 0.4 V | -2 | - | - | mA |
| | | high mode; V _{OH} = V _{DD(I/O)} - 0.4 V | -4 | - | - | mA |
| I _{OL} | LOW-level output current | low mode; V _{OL} = 0.4 V | 2 | - | - | mA |
| | | high mode; V _{OL} = 0.4 V | 4 | - | - | mA |
| I _{OHS} | HIGH-level short-circuit output current | V _{OH} = 0 V | ^[5] - | - | -45 | mA |
| I _{OLS} | LOW-level short-circuit output current | V _{OL} = V _{DDA} | ^[5] - | - | 50 | mA |
| I _{pu} | pull-up current | V _I = 0 V | -50 | -80 | -100 | μA |
| High-drive output pins (PIO0_27, PIO0_28, PIO0_29, PIO0_12) | | | | | | |
| I _{IL} | LOW-level input current | V _I = 0 V; | - | - | 100 | nA |
| I _{IH} | HIGH-level input current | V _I = V _{DD(I/O)} ; | - | - | 100 | nA |
| I _{OZ} | OFF-state output current | V _O = 0 V; V _O = V _{DD(I/O)} ; | - | - | 100 | nA |
| V _I | input voltage | pin configured to provide a digital function | ^{[2][3]} 0 ^[4] | - | V _{DD(I/O)} | V |
| V _O | output voltage | output active | 0 | - | V _{DD(I/O)} | V |
| V _{IH} | HIGH-level input voltage | | 0.7V _{DD(I/O)} | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.3V _{DD(I/O)} | - |
| V _{hys} | hysteresis voltage | | - | - | - | V |
| V _{OH} | HIGH-level output voltage | low mode; I _{OH} = -20 mA | V _{DD(I/O)} - 0.7 | - | - | V |
| | | high mode; I _{OH} = -28 mA | V _{DD(I/O)} - 0.7 | - | - | V |
| V _{OL} | LOW-level output voltage | low mode; I _{OL} = 12 mA | - | - | 0.4 | V |
| | | high mode; I _{OL} = 18 mA | - | - | 0.4 | V |

Table 7. Static characteristics ...continued
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|--|--|------------------|--------------------|-----------------|---------------|
| I_{OH} | HIGH-level output current | low mode; $V_{OH} = V_{DD(IO)} - 0.7$ | 20 | - | - | mA |
| | | high mode; $V_{OH} = V_{DD(IO)} - 0.7$ | 28 | - | - | mA |
| I_{OL} | LOW-level output current | $V_{OL} = 0.4\text{ V}$ low mode | 12 | - | - | mA |
| | | high mode | 18 | - | - | mA |
| I_{OLS} | LOW-level short-circuit output current | $V_{OL} = V_{DD}$ | ^[5] - | - | - | mA |
| I_{pu} | pull-up current | $V_I = 0\text{ V}$ | -50 | -80 | -100 | μA |
| I²C-bus pins (PIO0_10 and PIO0_11) | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD(IO)}$ | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | $0.3V_{DD(IO)}$ | V |
| V_{hys} | hysteresis voltage | | - | $0.05V_{DD(IO)}$ | - | V |
| V_{OL} | LOW-level output voltage | $I_{OLS} = 20\text{ mA}$ | - | - | 0.4 | V |
| I_{LI} | input leakage current | $V_I = V_{DD(IO)}$ | ^[6] - | 2 | 4 | μA |
| | | $V_I = 5\text{ V}$ | - | 10 | 22 | μA |
| C_i | capacitance for each I/O pin | on pins PIO0_10 and PIO0_11 | - | - | 8 | pF |
| Oscillator pins | | | | | | |
| $V_{i(xtal)}$ | crystal input voltage | see Section 12.1 | 0 | 1.8 | 1.95 | V |
| $V_{o(xtal)}$ | crystal output voltage | | 0 | 1.8 | 1.95 | V |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Including voltage on outputs in 3-state mode.

[3] $V_{DD(3V3)}$ and $V_{DD(IO)}$ supply voltages must be present.

[4] 3-state outputs go into 3-state mode when $V_{DD(IO)}$ is grounded.

[5] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[6] To V_{SS} .

10.1 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25\text{ °C}$ and $V_{DD(3V3)} = 3.3\text{ V}$.

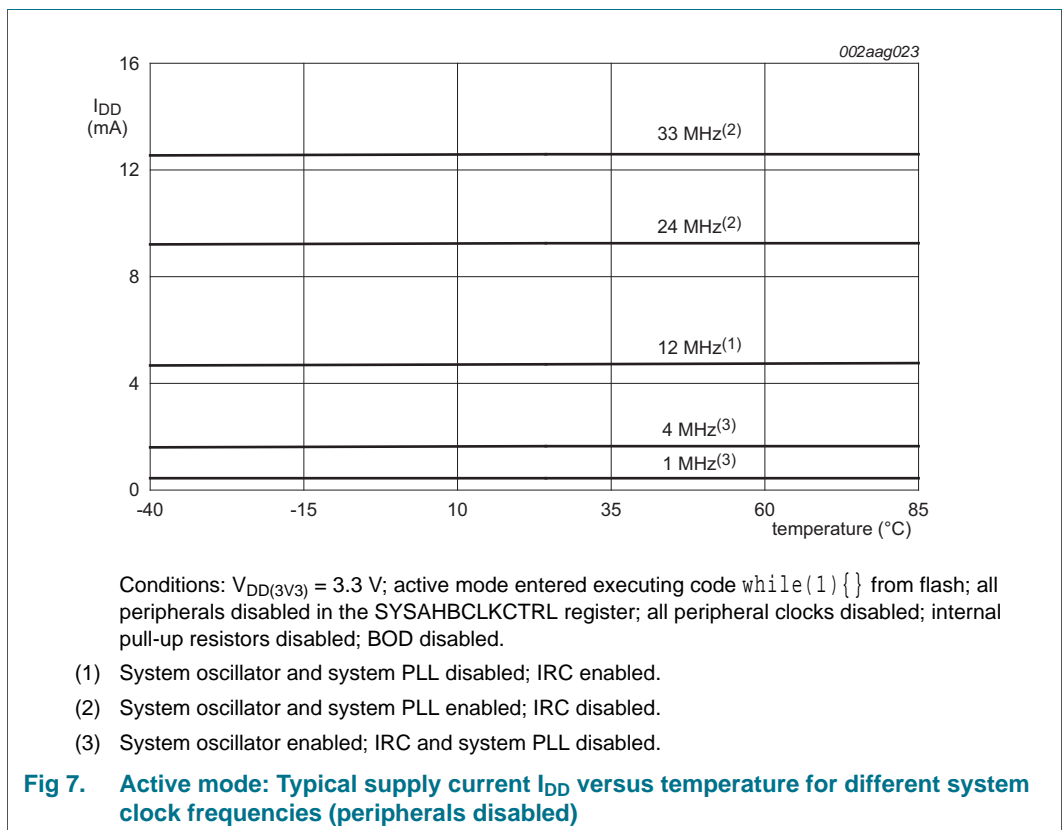
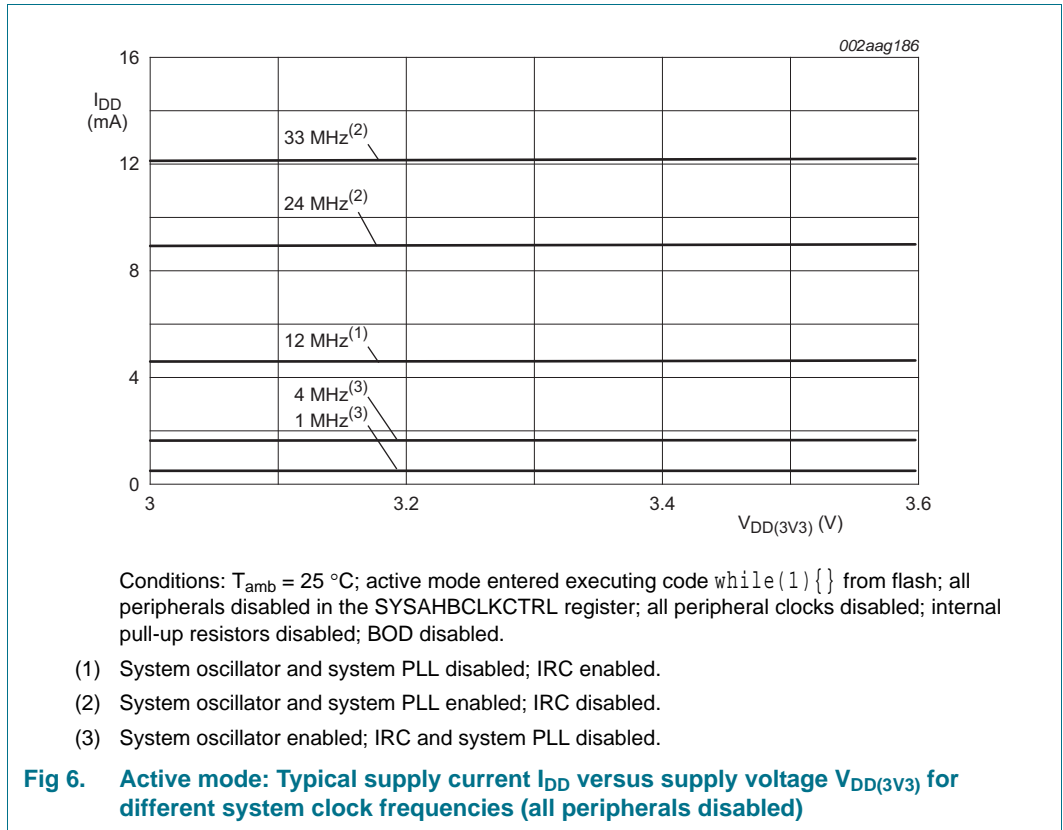
Table 8. Peripheral power consumption

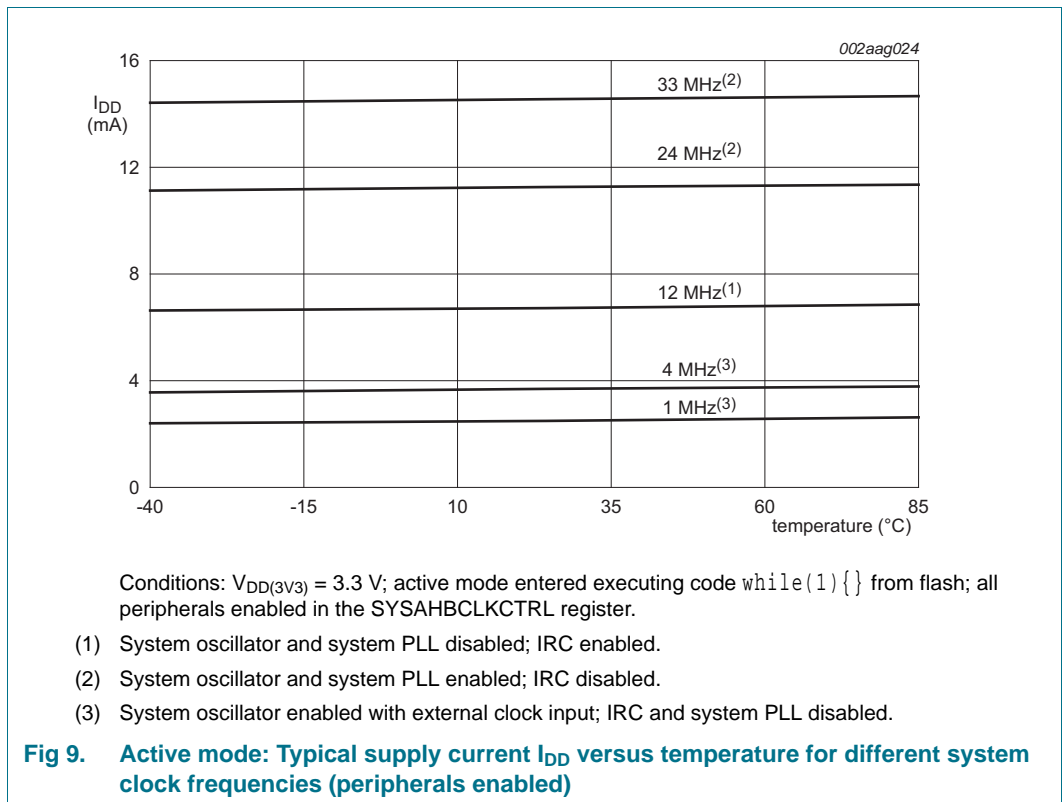
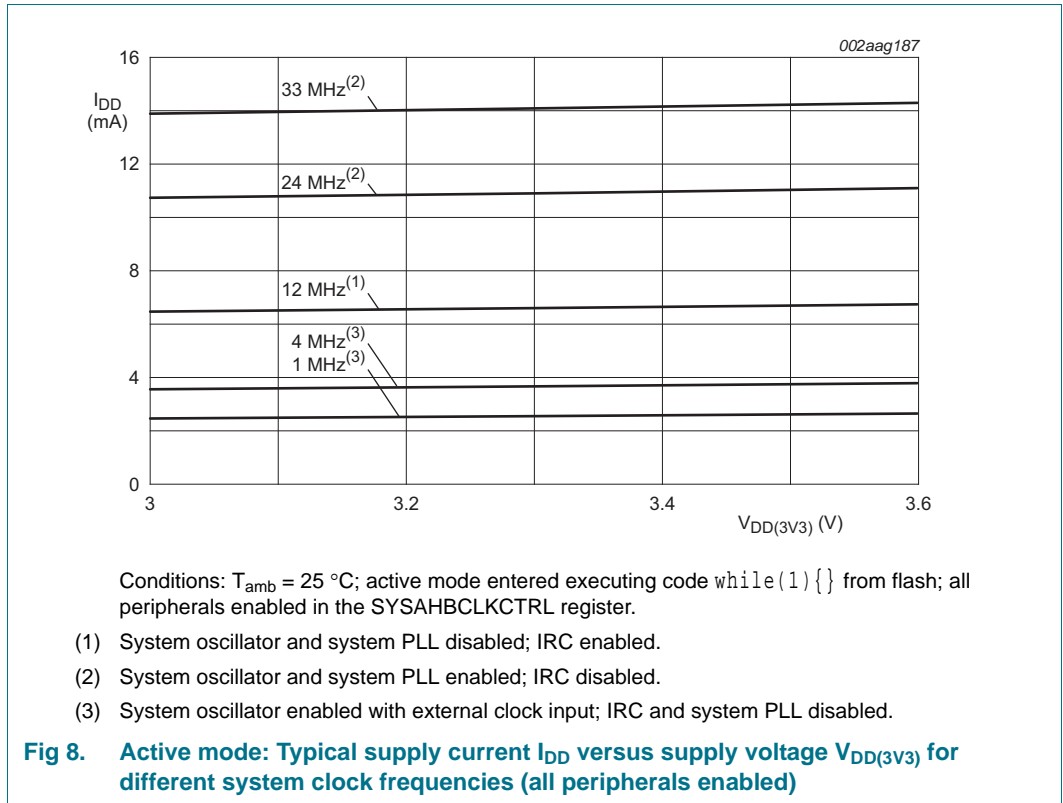
| Peripheral | Typical current consumption I_{DD} in mA | Frequency independent | | | |
|--|--|--------------------------------------|-----------|--------------------------------|------|
| | | 24 MHz system oscillator + PLL | IRC + PLL | 12 MHz system oscillator | IRC |
| IRC | 0.29 | - | - | - | - |
| PLL (PLL output frequency = 24 MHz) | 1.87 | - | - | - | - |
| WDosc (WDosc output frequency = 500 kHz) | 0.25 | - | - | - | - |
| BOD | 0.06 | - | - | - | - |
| Analog comparator 0/1 | - | 0.05 | 0.05 | 0.03 | 0.02 |
| ADC | - | 1.86 | 1.85 | 1.61 | 1.61 |
| CRC engine | - | 0.04 | 0.04 | 0.02 | 0.02 |
| 16-bit timer 0 (CT16B0) | - | 0.09 | 0.09 | 0.04 | 0.04 |
| 16-bit timer 1 (CT16B1) | - | 0.09 | 0.09 | 0.04 | 0.04 |
| 32-bit timer 0 (CT32B0) | - | 0.08 | 0.08 | 0.04 | 0.04 |
| 32-bit timer 1 (CT32B1) | - | 0.08 | 0.08 | 0.04 | 0.04 |
| GPIO0 | - | 0.34 | 0.34 | 0.17 | 0.17 |
| GPIO1 | - | 0.34 | 0.34 | 0.17 | 0.17 |
| GPIO2 | - | 0.36 | 0.37 | 0.18 | 0.18 |
| I2C | - | 0.09 | 0.09 | 0.05 | 0.05 |
| IOCON | - | 0.09 | 0.10 | 0.05 | 0.05 |
| RTC | - | 0.10 | 0.10 | 0.05 | 0.05 |
| SSP | - | 0.30 | 0.29 | 0.15 | 0.15 |
| UART0 | - | 0.52 | 0.51 | 0.26 | 0.26 |
| UART1 | - | 0.52 | 0.51 | 0.26 | 0.26 |
| DMA | - | 0.18 | 0.18 | 0.09 | 0.09 |
| WWDT | - | 0.06 | 0.06 | 0.03 | 0.03 |

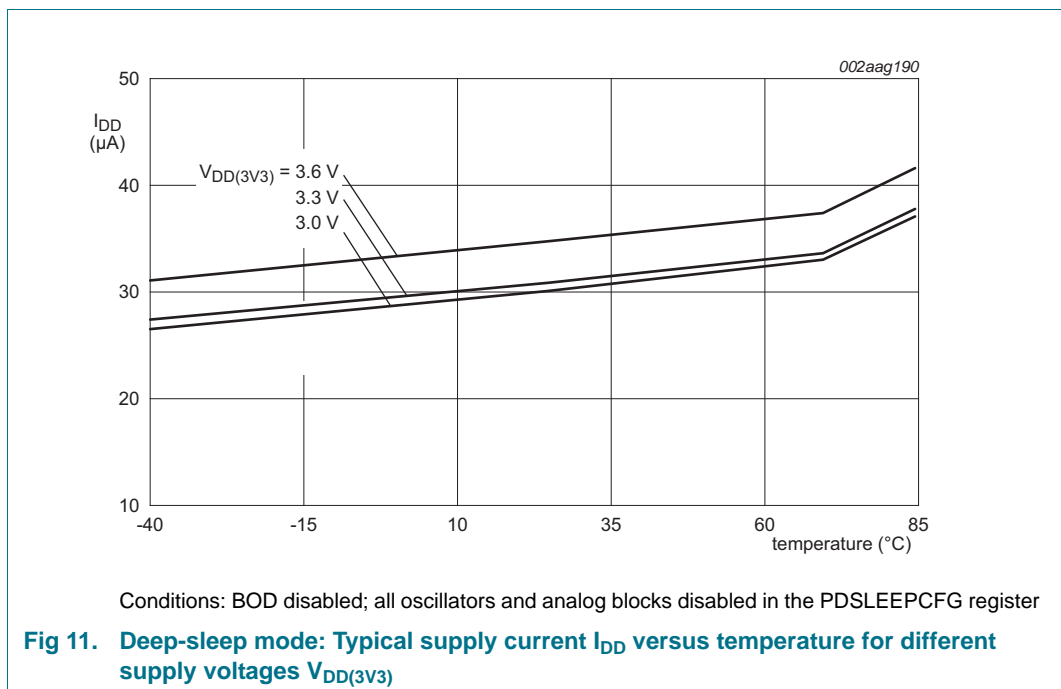
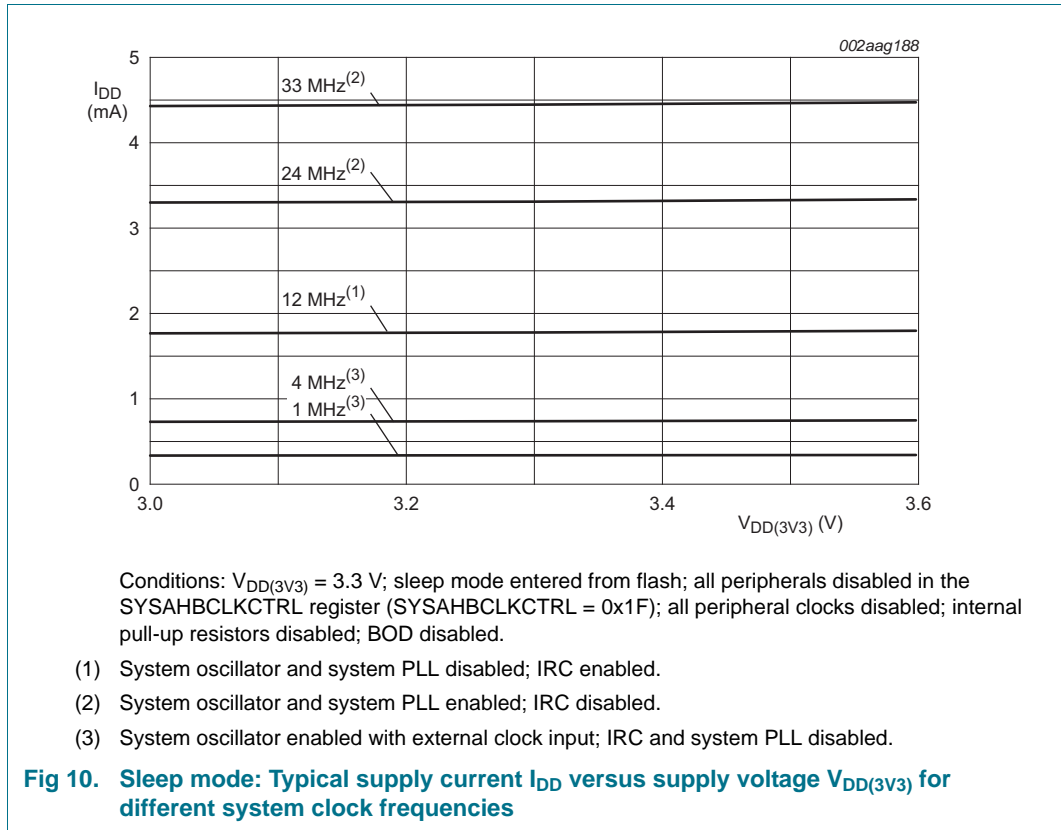
10.2 Power consumption

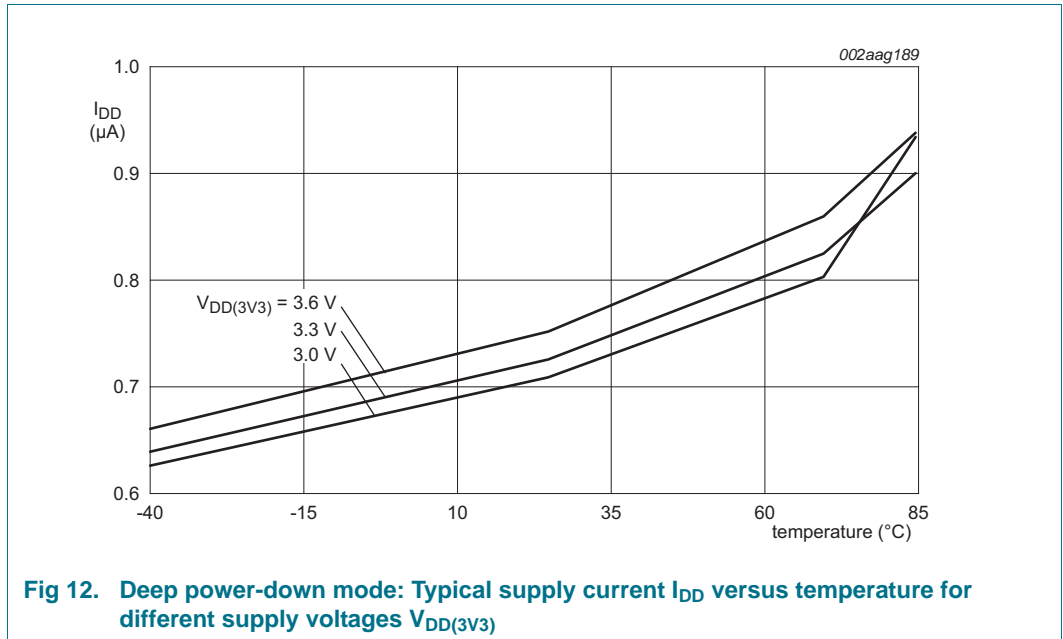
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC122x user manual*):

- Active mode: all GPIO pins set to input with external pull-up resistors.
- Sleep and Deep-sleep modes: all GPIO pins set to output driving LOW.
- Deep power-down mode: all GPIO pins set to input with external pull-up resistors.

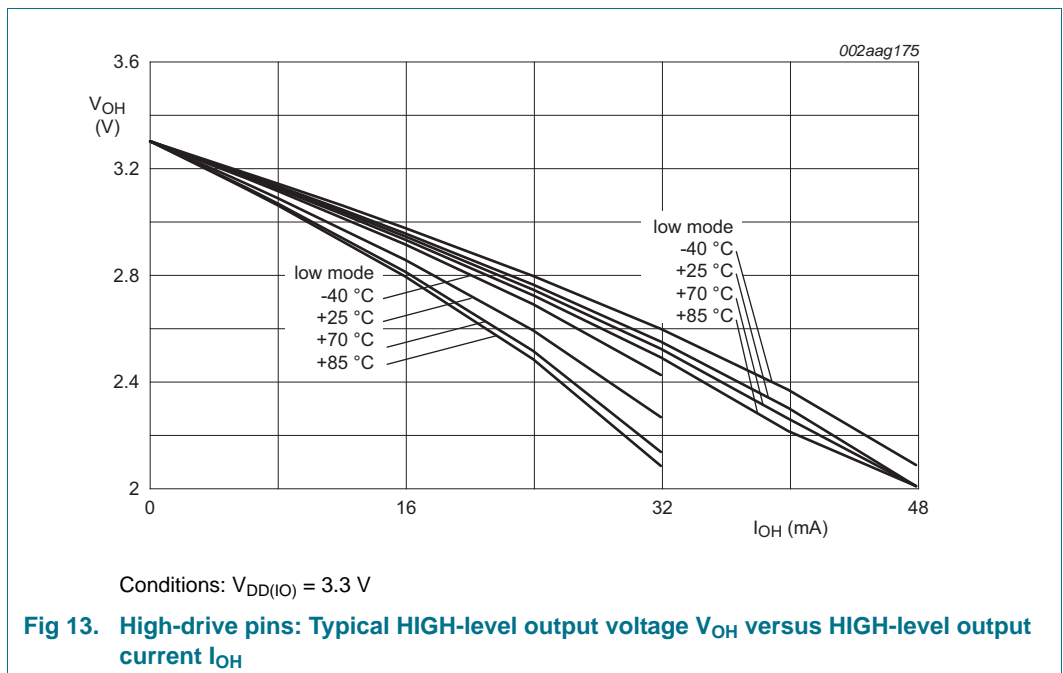


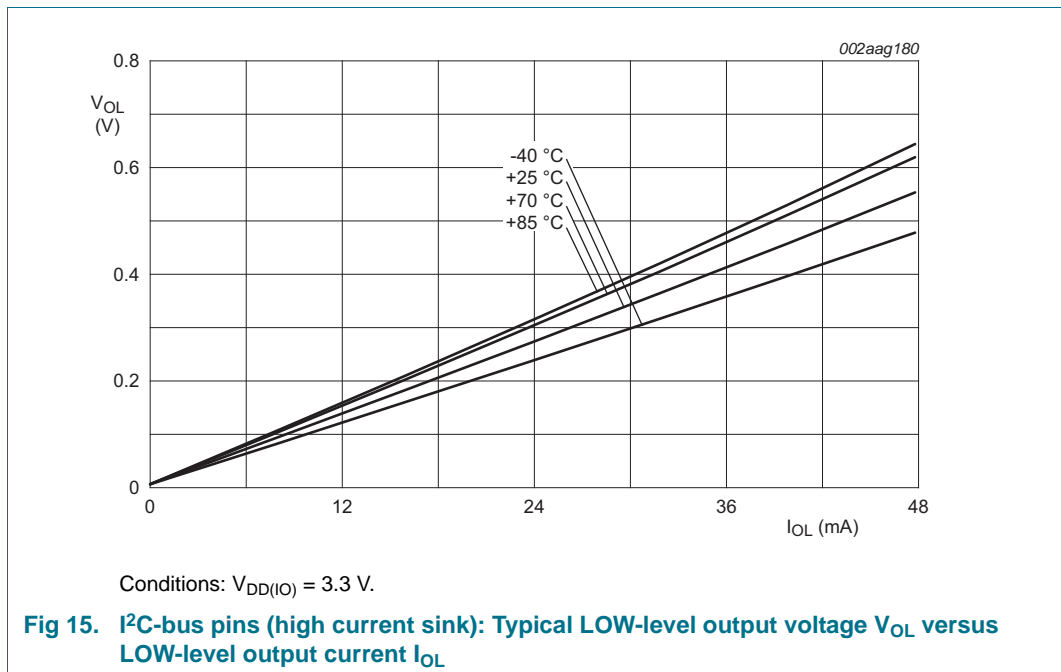
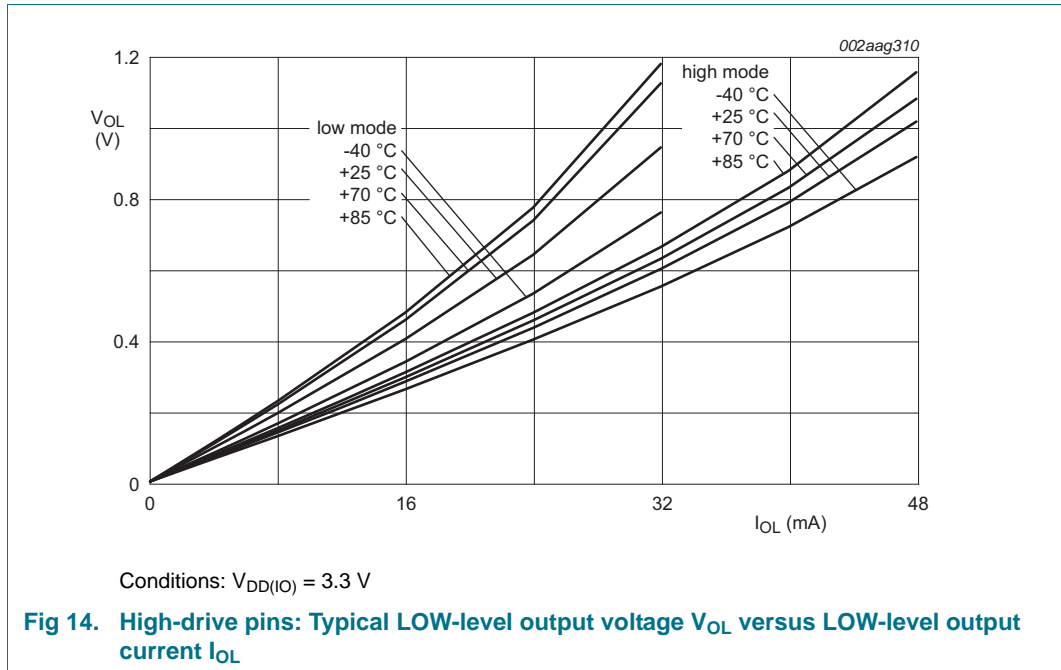


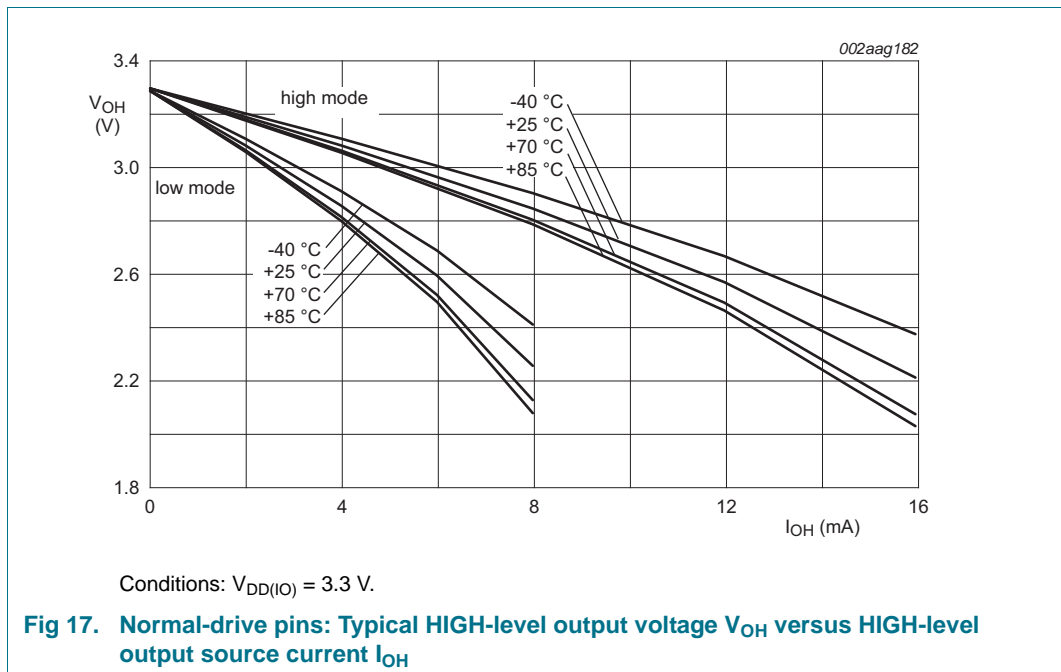
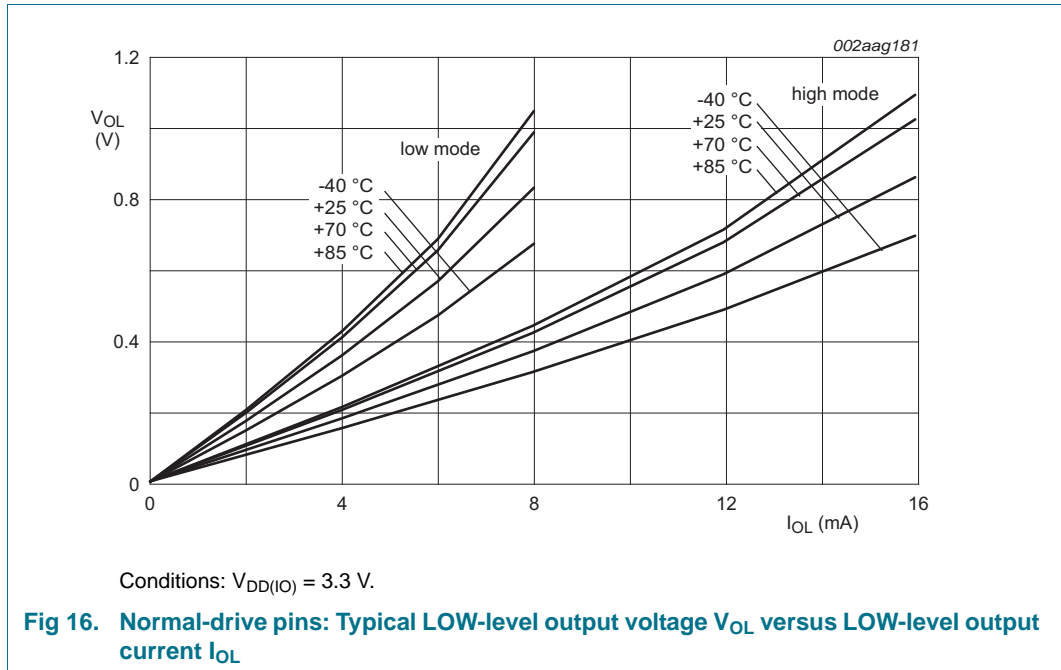


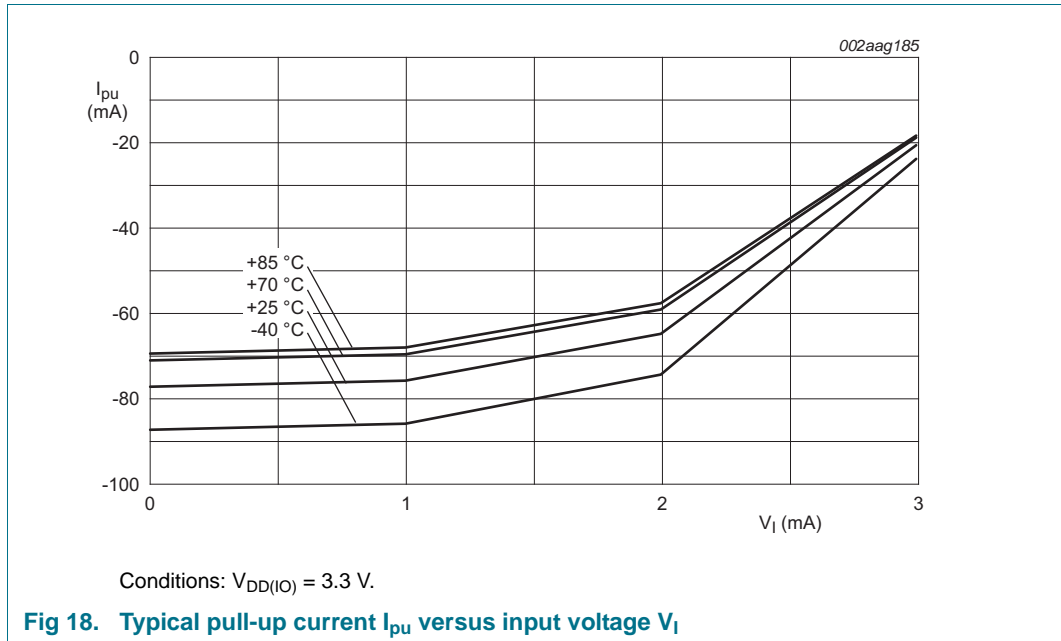


10.3 Electrical pin characteristics









10.4 ADC characteristics

Table 9. ADC static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency 9 MHz, $V_{DD(3V3)} = 3.0\text{ V}$ to 3.6 V .

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--------------|------------------------------|---------------------------|-----|--------------------|---------------|-----------|
| V_{IA} | analog input voltage | | 0 | - | $V_{DD(3V3)}$ | V |
| C_{ia} | analog input capacitance | | - | - | 1 | pF |
| E_D | differential linearity error | [2][3][4] | - | - | ± 1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | [2][5] | - | - | ± 2.5 | LSB |
| E_O | offset error | [2][6] | - | - | ± 1 | LSB |
| E_G | gain error | [2][7] | - | - | ± 3 | LSB |
| E_T | absolute error | [2][8] | - | - | ± 3 | LSB |
| $f_{c(ADC)}$ | ADC conversion frequency | | - | - | 257 | kHz |
| R_i | input resistance | [9][10] | - | - | 3.9 | $M\Omega$ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Conditions: $V_{SS} = 0\text{ V}$, $V_{DD(3V3)} = 3.3\text{ V}$.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 19](#).

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 19](#).

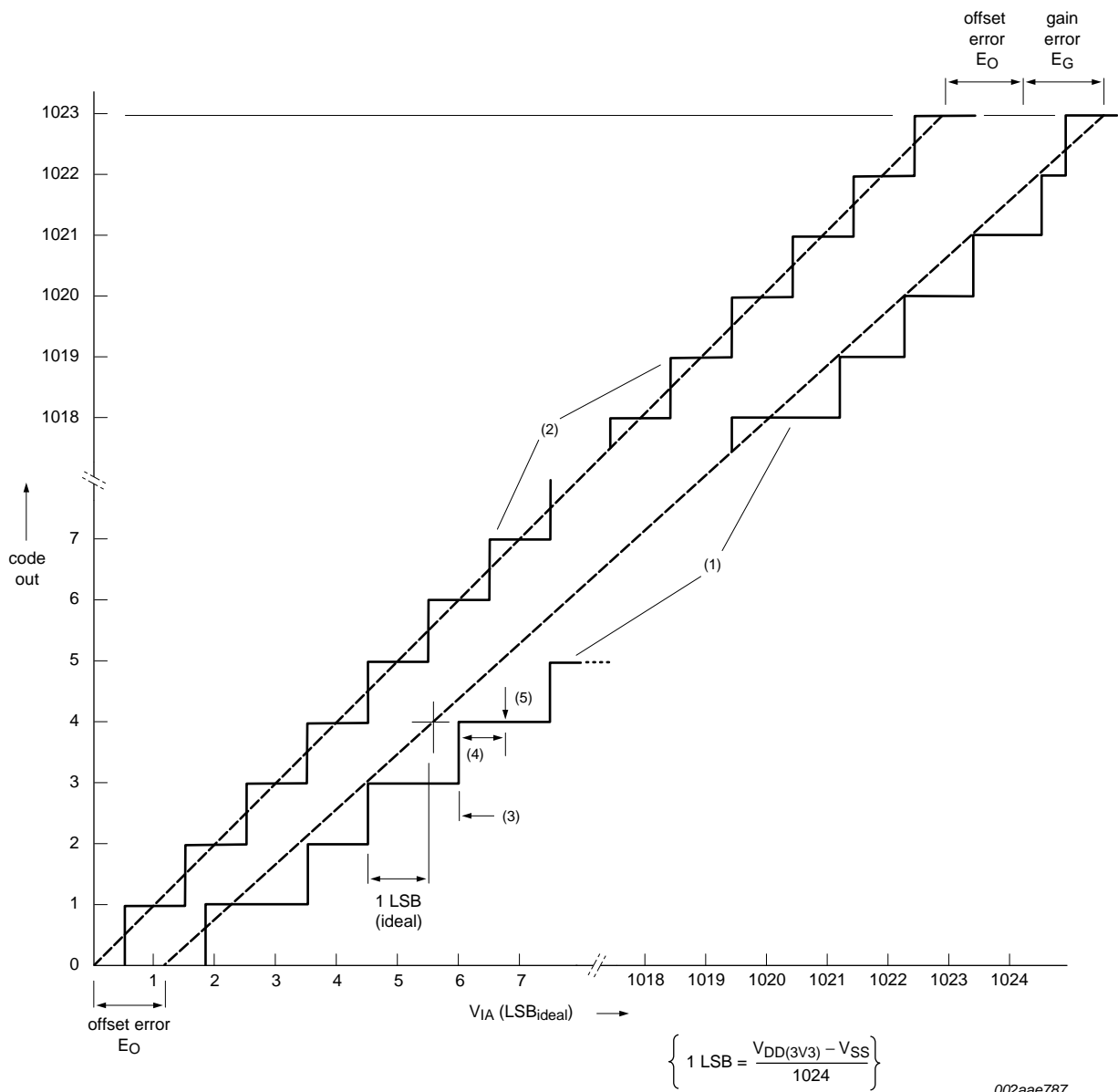
[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 19](#).

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 19](#).

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 19](#).

[9] $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum sampling frequency $f_s = 257\text{ kHz}$ and analog input capacitance $C_{ia} = 1\text{ pF}$.

[10] Input resistance R_i depends on the sampling frequency f_s : $R_i = 1 / (f_s \times C_{ia})$.



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- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 19. ADC characteristics

10.5 BOD static characteristics

Table 10. BOD static characteristics^[1]

$T_{amb} = 25\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-------------------|-------------------|-----|------|-----|------|
| V_{th} | threshold voltage | interrupt level 1 | | | | |
| | | assertion | - | 2.25 | - | V |
| | | de-assertion | - | 2.39 | - | V |
| | | interrupt level 2 | | | | |
| | | assertion | - | 2.54 | - | V |
| | | de-assertion | - | 2.67 | - | V |
| | | interrupt level 3 | | | | |
| | | assertion | - | 2.83 | - | V |
| | | de-assertion | - | 2.93 | - | V |
| | | reset level 1 | | | | |
| | | assertion | - | 2.04 | - | V |
| | | de-assertion | - | 2.18 | - | V |
| | | reset level 2 | | | | |
| | | assertion | - | 2.34 | - | V |
| | | de-assertion | - | 2.47 | - | V |
| | | reset level 3 | | | | |
| | | assertion | - | 2.62 | - | V |
| | | de-assertion | - | 2.76 | - | V |

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC122x user manual*.

11. Dynamic characteristics

11.1 Power-up ramp conditions

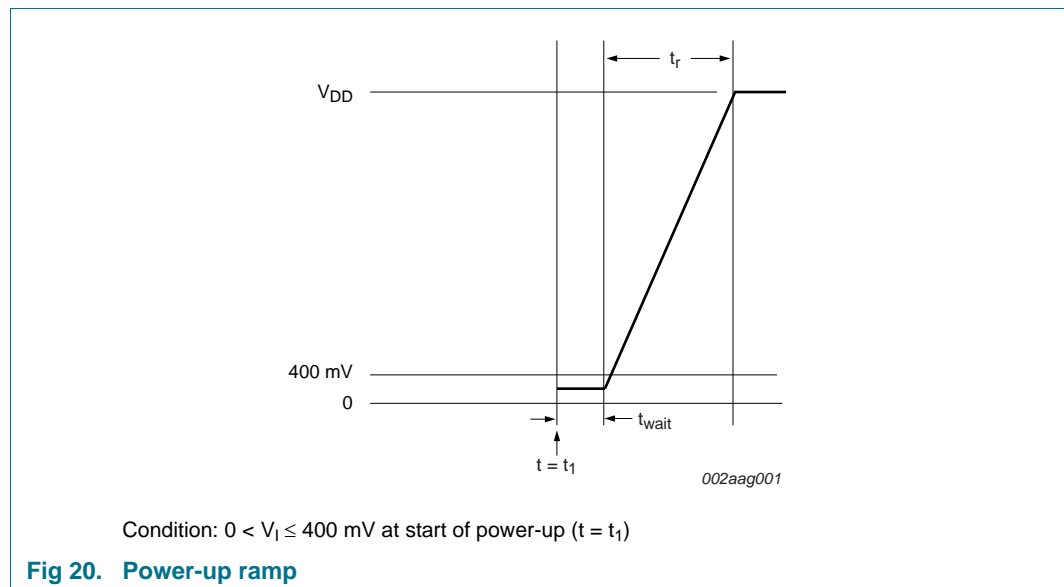
Table 11. Power-up characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|---------------|---|-----------|-----|-----|---------------|
| t_r | rise time | at $t = t_1$: $0 < V_1 \leq 400\text{ mV}$ | [1] 0 | - | 500 | ms |
| t_{wait} | wait time | | [1][2] 12 | - | - | μs |
| V_1 | input voltage | at $t = t_1$ on pin V_{DD} | 0 | - | 400 | mV |

[1] See [Figure 20](#).

[2] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.



11.2 Flash memory

Table 12. Dynamic characteristic: flash memory

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|------------------|---------------------------------|-----------|-----|---------------|
| t_{er} | erase time | for one page (512 byte) | [1] - | 20 | ms |
| | | for one sector (4 kB) | [1] | 162 | ms |
| | | for all sectors; mass erase | [1] - | 20 | ms |
| t_{prog} | programming time | one word (4 bytes) | [1] - | 49 | μs |
| | | four sequential words | [1] - | 194 | μs |
| | | 128 bytes (one row of 32 words) | [1] - | 765 | μs |
| N_{endu} | endurance | | [2] 20000 | - | cycles |
| t_{ret} | retention time | | 10 | - | years |

[1] Erase and programming times are valid over the lifetime of the device (minimum 20000 cycles).

[2] Number of program/erase cycles.

11.3 External clock

Table 13. Dynamic characteristic: external clock

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.[1]

| Symbol | Parameter | Conditions | Min | Typ[2] | Max | Unit |
|---------------|----------------------|------------|--------------------------|--------|------|------|
| f_{osc} | oscillator frequency | | 1 | - | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | 40 | - | 1000 | ns |
| t_{CHCX} | clock HIGH time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| t_{CLCX} | clock LOW time | | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| t_{CLCH} | clock rise time | | - | - | 5 | ns |
| t_{CHCL} | clock fall time | | - | - | 5 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

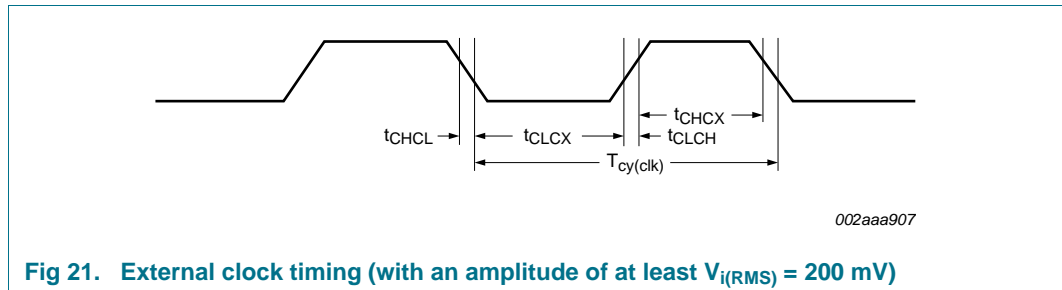


Fig 21. External clock timing (with an amplitude of at least $V_{i(RMS)} = 200\text{ mV}$)

11.4 Internal oscillators

Table 14. Dynamic characteristic: internal oscillators

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $V_{DD(3V3)}$ over specified ranges.^[1]

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|---------------|----------------------------------|------------|-------|--------------------|-------|------|
| $f_{osc(RC)}$ | internal RC oscillator frequency | - | 11.88 | 12 | 12.12 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

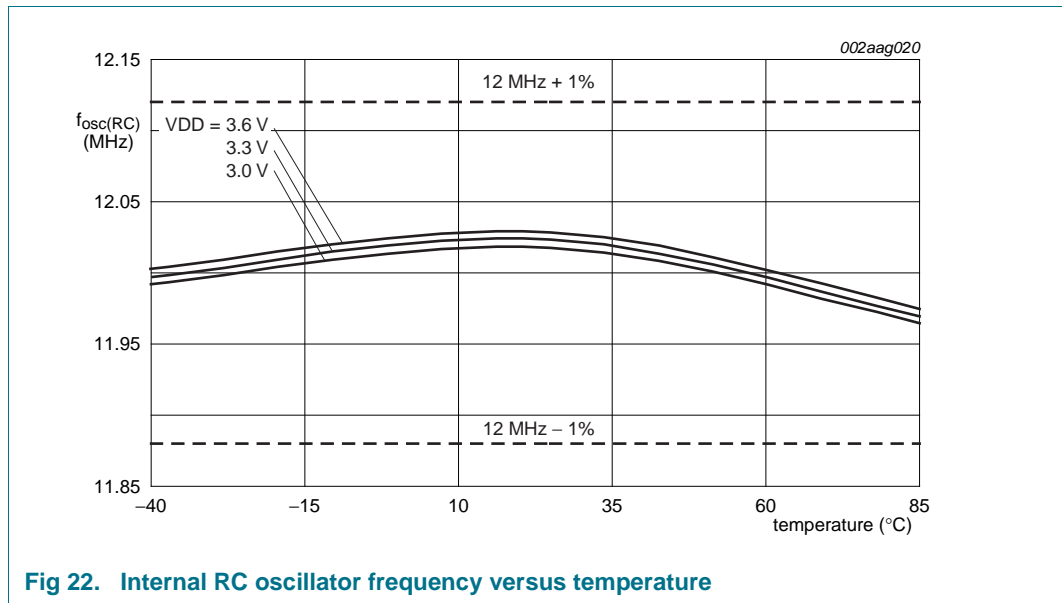


Fig 22. Internal RC oscillator frequency versus temperature

Table 15. Dynamic characteristics: Watchdog oscillator

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------------|-------------------------------|--|---------------------|--------------------|-----|------|
| $f_{osc(int)}$ | internal oscillator frequency | DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; | ^{[2][3]} - | 7.8 | - | kHz |
| | | DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register | ^{[2][3]} - | 1700 | - | kHz |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) is $\pm 40\%$.

[3] See the *LPC122x user manual*.

11.5 I²C-busTable 16. Dynamic characteristic: I²C-bus pins $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.^[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|------------------------------|---|-----------------------|-----|------|
| f _{SCL} | SCL clock frequency | Standard-mode | 0 | 100 | kHz |
| | | Fast-mode | 0 | 400 | kHz |
| | | Fast-mode Plus | 0 | 1 | MHz |
| t _f | fall time | ^{[3][4][5][6]} of both SDA and SCL signals | - | 300 | ns |
| | | Standard-mode | | | |
| | | Fast-mode | $20 + 0.1 \times C_b$ | 300 | ns |
| t _{LOW} | LOW period of the SCL clock | Standard-mode | 4.7 | - | μs |
| | | Fast-mode | 1.3 | - | μs |
| | | Fast-mode Plus | 0.5 | - | μs |
| t _{HIGH} | HIGH period of the SCL clock | Standard-mode | 4.0 | - | μs |
| | | Fast-mode | 0.6 | - | μs |
| | | Fast-mode Plus | 0.26 | - | μs |
| t _{HD;DAT} | data hold time | ^{[2][3][7]} Standard-mode | 0 | - | μs |
| | | Fast-mode | 0 | - | μs |
| | | Fast-mode Plus | 0 | - | μs |
| t _{SU;DAT} | data set-up time | ^{[8][9]} Standard-mode | 250 | - | ns |
| | | Fast-mode | 100 | - | ns |
| | | Fast-mode Plus | 50 | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] t_{HD;DAT} is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH(min)} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[7] The maximum t_{HD;DAT} could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of t_{VD;DAT} or t_{VD;ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[8] t_{SU;DAT} is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[9] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement t_{SU;DAT} = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

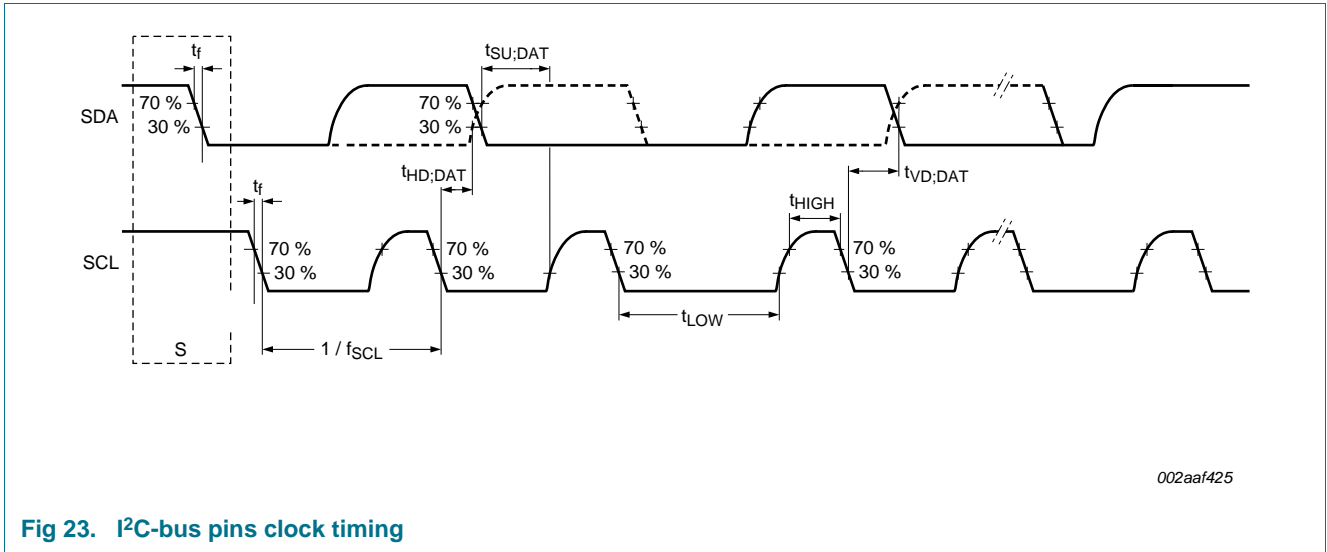


Fig 23. I²C-bus pins clock timing

12. Application information

12.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100$ pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

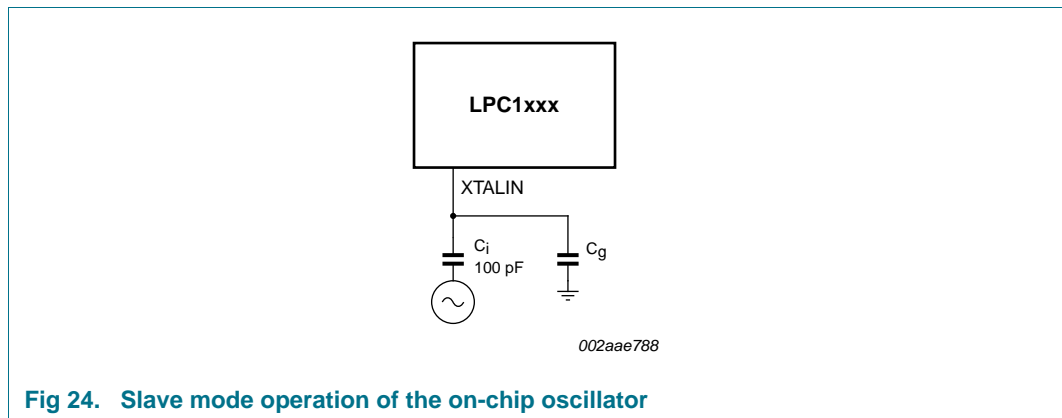


Fig 24. Slave mode operation of the on-chip oscillator

12.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1} , C_{x2} , and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

12.3 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1227FBD64/301 in [Table 17](#).

Table 17. ElectroMagnetic Compatibility (EMC) for part LPC1227FBD64/301 (TEM-cell method)

$V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$.

| Parameter | Frequency band | System clock = | | | Unit |
|---|------------------|----------------|--------|--------|------------|
| | | 12 MHz | 24 MHz | 33 MHz | |
| Input clock: IRC (12 MHz) | | | | | |
| maximum peak level | 150 kHz - 30 MHz | -4.2 | -3.8 | -6.4 | dB μ V |
| | 30 MHz - 150 MHz | 7.3 | 5.4 | 9 | dB μ V |
| | 150 MHz - 1 GHz | 16.4 | 20.1 | 23.4 | dB μ V |
| IEC level ^[1] | - | M | L | L | - |
| Input clock: crystal oscillator (12 MHz) | | | | | |
| maximum peak level | 150 kHz - 30 MHz | -4.8 | -4 | -6.6 | dB μ V |
| | 30 MHz - 150 MHz | 6.9 | 5.6 | 10 | dB μ V |
| | 150 MHz - 1 GHz | 16.3 | 20.3 | 22.3 | dB μ V |
| IEC level ^[1] | - | M | L | L | - |

[1] IEC levels refer to *Appendix D in the IEC61967-2 Specification*.

13. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm

SOT314-2

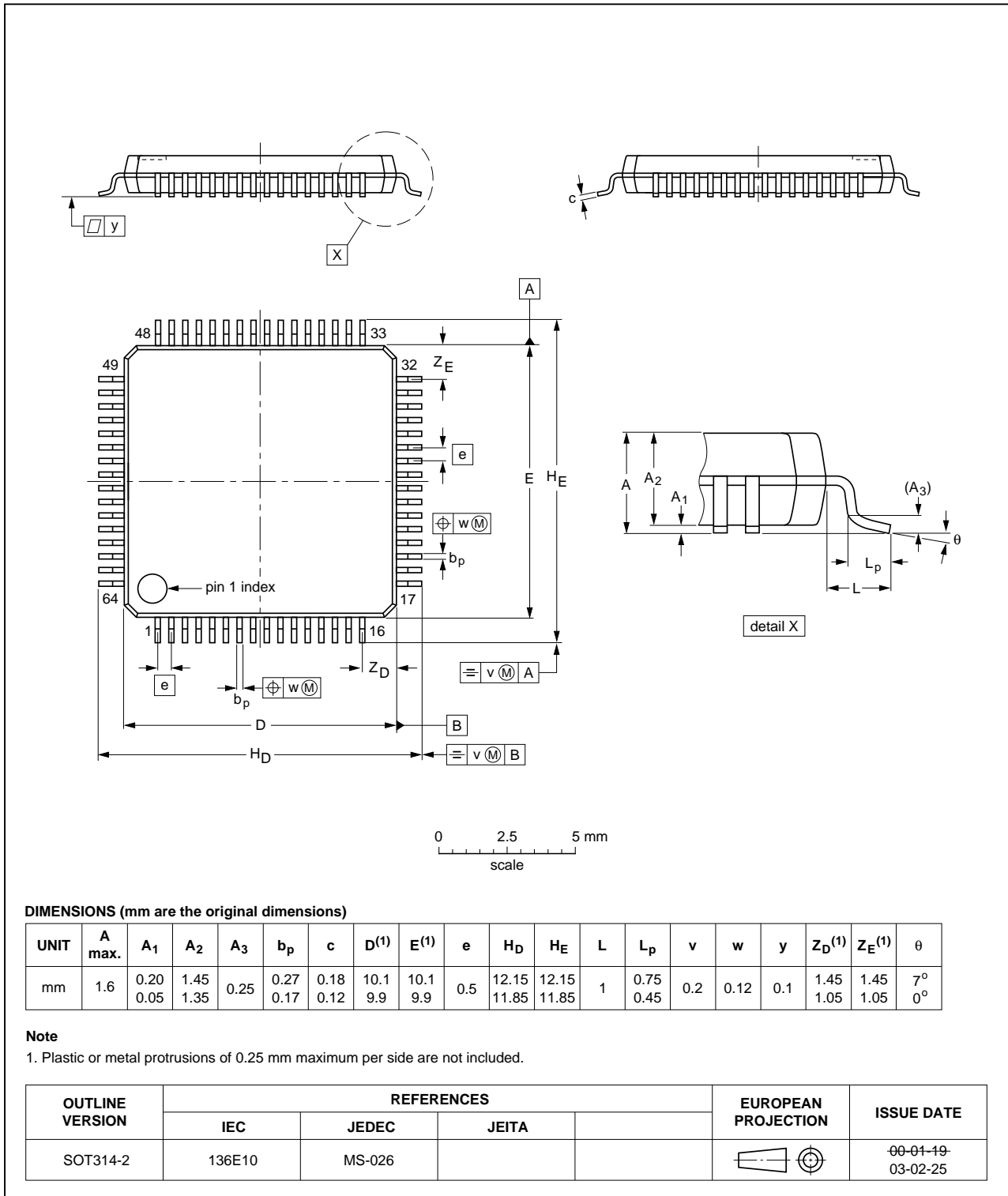


Fig 25. Package outline SOT314-2 (LQFP64)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2

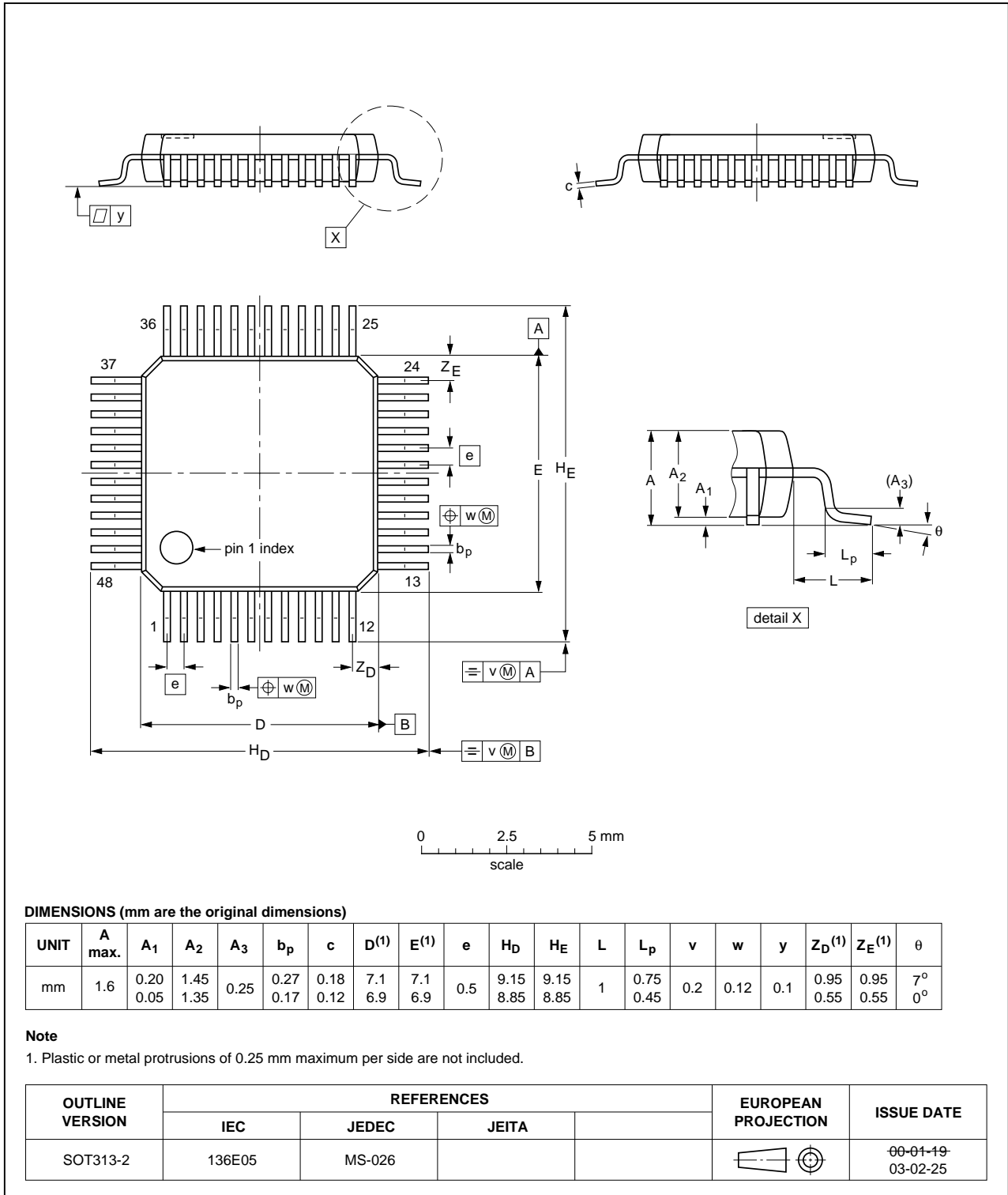


Fig 26. Package outline SOT313-2 (LQFP48)

14. Soldering

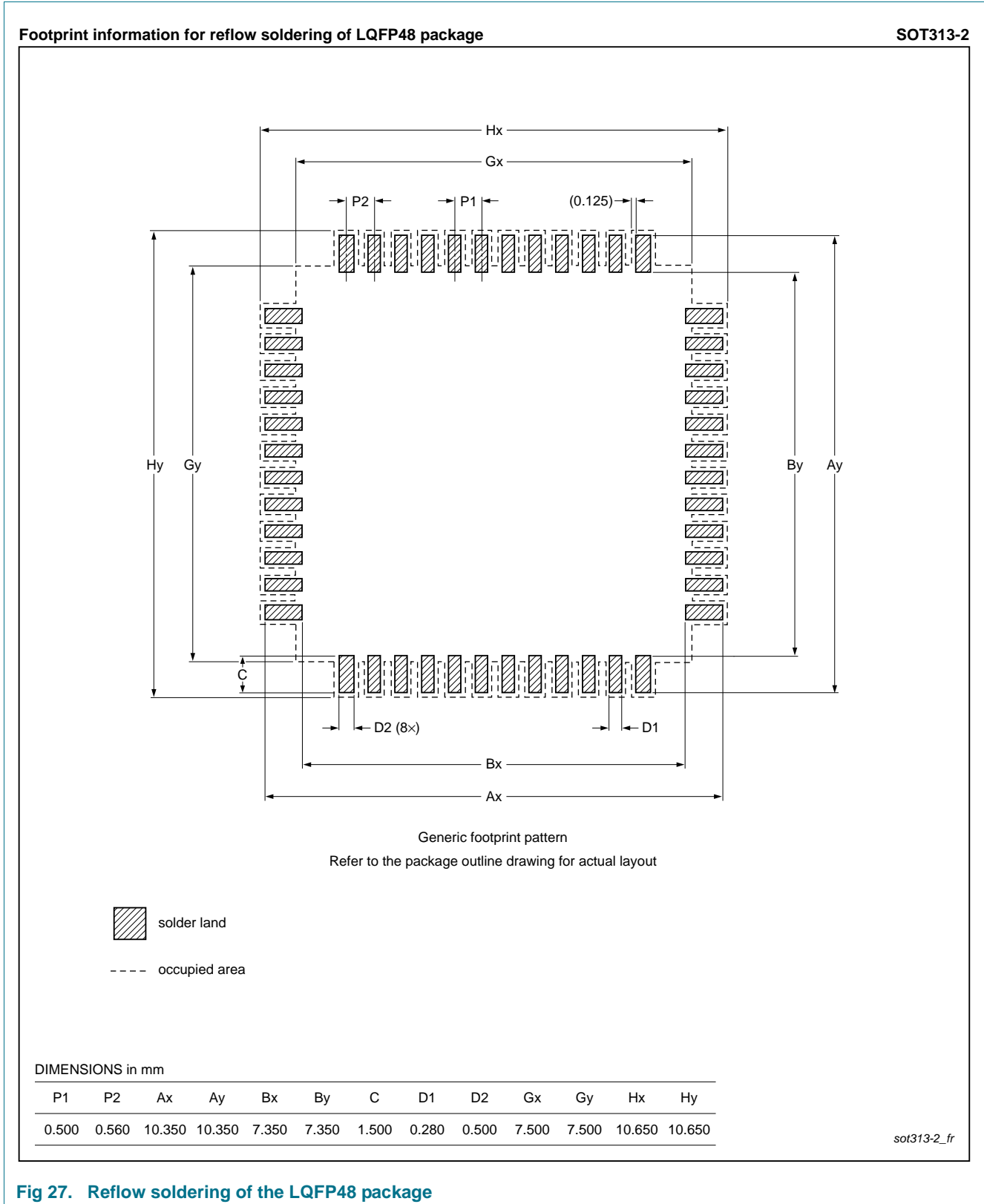


Fig 27. Reflow soldering of the LQFP48 package

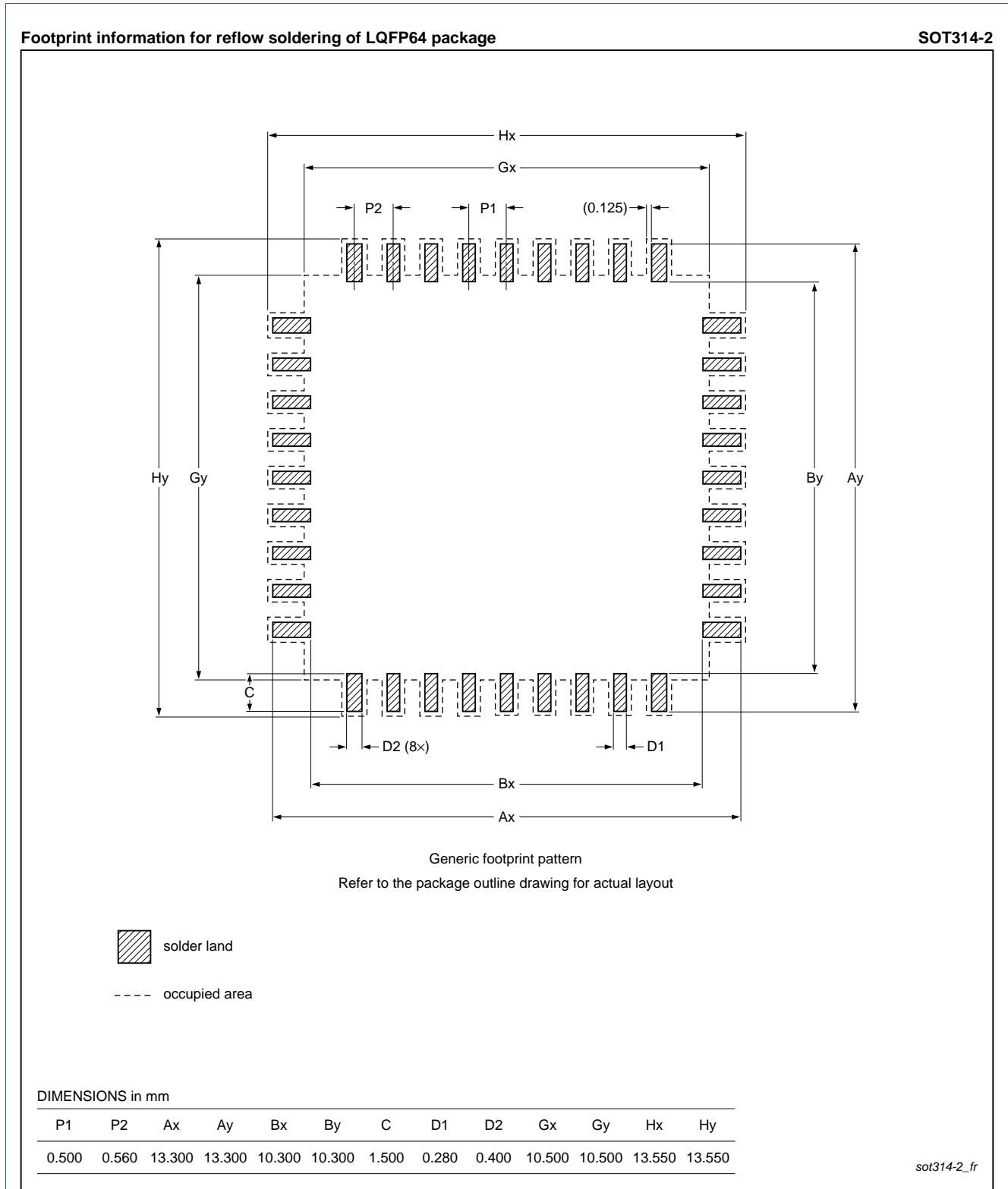


Fig 28. Reflow soldering of the LQFP64 package

15. Abbreviations

Table 18. Abbreviations

| Acronym | Description |
|---------|--|
| ADC | Analog-to-Digital-Converter |
| AHB | Advanced High-performance Bus |
| APB | Advanced Peripheral Bus |
| BOD | BrownOut Detection |
| CCITT | Comité Consultatif International Téléphonique et Télégraphique |
| CRC | Cyclic Redundancy Check |
| DMA | Direct Memory Access |
| FIFO | First-In-First-Out |
| GPIO | General Purpose Input/Output |
| I/O | Input/Output |
| IrDA | Infrared Data Association |
| IRC | Internal Resistor-Capacitor |
| JEDEC | Joint Electron Devices Engineering Council |
| PLL | Phase-Locked Loop |
| SPI | Serial Peripheral Interface |
| SSI | Serial Synchronous Interface |
| SSP | Synchronous Serial Port |
| UART | Universal Asynchronous Receiver/Transmitter |

16. Revision history

Table 19. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|----------------------|---------------|---------------|
| LPC122X v.2 | 20110826 | Product data sheet | - | LPC122X v.1.2 |
| Modifications: | <ul style="list-style-type: none"> • Power consumption data updated in Table 7. • Power consumption graphs added in Section 10.2. • Electrical pin characteristics updated for all pins in Table 7 and Section 10.3. • Parameter R_i added to Table 9. • EMC data added (Section 12.3). • Parameter V_I updated for I²C-bus pins in Table 5. • Section 11.1 "Power-up ramp conditions" added. • Data sheet status updated to Product Data Sheet. • SSP dynamic characteristics removed. | | | |
| LPC122X v.1.2 | 20110329 | Objective data sheet | - | LPC122X v.1.1 |
| Modifications: | <ul style="list-style-type: none"> • Figure 2 "Pin configuration LQFP64 package": Pin RTCXIN changed to 58 and pin RTCXOUT changed to 57. • Table 3 "LPC122x pin description": In column Pin LQFP64, pin RTCXIN changed to 58 and pin RTCXOUT changed to 57. | | | |
| LPC122X v.1.1 | 20110221 | Objective data sheet | - | LPC122X v.1 |
| Modifications: | <ul style="list-style-type: none"> • Section 1 "General description": Updated text. • Section 2 "Features and benefits": Updated text. | | | |
| LPC122X v.1 | 20110214 | Objective data sheet | - | - |

17. Legal information

17.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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