# PDTC114Y series

## NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 47 kΩ

Rev. 7 — 18 November 2011 | Product data sheet

## 1. Product profile

### 1.1 General description

NPN Resistor-Equipped Transistor (RET) family in Surface-Mounted Device (SMD) plastic packages.

**Table 1. Product overview**

| Type number | Package | | | PNP complement | Package configuration |
|---|---|---|---|---|---|
| | NXP | JEITA | JEDEC | | |
| PDTC114YE | SOT416 | SC-75 | - | PDTA114YE | ultra small |
| PDTC114YM | SOT883 | SC-101 | - | PDTA114YM | leadless ultra small |
| PDTC114YT | SOT23 | - | TO-236AB | PDTA114YT | small |
| PDTC114YU | SOT323 | SC-70 | - | PDTA114YU | very small |

### 1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

### 1.3 Applications

- Digital applications in automotive and industrial segments
- Control of IC inputs
- Cost-saving alternative for BC847/857 series in digital applications
- Switching loads

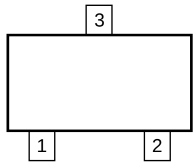
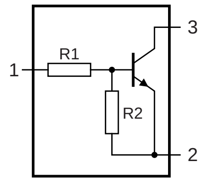
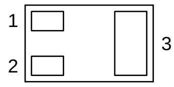
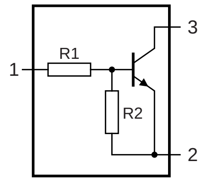
### 1.4 Quick reference data

**Table 2. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | 50 | V |
| $I_O$ | output current | | - | - | 100 | mA |
| R1 | bias resistor 1 (input) | | 7 | 10 | 13 | kΩ |
| R2/R1 | bias resistor ratio | | 3.7 | 4.7 | 5.7 | |

## 2. Pinning information

**Table 3. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| **SOT23; SOT323; SOT416** | | | |
| 1 | input (base) |  006aaa144 |  sym007 |
| 2 | GND (emitter) | | |
| 3 | output (collector) | | |
| **SOT883** | | | |
| 1 | input (base) |  Transparent top view |  sym007 |
| 2 | GND (emitter) | | |
| 3 | output (collector) | | |

## 3. Ordering information

**Table 4. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PDTC114YE | SC-75 | plastic surface-mounted package; 3 leads | SOT416 |
| PDTC114YM | SC-101 | leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm | SOT883 |
| PDTC114YT | - | plastic surface-mounted package; 3 leads | SOT23 |
| PDTC114YU | SC-70 | plastic surface-mounted package; 3 leads | SOT323 |

## 4. Marking

**Table 5. Marking codes**

| Type number | Marking code[1] |
|---|---|
| PDTC114YE | 33 |
| PDTC114YM | DU |
| PDTC114YT | *27 |
| PDTC114YU | *30 |

[1] * = placeholder for manufacturing site code

## 5. Limiting values

**Table 6. Limiting values**

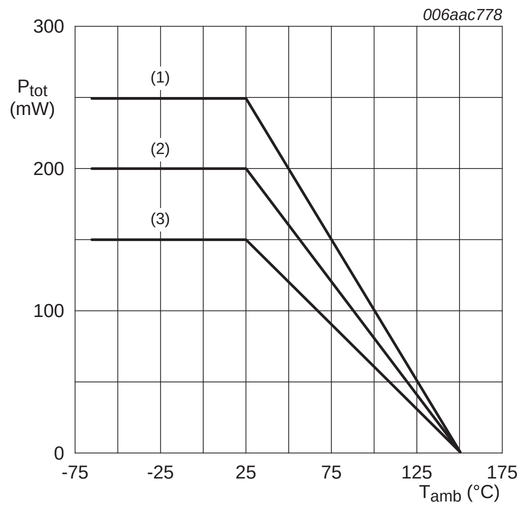
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CBO}$ | collector-base voltage | open emitter | - | 50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | - | 50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | - | 6 | V |
| $V_I$ | input voltage | | | | |
| | positive | | - | +40 | V |
| | negative | | - | −6 | V |
| $I_O$ | output current | | - | 100 | mA |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | - | 100 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | | | |
| | PDTC114YE (SOT416) | [1][2] | - | 150 | mW |
| | PDTC114YM (SOT883) | [2][3] | - | 250 | mW |
| | PDTC114YT (SOT23) | [1] | - | 250 | mW |
| | PDTC114YU (SOT323) | [1] | - | 200 | mW |
| $T_j$ | junction temperature | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | −65 | +150 | °C |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.




(1) SOT23; FR4 PCB, standard footprint
SOT883; FR4 PCB with 70 μm copper strip line, standard footprint

(2) SOT323; FR4 PCB, standard footprint

(3) SOT416; FR4 PCB, standard footprint

**Fig 1. Power derating curves**

## 6. Thermal characteristics

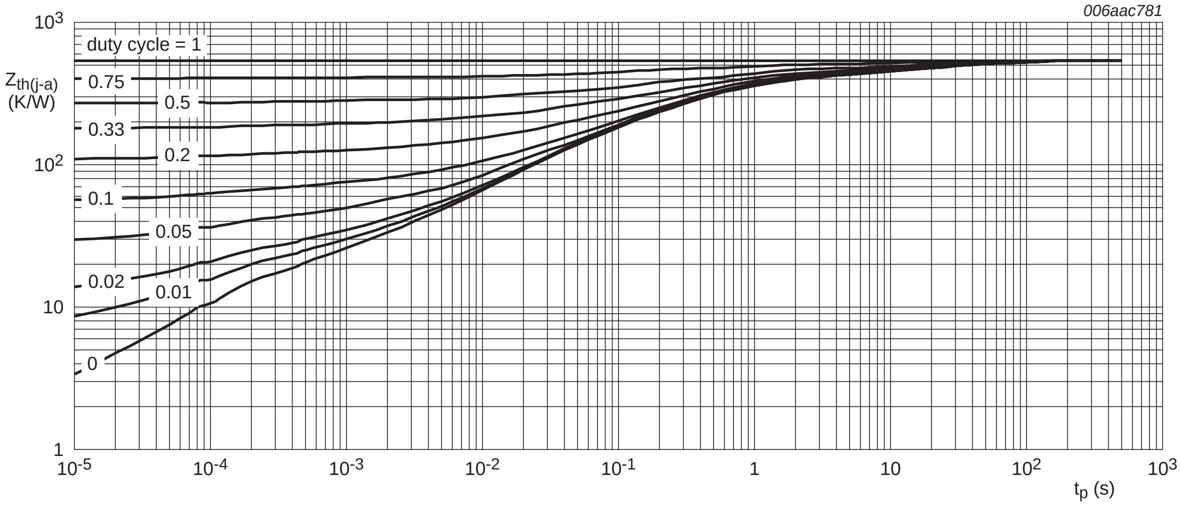
**Table 7. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | | | | |
| | PDTC114YE (SOT416) | | [1][2] | - | - | 830 | K/W |
| | PDTC114YM (SOT883) | | [2][3] | - | - | 500 | K/W |
| | PDTC114YT (SOT23) | | [1] | - | - | 500 | K/W |
| | PDTC114YU (SOT323) | | [1] | - | - | 625 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

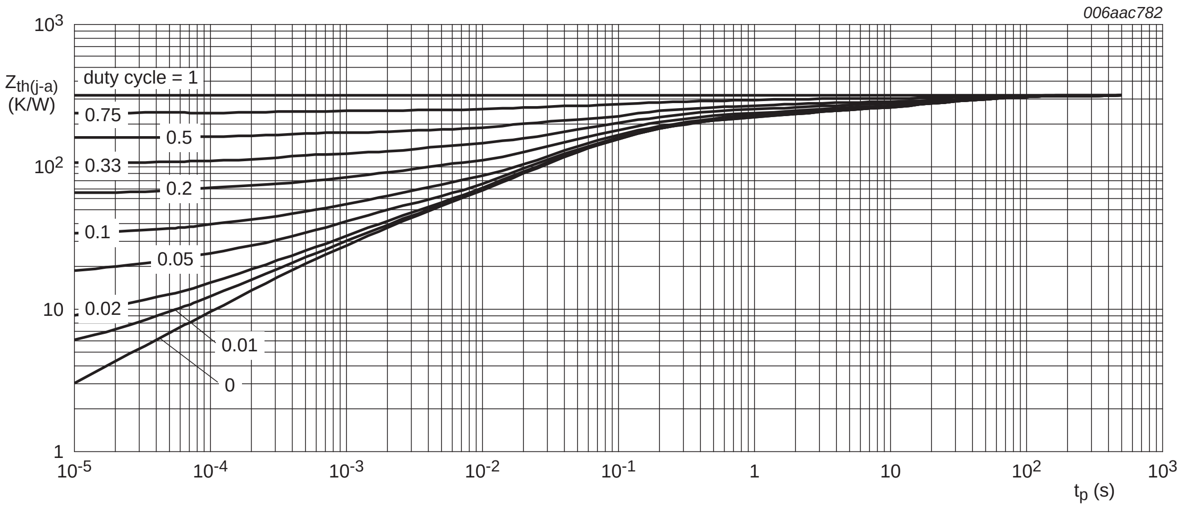
[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.



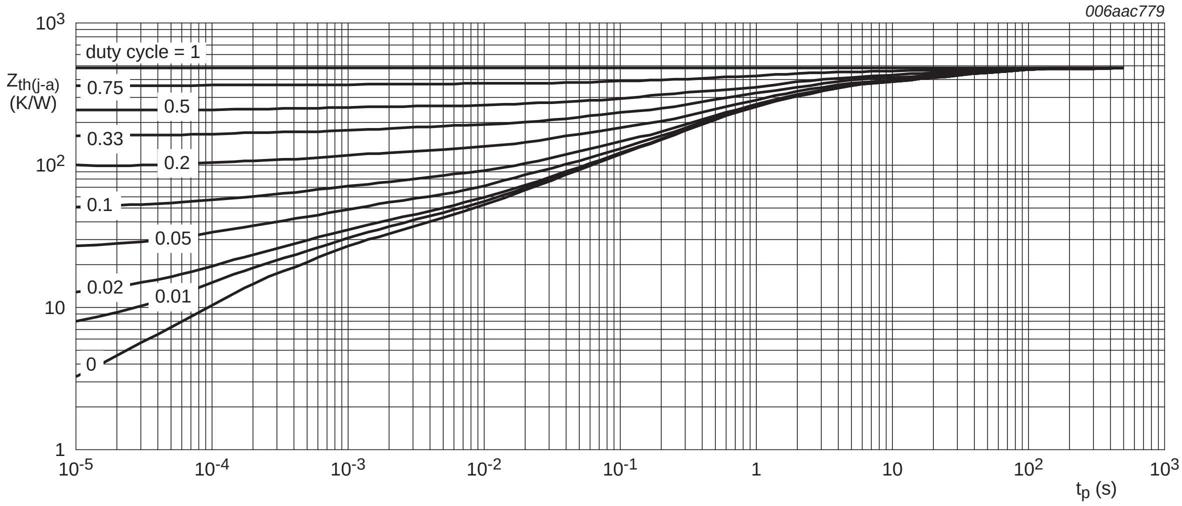

FR4 PCB, standard footprint

**Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114YE (SOT416); typical values**



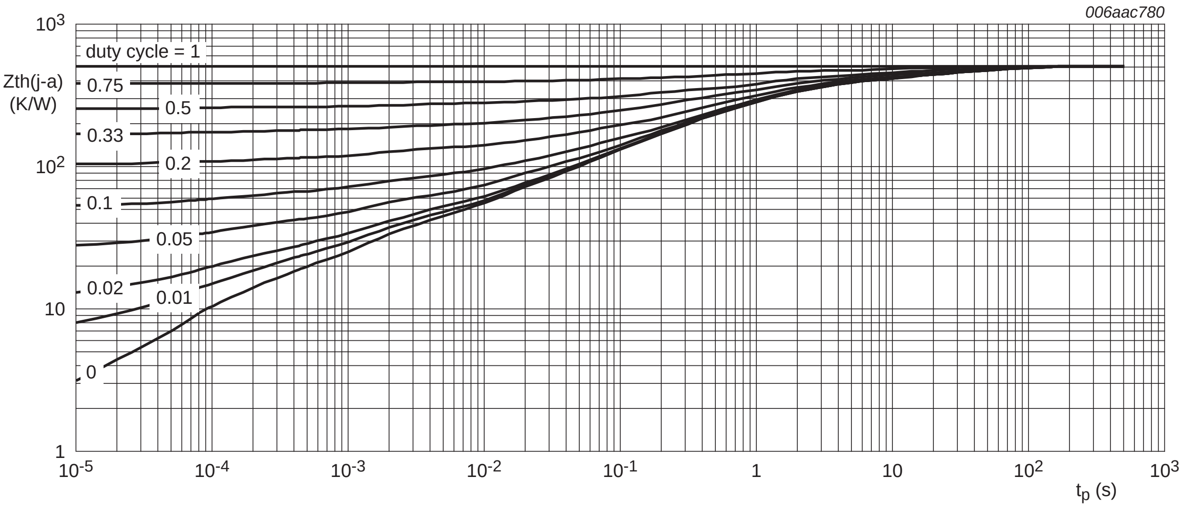

FR4 PCB, 70 μm copper strip line

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114YM (SOT883); typical values**




FR4 PCB, standard footprint

**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114YT (SOT23); typical values**




FR4 PCB, standard footprint

**Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114YU (SOT323); typical values**

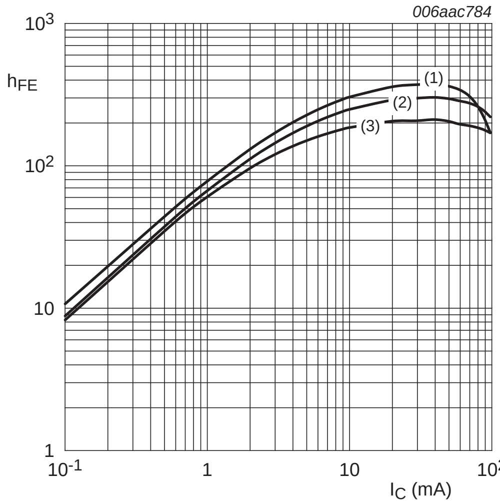
# 7. Characteristics

**Table 8. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 50 V; $I_E$ = 0 A | | - | - | 100 | nA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = 30 V; $I_B$ = 0 A | | - | - | 1 | µA |
| | | $V_{CE}$ = 30 V; $I_B$ = 0 A; $T_j$ = 150 °C | | - | - | 5 | µA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = 5 V; $I_C$ = 0 A | | - | - | 150 | µA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = 5 V; $I_C$ = 5 mA | | 100 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 5 mA; $I_B$ = 0.25 mA | | - | - | 100 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE}$ = 5 V; $I_C$ = 100 µA | | - | 0.7 | 0.5 | V |
| $V_{I(on)}$ | on-state input voltage | $V_{CE}$ = 0.3 V; $I_C$ = 1 mA | | 1.4 | 0.8 | - | V |
| R1 | bias resistor 1 (input) | | | 7 | 10 | 13 | kΩ |
| R2/R1 | bias resistor ratio | | | 3.7 | 4.7 | 5.7 | |
| $C_c$ | collector capacitance | $V_{CB}$ = 10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | | - | - | 2.5 | pF |
| $f_T$ | transition frequency | $V_{CE}$ = 5 V; $I_C$ = 10 mA; f = 100 MHz | [1] | - | 230 | - | MHz |

[1] Characteristics of built-in transistor



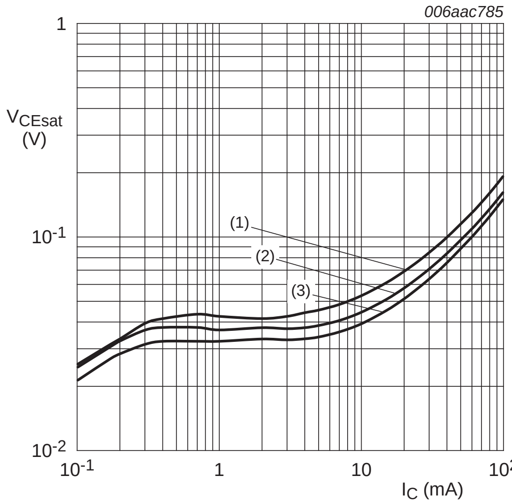

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 6. DC current gain as a function of collector current; typical values**



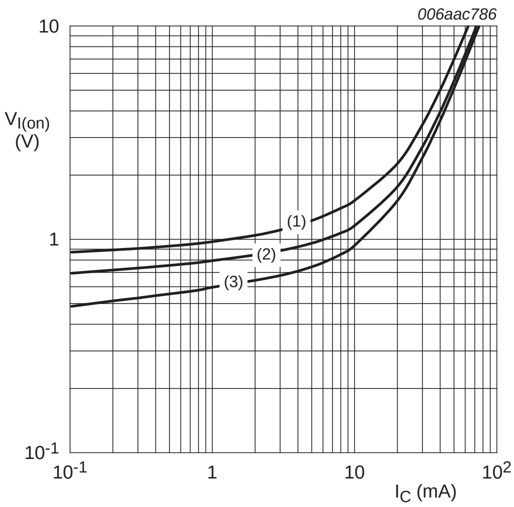

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −40 °C

**Fig 7. Collector-emitter saturation voltage as a function of collector current; typical values**



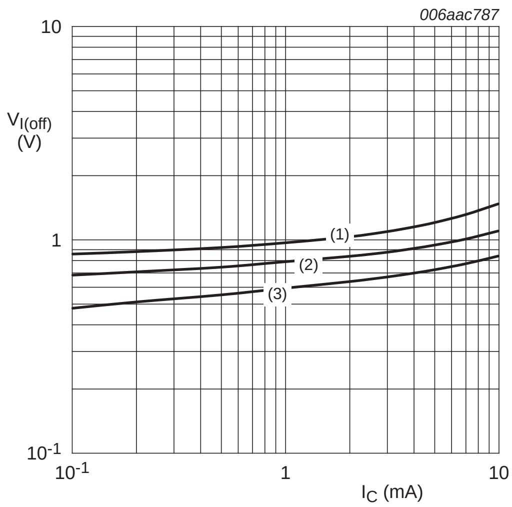

$V_{CE}$ = 0.3 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 8. On-state input voltage as a function of collector current; typical values**



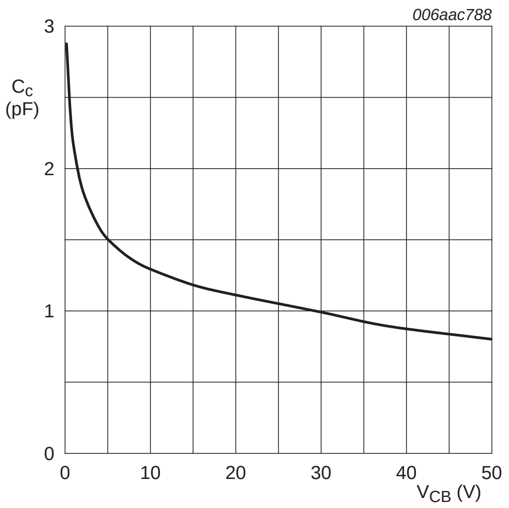

$V_{CE}$ = 5 V

(1) $T_{amb}$ = −40 °C

(2) $T_{amb}$ = 25 °C

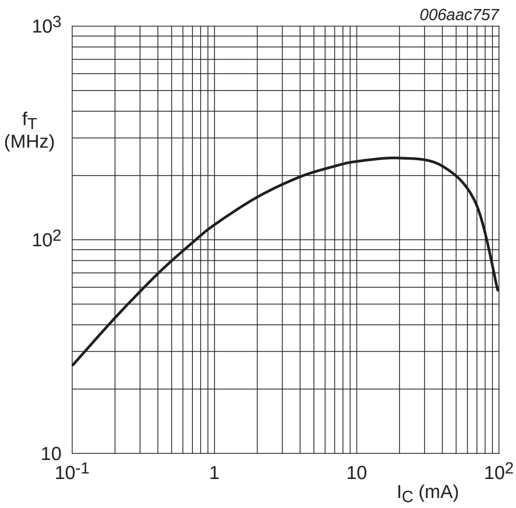
(3) $T_{amb}$ = 100 °C

**Fig 9. Off-state input voltage as a function of collector current; typical values**




f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 10. Collector capacitance as a function of collector-base voltage; typical values**




$V_{CE}$ = 5 V; $T_{amb}$ = 25 °C

**Fig 11. Transition frequency as a function of collector current; typical values of built-in transistor**

# 8. Test information

## 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

# 9. Package outline

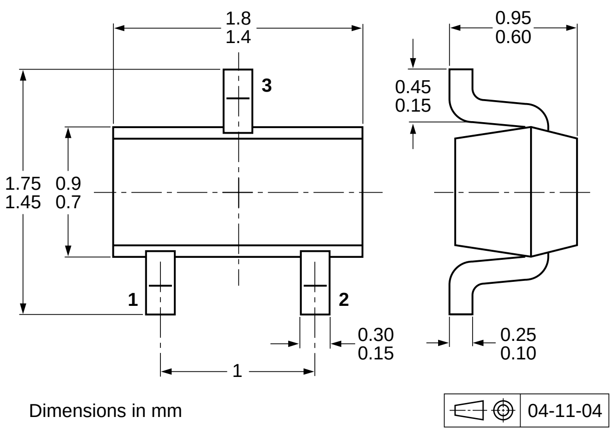



Fig 12. Package outline PDTC114YE (SOT416/SC-75)

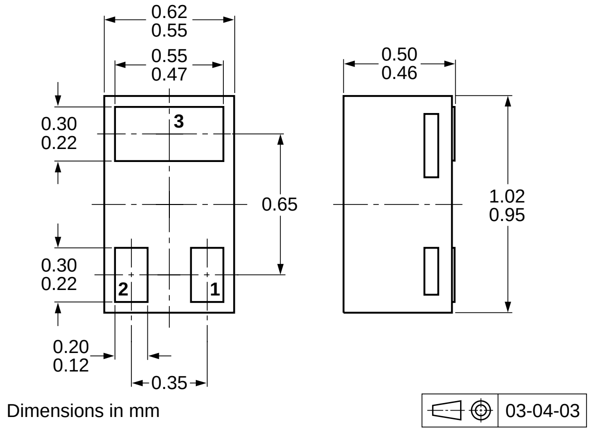



Fig 13. Package outline PDTC114YM (SOT883/SC-101)

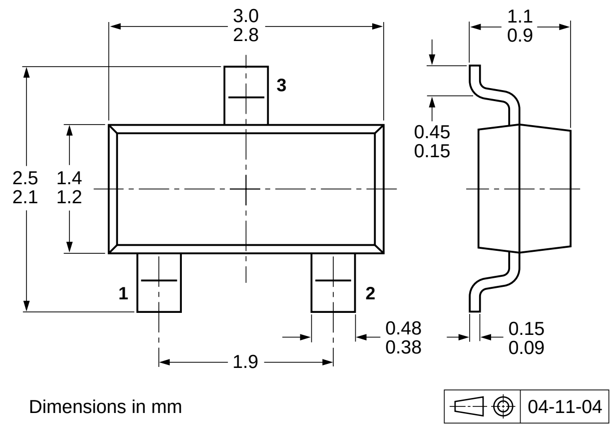



Fig 14. Package outline PDTC114YT (SOT23)

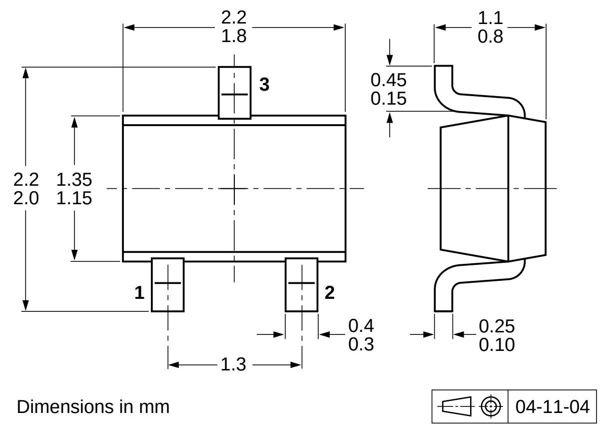



Fig 15. Package outline PDTC114YU (SOT323/SC-70)

## 10. Packing information

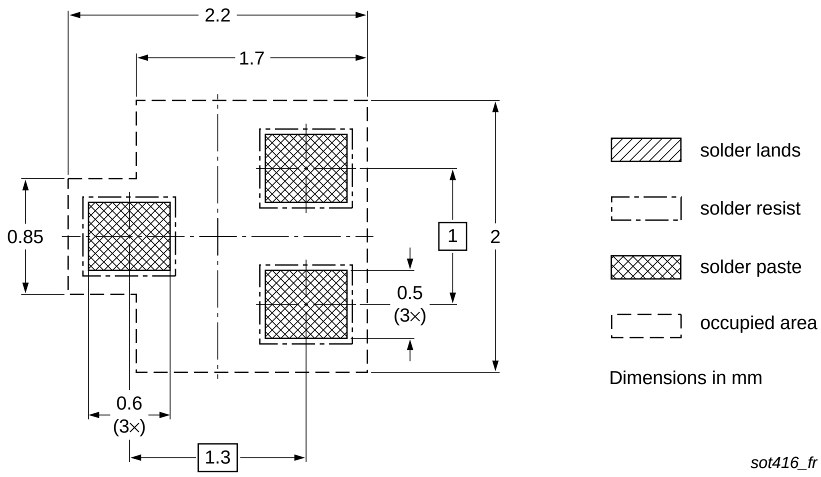
**Table 9. Packing methods**

*The indicated -xxx are the last three digits of the 12NC ordering code.*[1]

| Type number | Package | Description | Packing quantity | | |
|---|---|---|---|---|---|
| | | | 3000 | 5000 | 10000 |
| PDTC114YE | SOT416 | 4 mm pitch, 8 mm tape and reel | -115 | - | -135 |
| PDTC114YM | SOT883 | 2 mm pitch, 8 mm tape and reel | - | - | -315 |
| PDTC114YT | SOT23 | 4 mm pitch, 8 mm tape and reel | -215 | - | -235 |
| PDTC114YU | SOT323 | 4 mm pitch, 8 mm tape and reel | -115 | - | -135 |

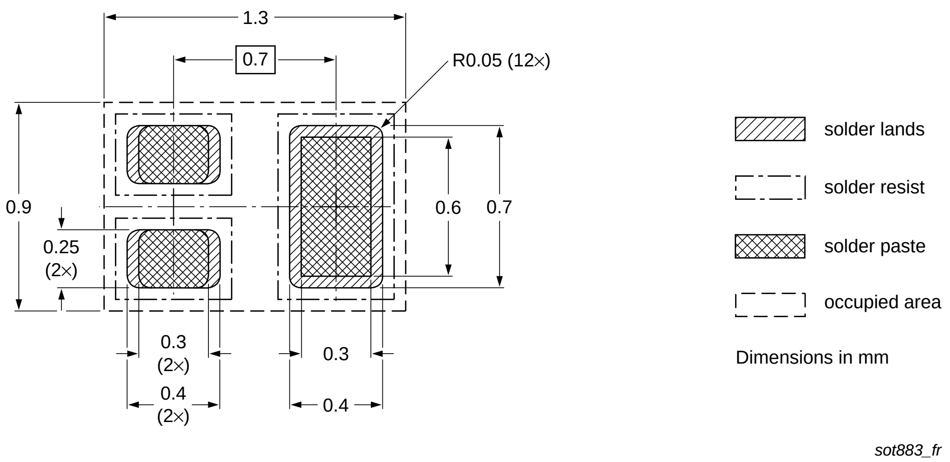
[1] For further information and the availability of packing methods, see Section 14.

## 11. Soldering




Reflow soldering is the only recommended soldering method.

**Fig 16. Reflow soldering footprint PDTC114YE (SOT416/SC-75)**




Reflow soldering is the only recommended soldering method.

**Fig 17. Reflow soldering footprint PDTC114YM (SOT883/SC-101)**

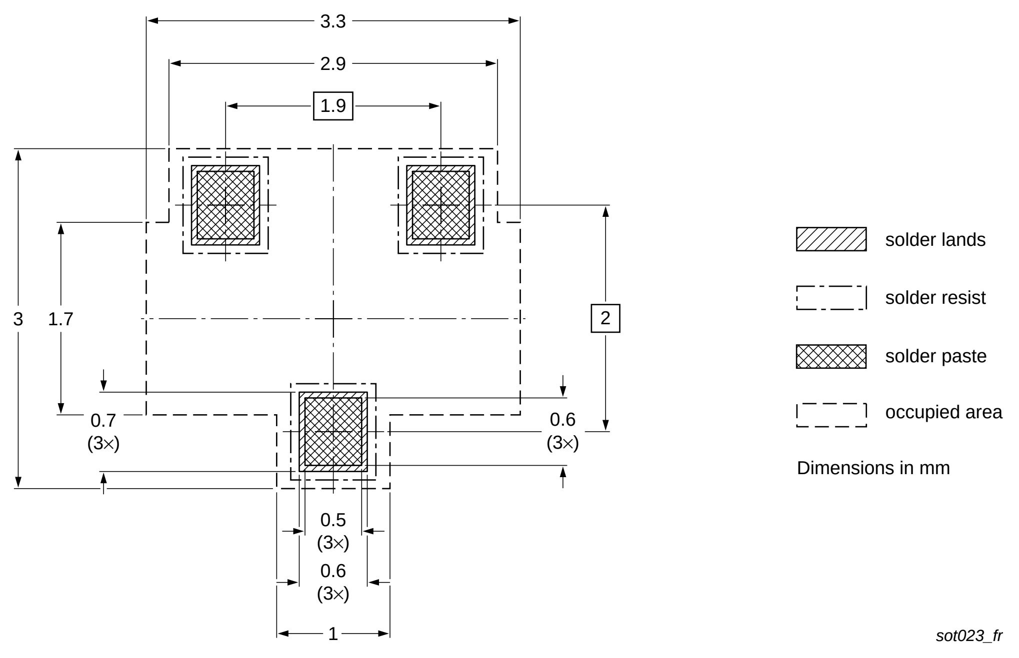



**Fig 18. Reflow soldering footprint PDTC114YT (SOT23)**

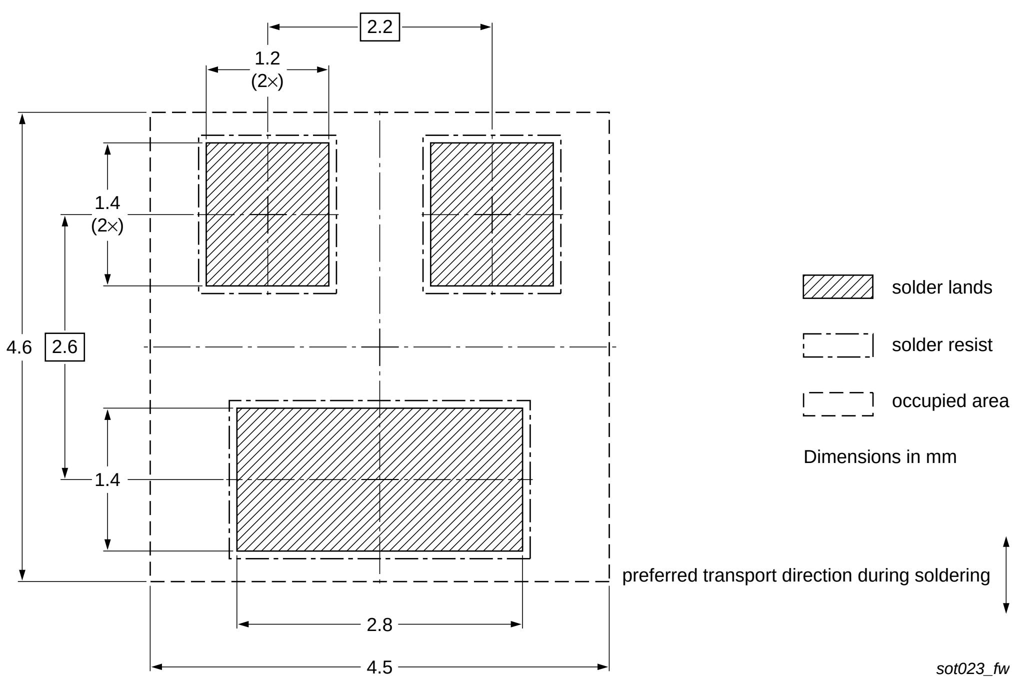



**Fig 19. Wave soldering footprint PDTC114YT (SOT23)**

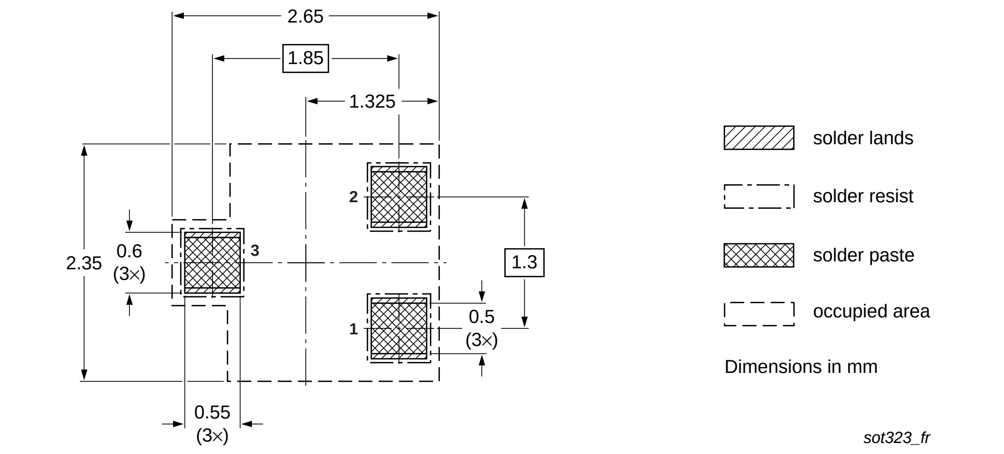



**Fig 20. Reflow soldering footprint PDTC114YU (SOT323/SC-70)**

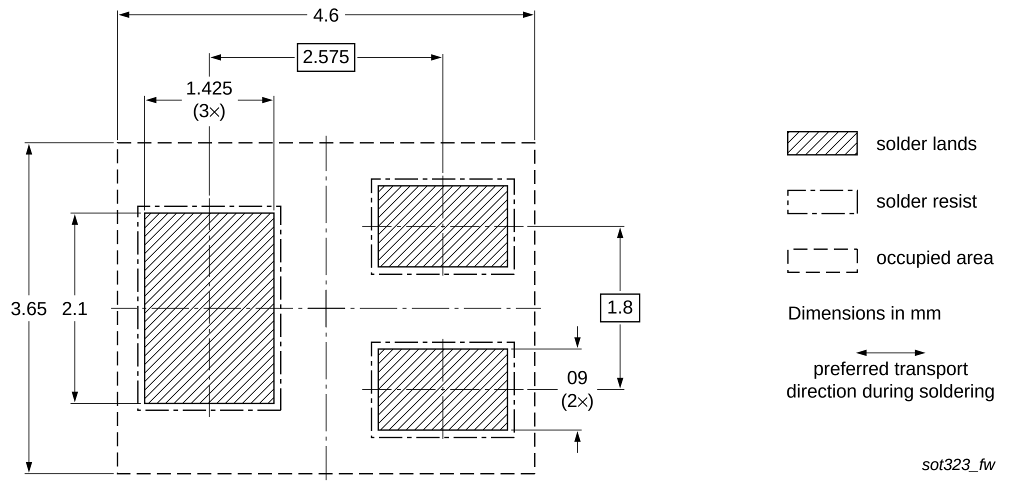



**Fig 21. Wave soldering footprint PDTC114YU (SOT323/SC-70)**

## 12. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PDTC114Y_SER v.7 | 20111118 | Product data sheet | - | PDTC114Y_SERIES v.6 |
| Modifications: | • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type numbers PDTC114YEF, PDTC114YK and PDTC114YS removed.<br>• Section 1 “Product profile”: updated<br>• Section 3 “Ordering information”: added<br>• Section 4 “Marking”: updated<br>• Figure 1 to 11: added<br>• Section 5 “Limiting values”: updated<br>• Section 6 “Thermal characteristics”: updated<br>• Table 8 “Characteristics”: $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, $I_{CEO}$ updated, $f_T$ added<br>• Section 8 “Test information”: added<br>• Section 9 “Package outline”: superseded by minimized package outline drawings<br>• Section 10 “Packing information”: added<br>• Section 11 “Soldering”: added<br>• Section 13 “Legal information”: updated | | | |
| PDTC114Y_SERIES v.6 | 20040817 | Product data sheet | - | PDTC114Y_SERIES v.5 |
| PDTC114Y_SERIES v.5 | 20040910 | Product specification | - | PDTC114Y_SERIES v.4 |
| PDTC114Y_SERIES v.4 | 20030414 | Product specification | - | - |

# 13. Legal information

## 13.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 15. Contents





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**Document identifier: PDTC114Y_SER**