

## 5V, 500mA low drop voltage regulator

Datasheet – production data

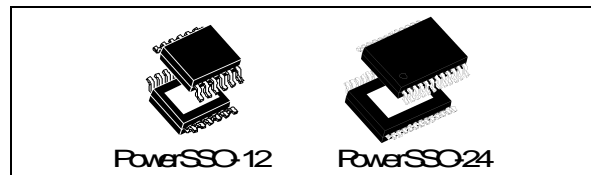
### Features

Max DC supply voltage	$V_S$	40V
Max output voltage tolerance	$\Delta V_0$	+/-2%
Max dropout voltage	$V_{dp}$	500mV
Output current	$I_0$	500mA
Quiescent current	$I_{qn}$	$3\mu A^{(1)}$

1. Typical value with regulator disabled

- Operating DC supply voltage range 5.6V to 31V
- Low dropout voltage
- Low quiescent current consumption
- Reset circuit sensing of output voltage down to 1 V
- Programmable reset pulse delay with external capacitor
- Programmable watchdog<sup>(a)</sup> timer with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range ( $T_j = -40\text{ °C}$  to  $150\text{ °C}$ )
- Enable<sup>(a)</sup> input for enabling/disabling the voltage regulator

a. Watchdog and Enable facilities are available according to Device summary table.



### Description

L4995 is a family of monolithic integrated 5 V voltage regulators with a low drop voltage at currents of up to 500 mA, available in both 12 and 24 pin packages.

The output voltage regulating element consists of a p-channel MOS and regulation is performed regardless of input voltage transients of up to 40V.

The high precision of the output voltage is obtained using a pre-trimmed reference voltage. The L4995 family is protected against short circuit and overtemperature protection switches off the devices in the case of extremely high power dissipation. The L4995 integrates the watchdog, enable and externally programmable reset circuits. The L4995A features the externally programmable reset and enable. Finally the L4995R features the externally programmable reset.

The combination of such features makes this device particularly flexible and suitable to supply microprocessor systems in automotive applications.

**Table 1. Device summary**

Package	Order codes		
	Tube		Tape and reel
PowerSSO-12 (exposed pad)	L4995J - L4995AJ - L4995RJ		L4995JTR - L4995AJTR - L4995RJTR
PowerSSO-24 (exposed pad)	L4995K - L4995AK - L4995RK		L4995KTR - L4995AKTR - L4995RKTR
P/N	Watchdog	Reset	Enable
L4995J - L4995K	X	X	X
L4995AJ - L4995AK	-	X	X
L4995RJ - L4995RK	-	X	-

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# 1 Block diagrams and pins descriptions

Figure 1. Block diagram of L4995

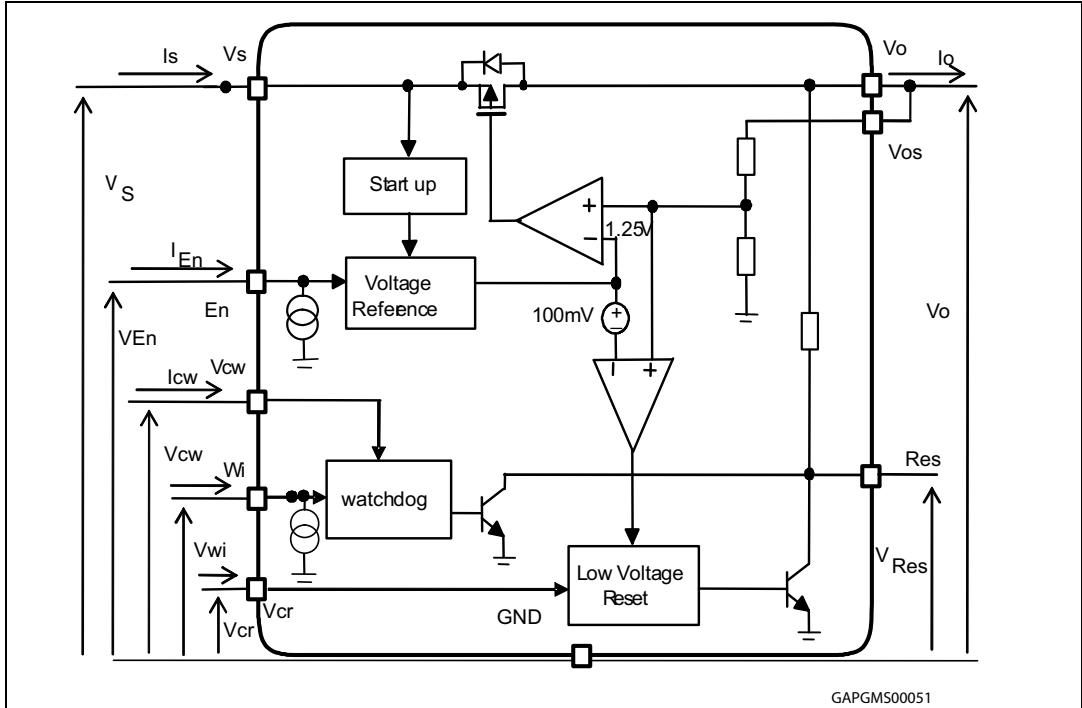


Figure 2. Block diagram of L4995A

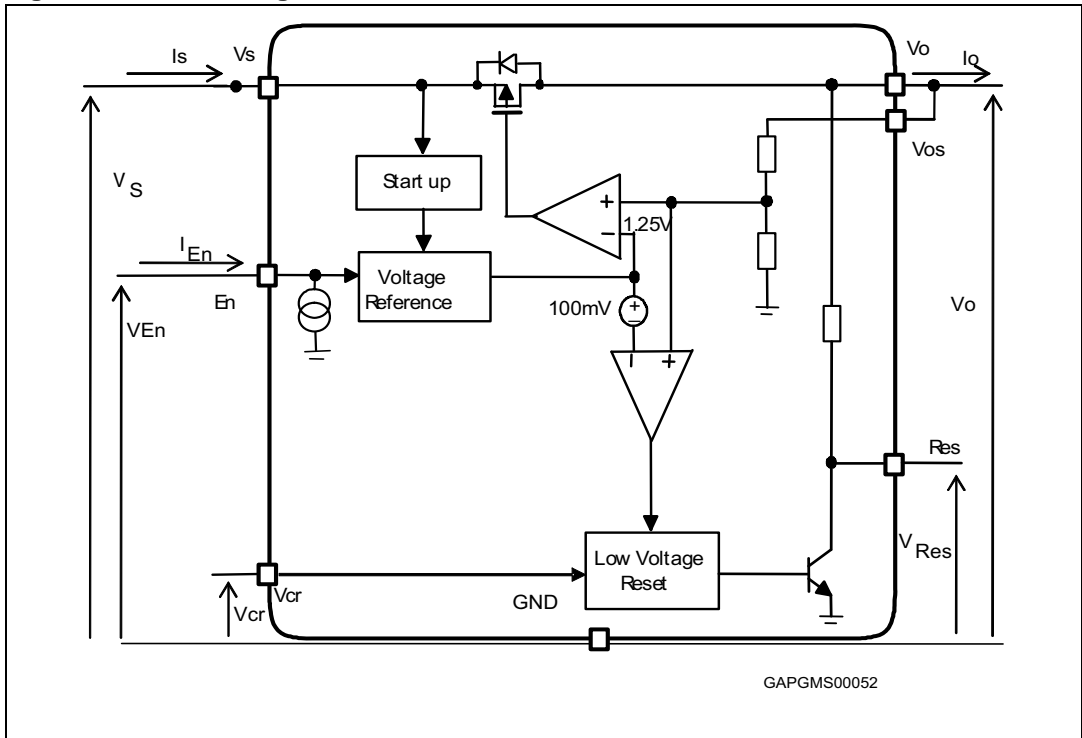


Figure 3. Block diagram of L4995R

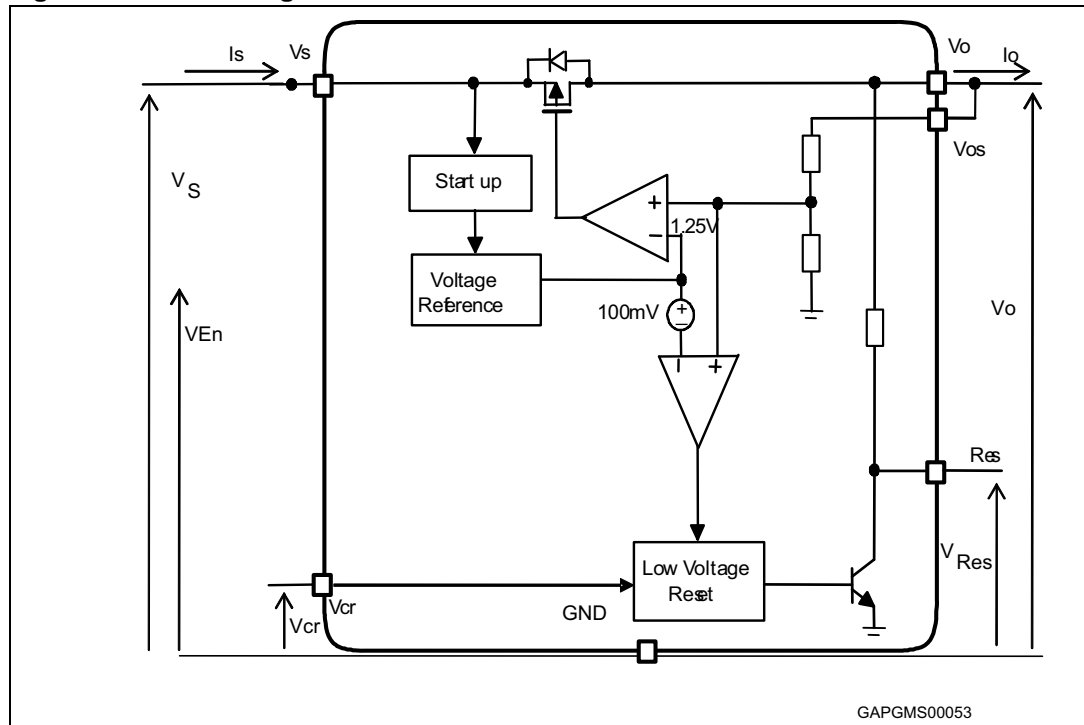


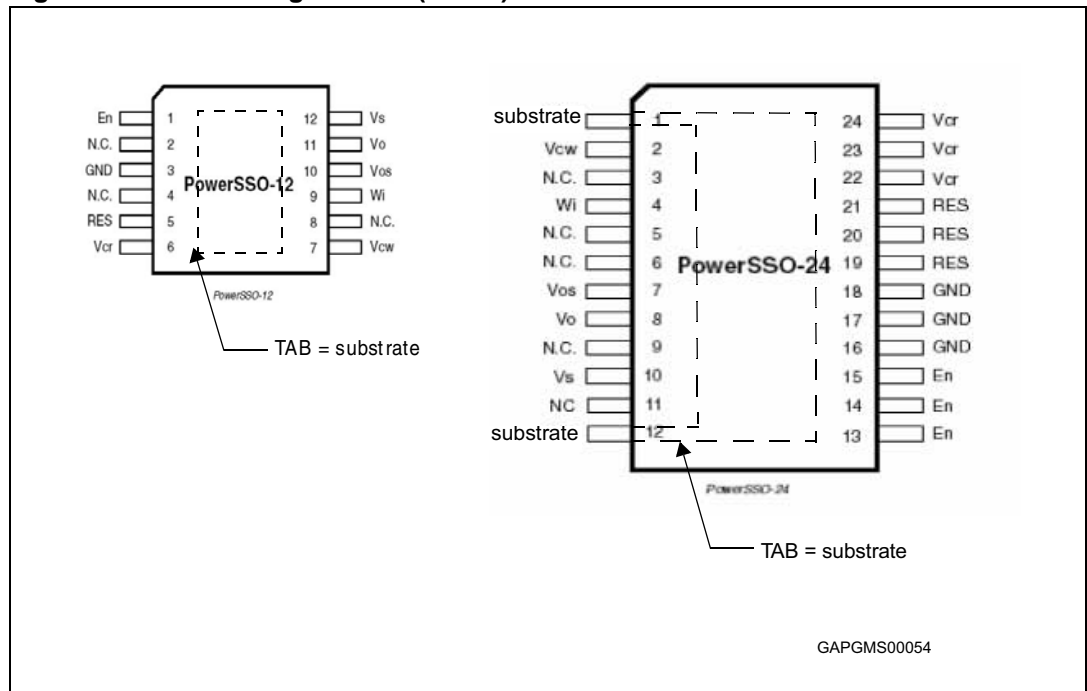
Table 2. Pins descriptions

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
$E_n$	1	13, 14, 15	Enable input (L4995 and L4996A only, otherwise not connected). If high regulator, watchdog and reset are operating. If low regulator, watchdog and reset are shutdown. Connect to $V_s$ if not used.
NC	2, 4, 8	3, 5, 6, 9, 11	Not connected.
GND	3	16, 17, 18	Ground reference.
-	TAB	TAB, 1, 12	Substrate of the chip: connect the pins or the TAB to GND.
$R_{es}$	5	19, 20, 21	Reset output. It is pulled down when output voltage goes below $V_{o\_th}$ or frequency at $W_i$ is too low. Leave floating if not used.
$V_{cr}$	6	22, 23, 24	Reset timing adjust. A capacitor between $V_{cr}$ pin and GND. Sets the reset delay time ( $t_{rd}$ ). Leave floating if Reset is not used.
$V_{cw}$	7	2	Watchdog timer adjust (L4995 only, otherwise not connected). A capacitor between $V_{cw}$ pin and GND. Sets the time response of the watchdog monitor.

Table 2. Pins descriptions (continued)

Pin name	PowerSSO-12 pin #	PowerSSO-24 pin #	Function
$W_i$	9	4	Watchdog input (L4995 only, otherwise not connected). If the frequency at this input pin is too low, the Reset output is activated.
$V_{os}$	10	7	Regulator voltage output sensing.
$V_o$	11	8	5 voltage regulator output. Block to ground with a capacitor >100nF (needed for regulator stability).
$V_S$	12	10	Supply voltage. Block to ground directly at $V_S$ pin with a ceramic capacitor (e.g. 200nF).

Figure 4. Pins configurations (L4995)



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{VsdC}$	DC supply voltage	- 0.3 to 40	V
$I_{VsdC}$	Input current	Internally limited	
$V_{Vo}^{(1)}$	DC output voltage	- 0.3 to 6	V
$I_{Vo}$	DC output current	Internally limited	
$V_{Wi}$	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
$V_{od}$	$R_{es}$ output voltage	-0.3 to $V_{Vo} + 0.3$	V
$I_{od}$	$R_{es}$ output current	Internally limited	
$V_{cr}$	$V_{cr}$ voltage	- 0.3 to $V_{Vo} + 0.3$	V
$V_{cw}$	Watchdog delay voltage	- 0.3 to $V_{Vo} + 0.3$	V
$V_{En}$	Enable input	- 0.3 to $V_{VsdC} + 0.3$	V
$T_j$	Junction temperature	- 40 to 150	C
$V_{ESD}$	ESD voltage level (HBM-MIL STD 883C)	$\pm 2$	kV
$V_{ESD}$	ESD voltage level (CDM AEC-Q100-011)	750	V

1. Using the typical application schematic with  $C_{out} = 10 \mu F$  and  $I_{out} = 0 A$ , when the regulator is switched-on, an overshoot exceeding 6 V could occur. This behavior does not impact the reliability of the regulator.



## 2.2 Thermal data

For details, please refer to [Section 4.1: PowerSSO-12 thermal data](#) and [Section 4.2: PowerSSO-24 thermal data](#).

**Table 4. Thermal data<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance Junction to Case:		
	PowerSSO-12	5	°K/W
	PowerSSO-24	4	°K/W
R <sub>thj-amb</sub>	Thermal resistance Junction to Ambient:		
	PowerSSO-12	52	°K/W
	PowerSSO-24	38	°K/W

1. The values quoted are for PCB 77mm x 86mm x 1.6mm, FR4, double layer; Copper thickness 0.070mm  
Copper area 3cm<sup>2</sup> Thermal Vias, Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm.

## 2.3 Electrical characteristics

Values specified in this section are for V<sub>S</sub> = 5.6V to 31V, T<sub>J</sub> = -40 °C to +150 °C unless otherwise stated.

**Table 5. General**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>o</sub>	V <sub>o_ref</sub>	Output voltage	V <sub>S</sub> = 5.6 to 31V I <sub>o</sub> = 0 to 500mA	4.9	5.00	5.1	V
V <sub>o</sub>	I <sub>short</sub>	Short circuit current	V <sub>S</sub> = 13.5V <sup>(1)</sup>	550	800	1050	mA
V <sub>o</sub>	I <sub>lim</sub> <sup>(2)</sup>	Output current limitation	V <sub>S</sub> = 13.5V <sup>(1)</sup>	600	900	1250	mA
V <sub>S</sub> , V <sub>o</sub>	V <sub>line</sub>	Line regulation voltage	V <sub>S</sub> = 5.6 to 31V I <sub>o</sub> = 0 to 500mA			25	mV
V <sub>o</sub>	V <sub>load</sub>	Load regulation voltage	I <sub>o</sub> = 0 to 500mA			25	mV
V <sub>S</sub> , V <sub>o</sub>	V <sub>dp</sub> <sup>(3)</sup>	Drop voltage	I <sub>o</sub> = 400mA		270	500	mV
V <sub>S</sub> , V <sub>o</sub>	SVR	Ripple rejection	f <sub>r</sub> = 100 Hz <sup>(4)</sup>	55			dB
V <sub>S</sub> , V <sub>o</sub>	I <sub>qs</sub>	Current consumption with regulator disabled	V <sub>S</sub> = 13.5V, E <sub>n</sub> = low		3	10	μA
V <sub>S</sub> , V <sub>o</sub>	I <sub>qn_1</sub>	Current consumption with regulator enabled	V <sub>S</sub> = 13.5V, I <sub>o</sub> < 1mA,		90	160	μA
V <sub>S</sub> , V <sub>o</sub>	I <sub>qn_50</sub>	Current consumption with regulator enabled	V <sub>S</sub> = 13.5V, I <sub>o</sub> = 50mA,		290	400	μA

**Table 5. General (continued)**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_S, V_O$	$I_{qn\_150}$	Current consumption with regulator enabled	$V_S = 13.5V,$ $I_O = 150mA,$		740	1000	$\mu A$
$V_S, V_O$	$I_{qn\_250}$	Current consumption with regulator enabled	$V_S = 13.5V,$ $I_O = 250mA,$		1	1.4	mA
$V_S, V_O$	$I_{qn\_500}$	Current consumption with regulator enabled	$V_S = 13.5V,$ $I_O = 500mA,$		2.1	2.7	mA
	$T_w$	Thermal protection temperature		150		190	$^{\circ}C$
	$T_{w\_hy}$	Thermal protection temperature hysteresis			10		$^{\circ}C$

1. See [Figure 28](#).
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at  $V_S=13.5V$  and  $I_O= 250mA$ .
3.  $V_S-V_O$  measured when the output voltage has dropped 100mV from its nominal value obtained at  $V_S=13.5V$  and  $I_O= 250mA$ .
4. Guaranteed by design.

**Table 6. Reset**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{es}$	$V_{res\_l}$	Reset output low voltage	$R_{ext} = 5k\Omega$ to $V_O,$ $V_O > 1V$			0.4	V
$R_{es}$	$I_{Res\_lkg}$	Reset output high leakage current	$V_{Res} = 5V$			1	$\mu A$
$R_{es}$	$R_{Res}$	Pull up internal resistance (versus $V_O$ )		10	20	40	$k\Omega$
$R_{es}$	$V_{o\_th}$	$V_O$ out of regulation threshold	$V_S = 5.6$ to $31V$ $I_O = 1$ to $500mA$	6%	8%	10%	below $V_{o\_ref}$
$V_{cr}$	$V_{Rlth}$	Reset delay circuit low threshold	$V_S = 13.5V$	10%	13%	16%	$V_{o\_ref}$
$V_{cr}$	$V_{Rhth}$	Reset delay circuit high threshold	$V_S = 13.5V$	44%	47%	50%	$V_{o\_ref}$
$V_{cr}$	$I_{cr}$	Charge current	$V_S = 13.5V$	8	15	30	$\mu A$
$V_{cr}$	$I_{dr}$	Discharge current	$V_S = 13.5V$	8	15	30	$\mu A$
$R_{es}$	$T_{rr}$	Reset reaction time <sup>(1)</sup>	$V_O = V_{o\_th} - 100mV$	100	250	700	$\mu s$
$R_{es}$	$T_{rd}$	Reset delay time	$V_S = 13.5V,$ $C_{tr} = 47nF$	12	33	73	ms

1. When  $V_O$  becomes lower than 4V, the reset reaction time decreases down to  $2\mu s$  assuring a faster reset condition in this particular case.

**Table 7. Watchdog**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
W <sub>i</sub>	V <sub>ih</sub>	Input high voltage	V <sub>S</sub> = 13.5V	3.5			V
W <sub>i</sub>	V <sub>il</sub>	Input low voltage	V <sub>S</sub> = 13.5V			1.5	V
W <sub>i</sub>	V <sub>ih</sub>	Input hysteresis	V <sub>S</sub> = 13.5V		500		mV
W <sub>i</sub>	I <sub>wi</sub>	Pull down current	V <sub>S</sub> = 13.5V V <sub>wi</sub> = 3.5V		6	10	μA
V <sub>cw</sub>	V <sub>wlth</sub>	Low threshold	V <sub>S</sub> = 13.5V	10%	13%	16%	V <sub>o_ref</sub>
V <sub>cw</sub>	V <sub>wlth</sub>	High threshold	V <sub>S</sub> = 13.5V	44%	47%	50%	V <sub>o_ref</sub>
V <sub>cw</sub>	I <sub>cwc</sub>	Charge current	V <sub>S</sub> = 13.5V, V <sub>cw</sub> = 0.1V	5	10	20	μA
V <sub>cw</sub>	I <sub>cwd</sub>	Discharge current	V <sub>S</sub> = 13.5V, V <sub>cw</sub> = 2.5V	1.25	2.5	5	μA
V <sub>cw</sub>	T <sub>wop</sub>	Watchdog period	V <sub>S</sub> = 13.5V, C <sub>tw</sub> = 47nF	20	40	80	ms
R <sub>es</sub>	t <sub>wol</sub>	Watchdog output low time	V <sub>S</sub> = 13.5V, C <sub>tw</sub> = 47nF	4	8	16	ms

**Table 8. Enable**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E <sub>n</sub>	V <sub>En_low</sub>	E <sub>n</sub> input low voltage				1	V
E <sub>n</sub>	V <sub>En_high</sub>	E <sub>n</sub> input high voltage		3			V
E <sub>n</sub>	V <sub>En_hyst</sub>	E <sub>n</sub> input hysteresis			830		mV
E <sub>n</sub>	I <sub>En</sub>	Pull down current	V <sub>S</sub> = 13.5V		10	18	μA

## 2.4 Electrical characteristics curves

Figure 5. Output voltage vs  $T_j$

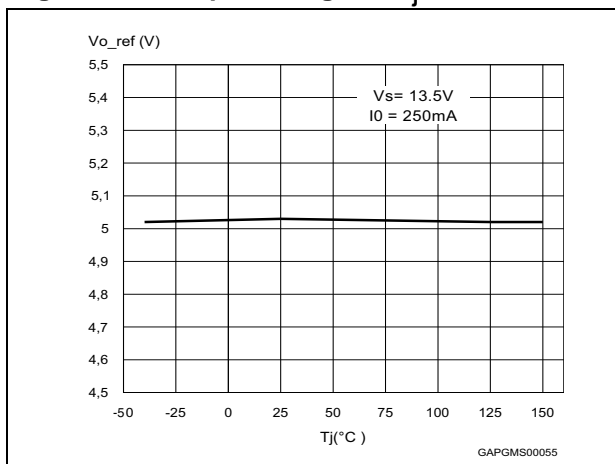


Figure 7. Drop voltage vs output current

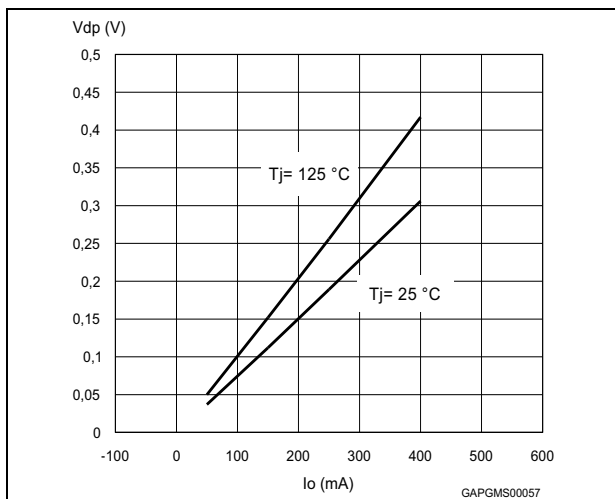


Figure 9. Current consumption vs input voltage

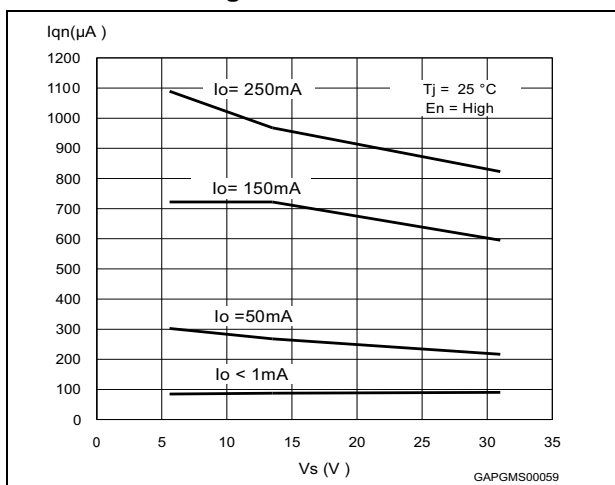


Figure 6. Output voltage vs  $V_s$

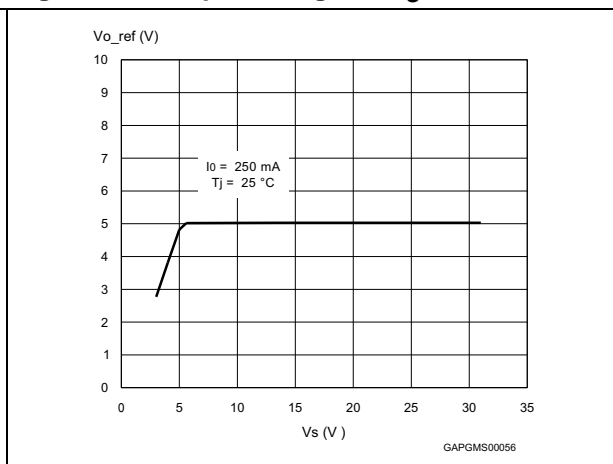


Figure 8. Current consumption vs output current

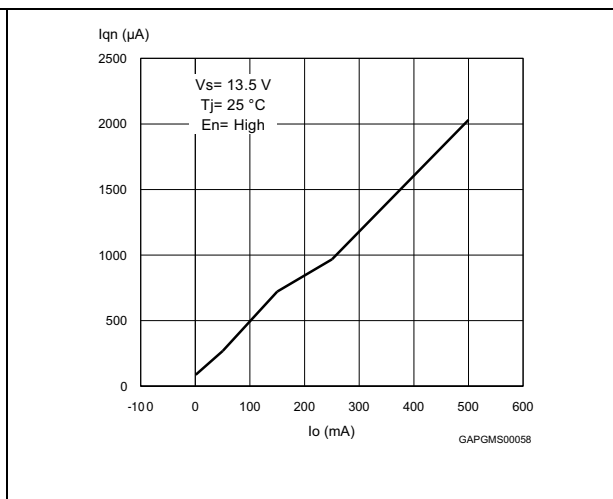


Figure 10. Current limitation vs  $T_j$

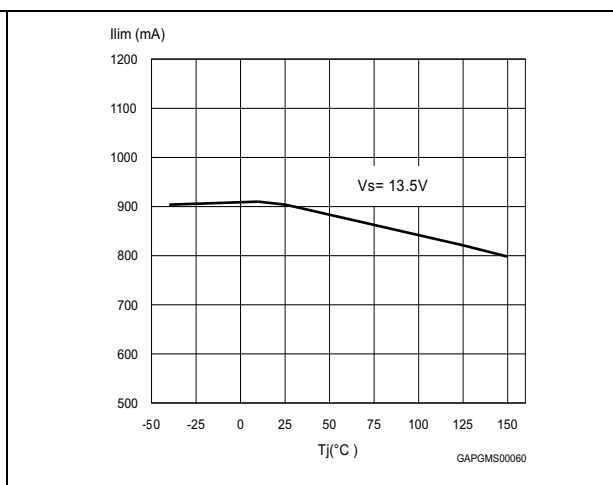


Figure 11. Current limitation vs input voltage

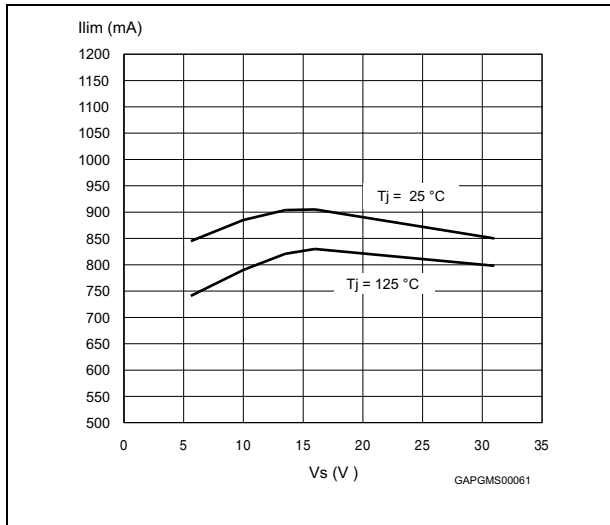


Figure 12. Short circuit current vs input voltage

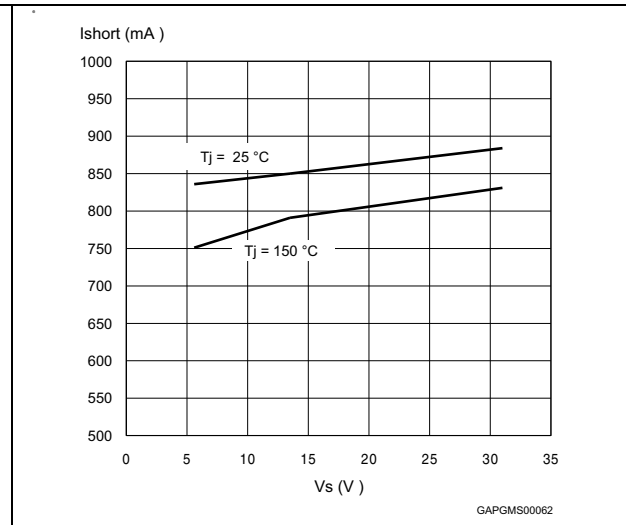


Figure 13. Output voltage vs enable voltage

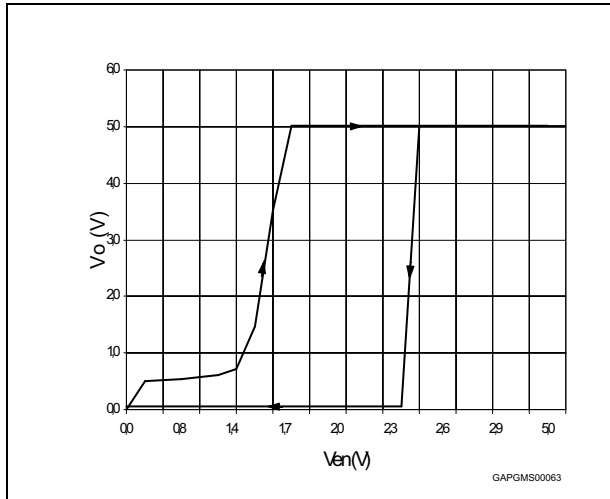


Figure 14. V<sub>En\_high</sub> vs T<sub>j</sub>

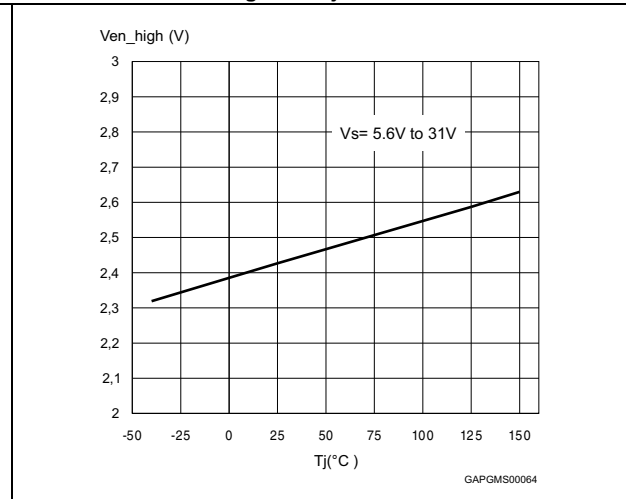


Figure 15. V<sub>EN\_LOW</sub> vs T<sub>j</sub>

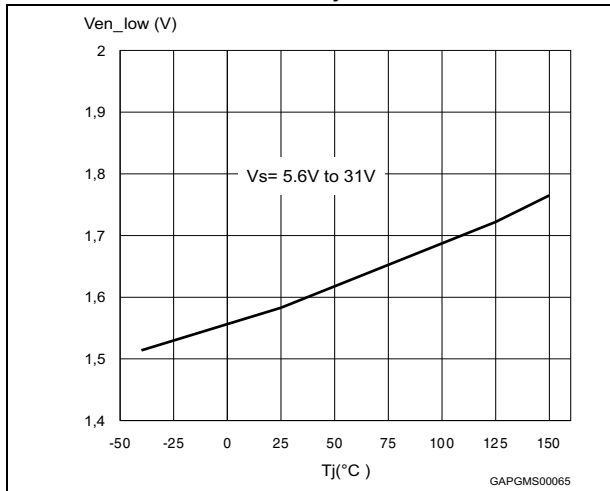


Figure 16. V<sub>Rhth</sub> vs T<sub>j</sub>

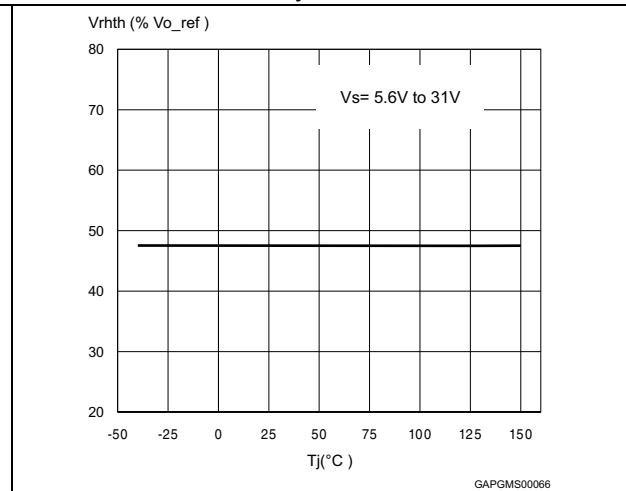


Figure 17.  $V_{Rlth}$  vs  $T_j$

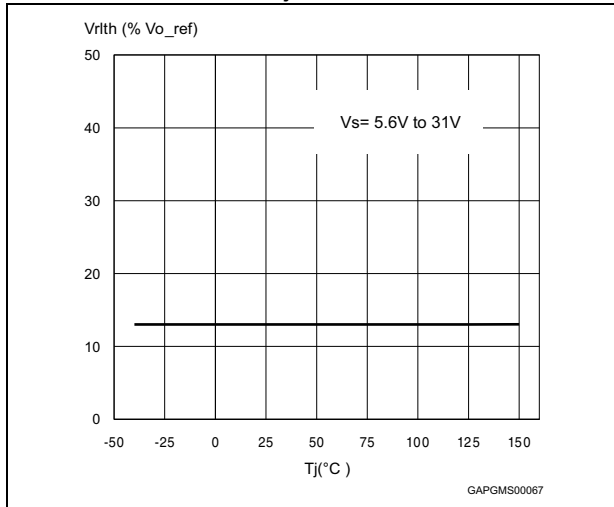


Figure 18.  $V_{whth}$  vs  $T_j$

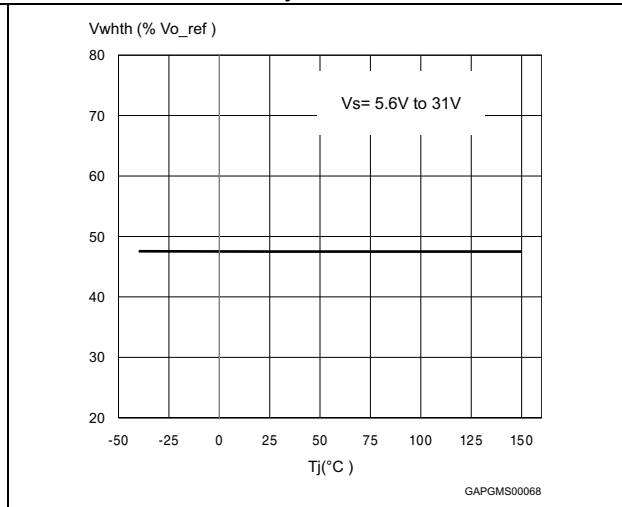


Figure 19.  $V_{wlth}$  vs  $T_j$

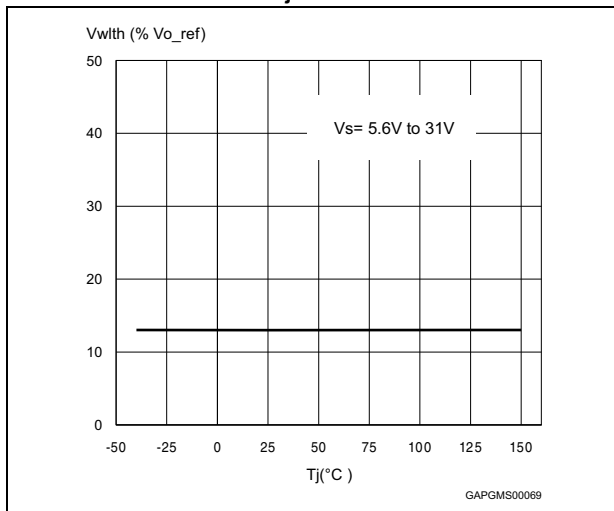


Figure 20.  $I_{cr}$  and  $I_{cwc}$  vs  $T_j$

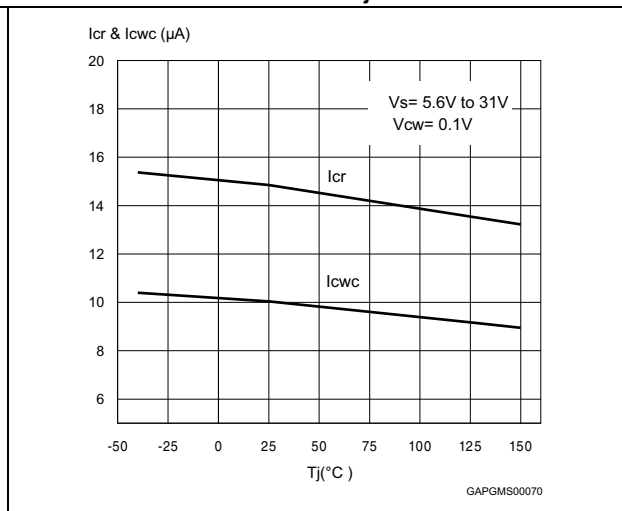


Figure 21.  $I_{dr}$  and  $I_{cwd}$  vs  $T_j$

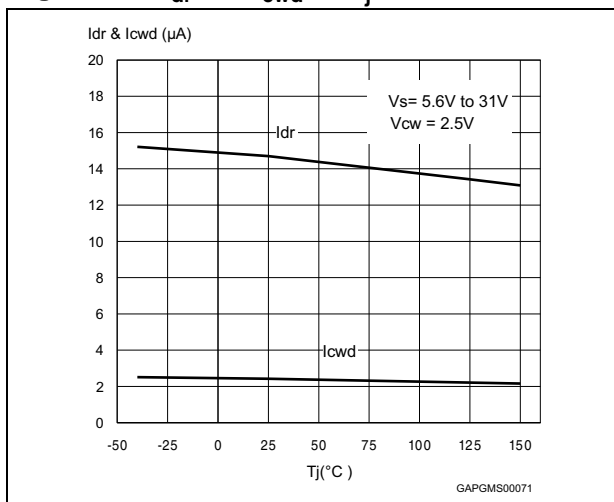


Figure 22.  $T_{wop}$  vs  $T_j$

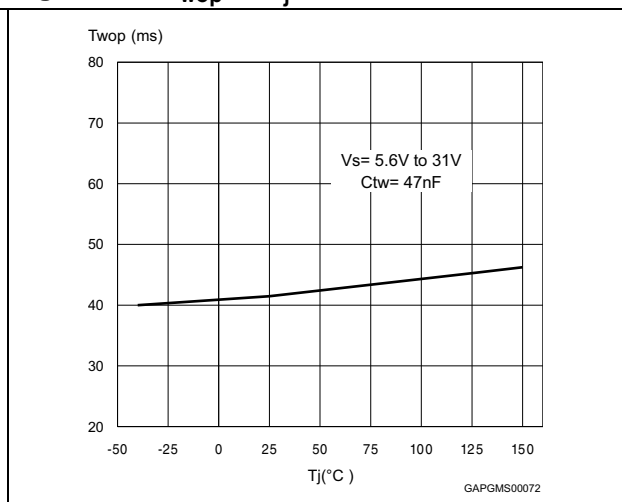
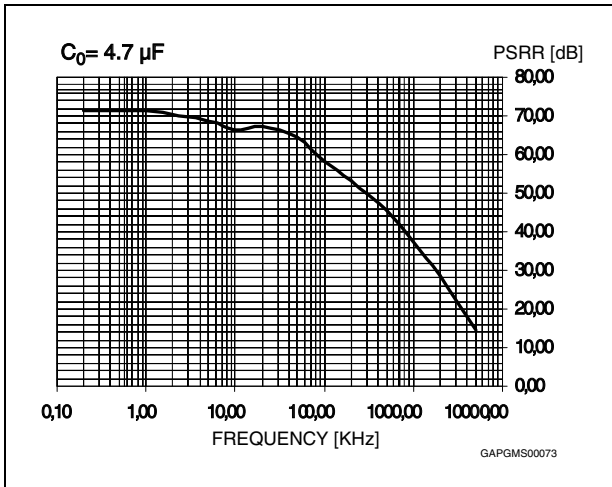


Figure 23. PSRR



## 2.5 Test circuit and waveforms plot

### 2.5.1 Load regulation

Figure 24. Load regulation test circuit

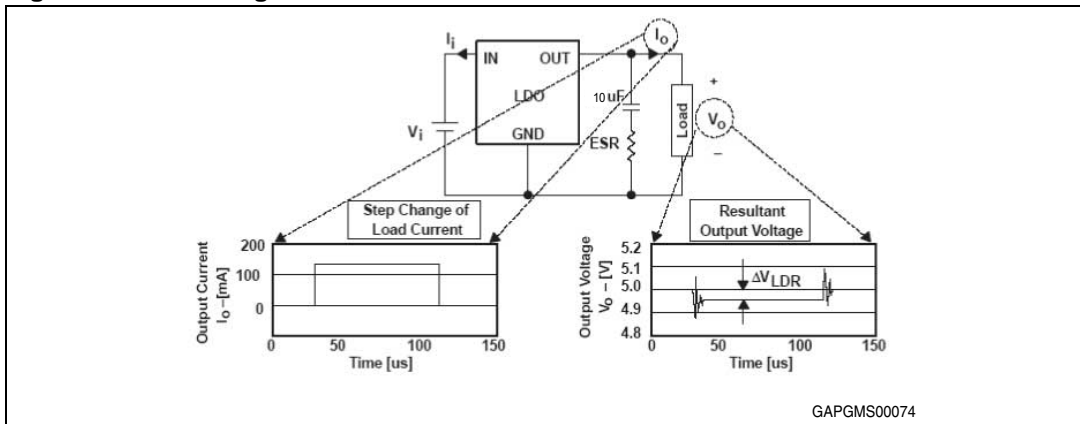
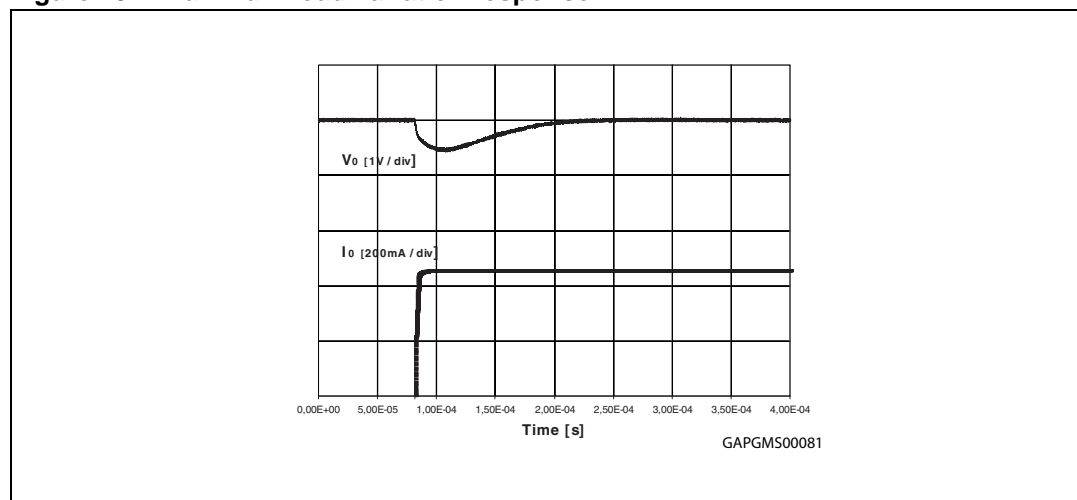


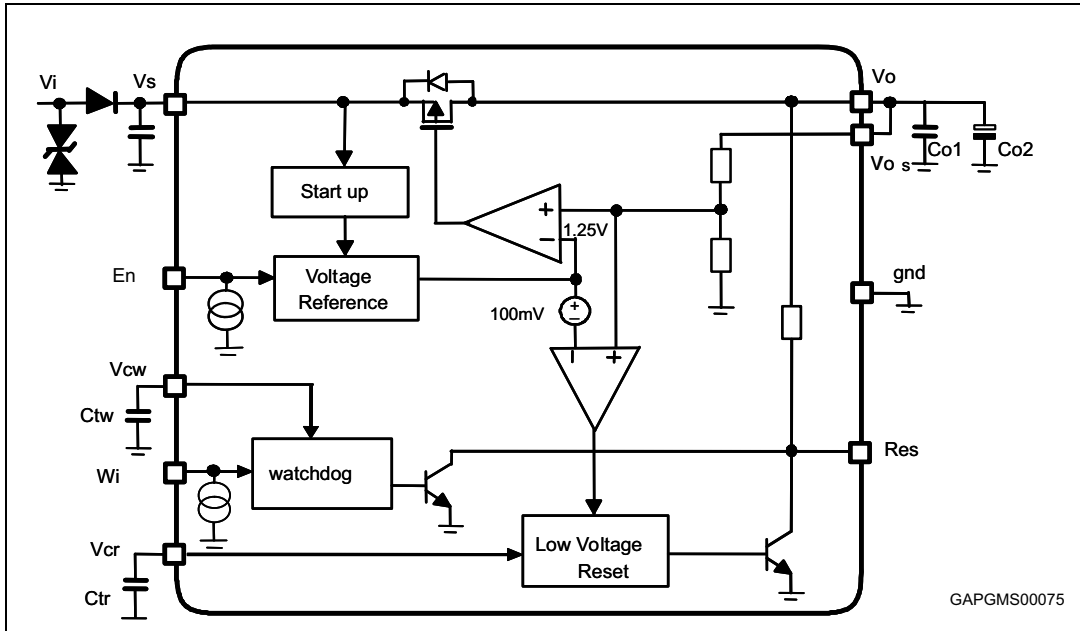
Figure 25. Maximum load variation response





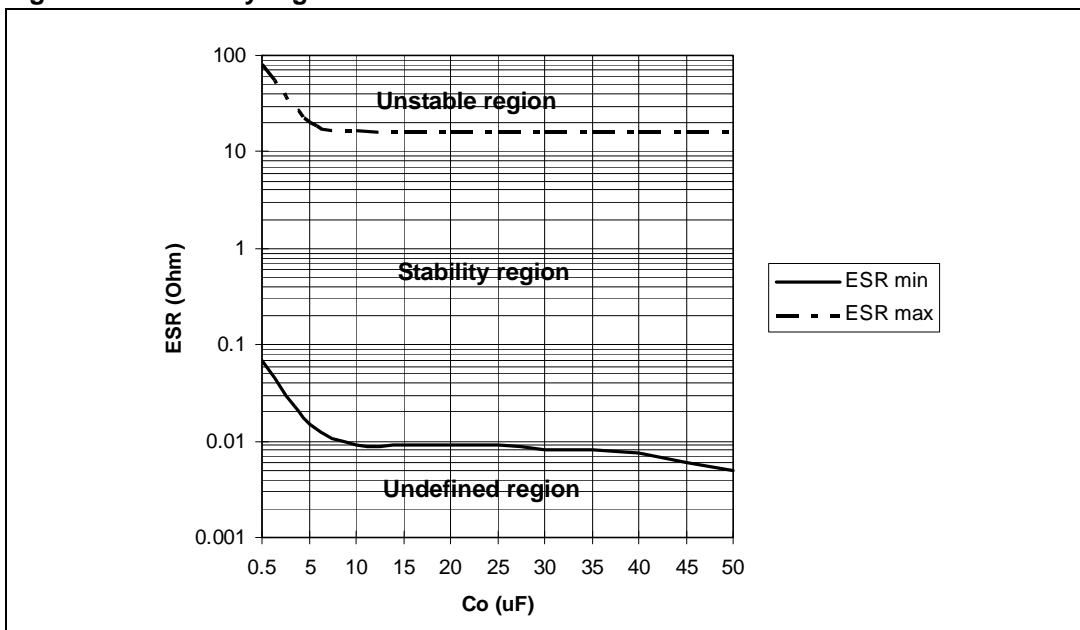
### 3 Application information

Figure 26. L4995 application schematic<sup>(1)</sup>



1. The input capacitor  $C_s > 200\text{nF}$  is necessary for the smoothing of line disturbances. The output capacitor  $C_{O1} > 100\text{nF}$  is necessary for the stability of the regulation loop. In order to dampen output voltage oscillations during high load current surges, it is recommended an additional electrolytic capacitor  $C_{O2} > 10\mu\text{F}$  to be placed at the output pin.

Figure 27. Stability region<sup>(1)</sup>



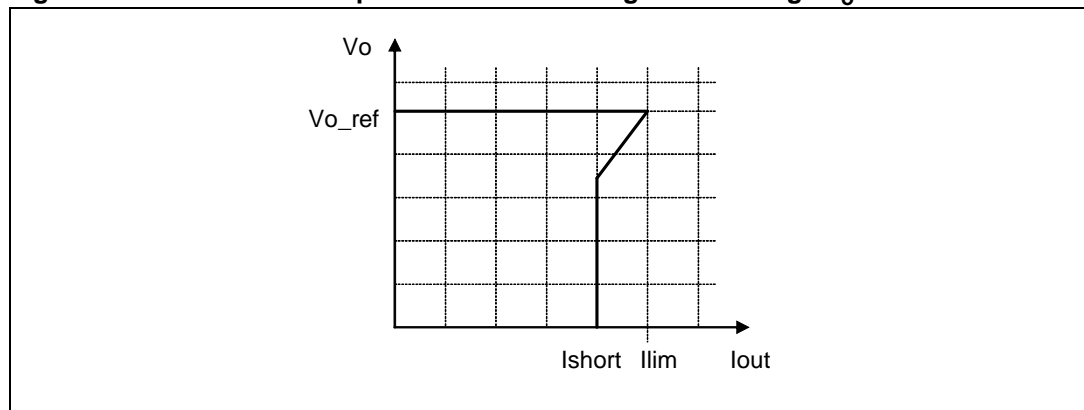
1. The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

### 3.1 Voltage regulator

Voltage regulator uses a p-channel transistor as a regulating element. With this structure, very low dropout voltage at current up to 500mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided.

The voltage regulator is active when  $E_n$  is high.

**Figure 28. Behavior of output current versus regulated voltage  $V_o$**



### 3.2 Reset

The reset circuit supervises the output voltage  $V_o$ . The  $V_{o\_th}$  reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than  $V_{o\_th}$  then  $R_{es}$  goes low with a reaction time  $t_{rr}$ . The reset low signal is guaranteed for an output voltage  $V_o$  greater than 1V.

When the output voltage becomes higher than  $V_{o\_th}$  then  $R_{es}$  goes high with a delay  $t_{rd}$ . This delay is obtained by an internal oscillator.

The oscillator period is given by:

**Equation 1**

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

$I_{cr}$ : is an internally generated charge current

$I_{dr}$ : is an internally generated discharge current

$V_{Rhth}$ ,  $V_{Rlth}$ : are two voltages defined with the output voltage and a resistor output divider

$C_{tr}$ : is an external capacitance.

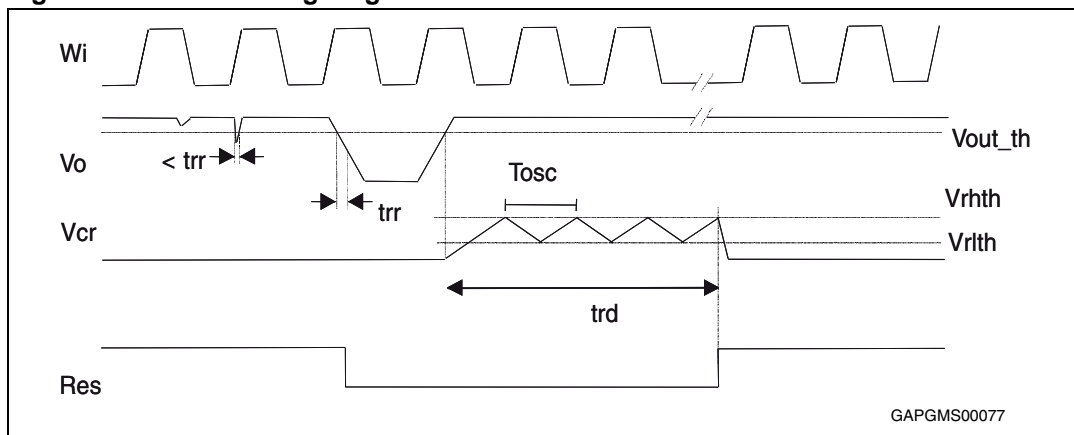
$t_{rd}$  is given by:

**Equation 2**

$$t_{rd} = (V_{Rhth} \times C_{tr}) / I_{cr} + 3 \times T_{osc}$$

Reset is active when  $E_n$  is high.

**Figure 29. Reset timing diagram**



### 3.3 Watchdog

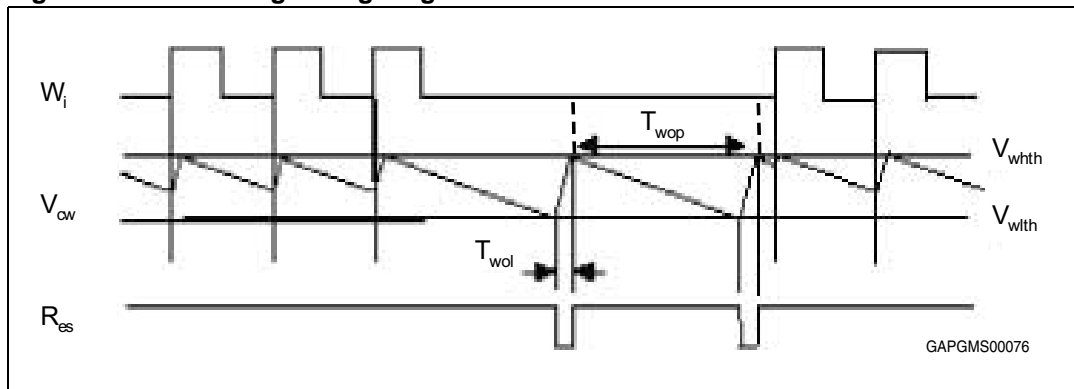
A connected microcontroller is monitored by the watchdog input  $W_i$ . If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor,  $C_{tw}$ . The watchdog circuit discharges the capacitor  $C_{tw}$ , with the constant current  $I_{cwd}$ . If the lower threshold  $V_{wlth}$  is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold  $V_{wlth}$ . In order to calculate the minimum time  $t$ , during which the micro-controller must output the positive edge, the following equation can be used:

**Equation 3**

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every  $W_i$  positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold,  $V_{whth}$ , the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor  $C_{tw}$ .

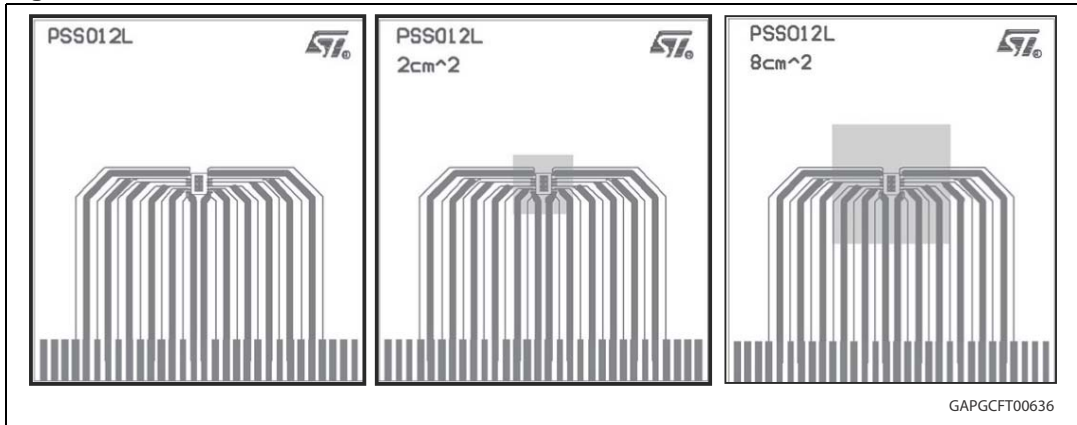
**Figure 30. Watchdog timing diagram**



## 4 Package and PCB thermal data

### 4.1 PowerSSO-12 thermal data

Figure 31. PowerSSO-12 PC board<sup>(1)</sup>



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 $\mu$ m (front and back side) Thermal vias separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 32.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

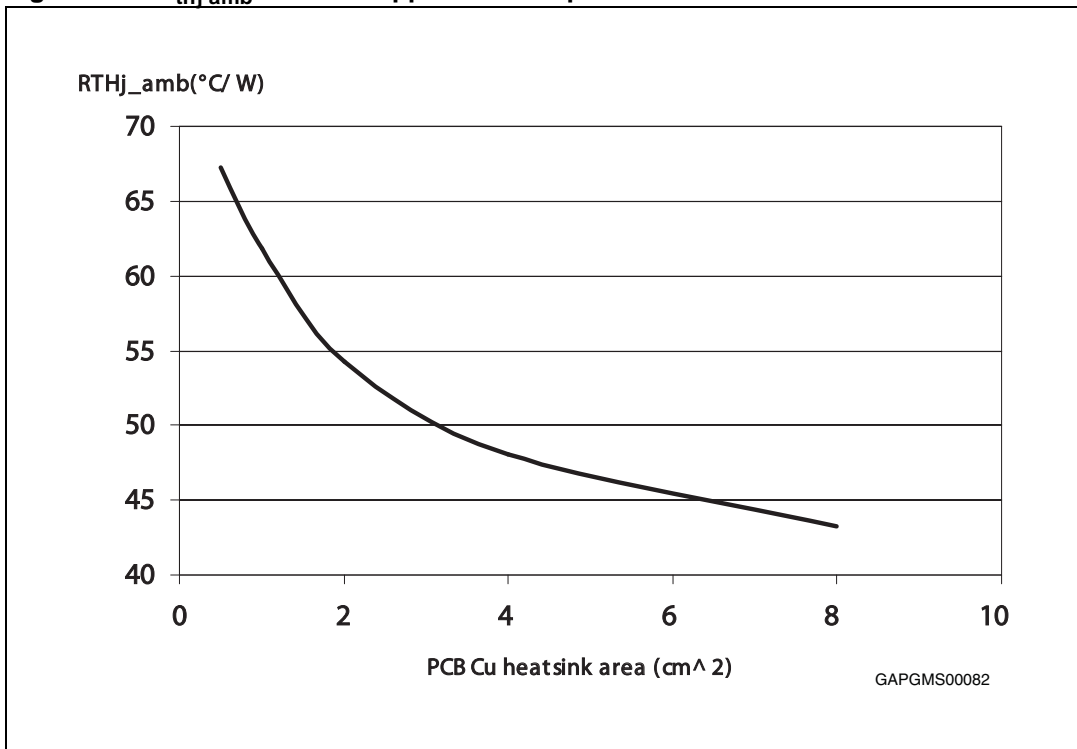
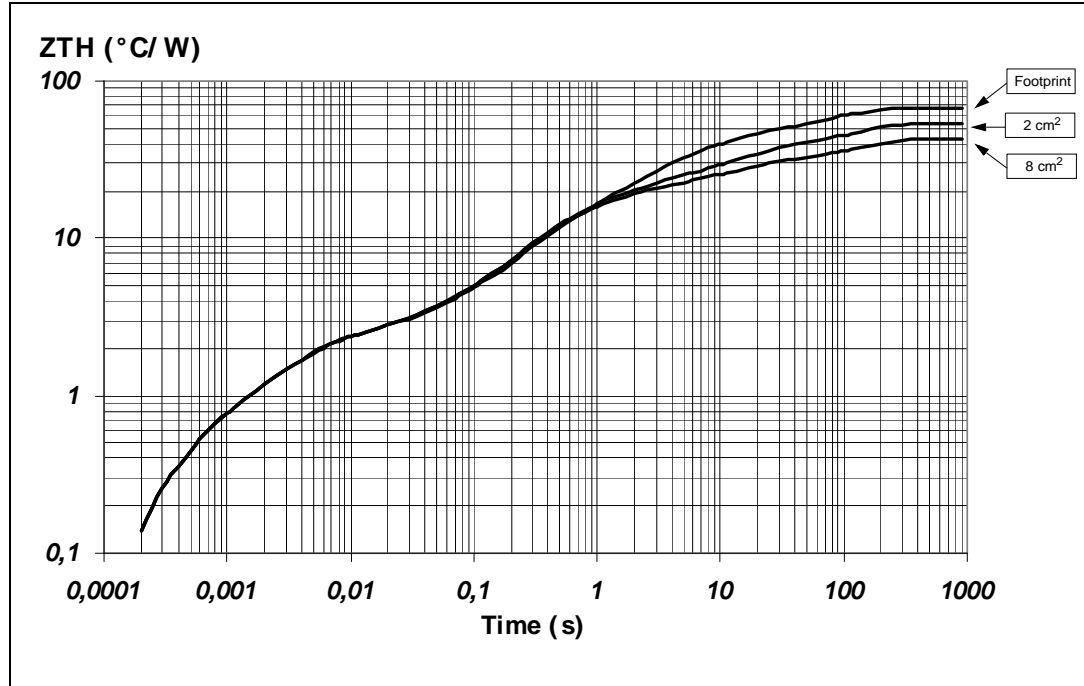


Figure 33. PowerSSO-12 thermal impedance junction ambient single pulse

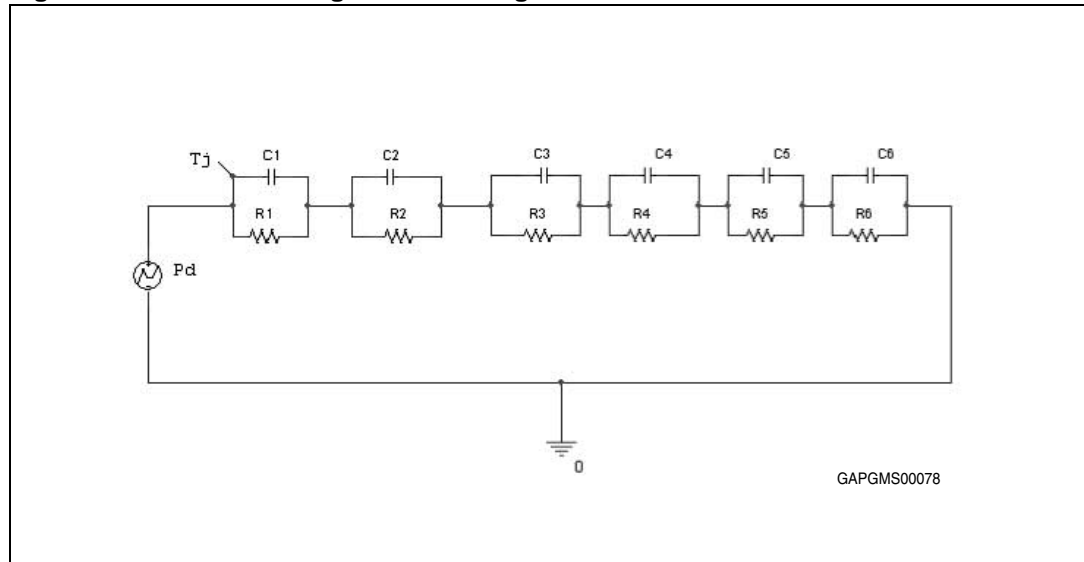


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 34. Thermal fitting model of Vreg in PowerSSO-12

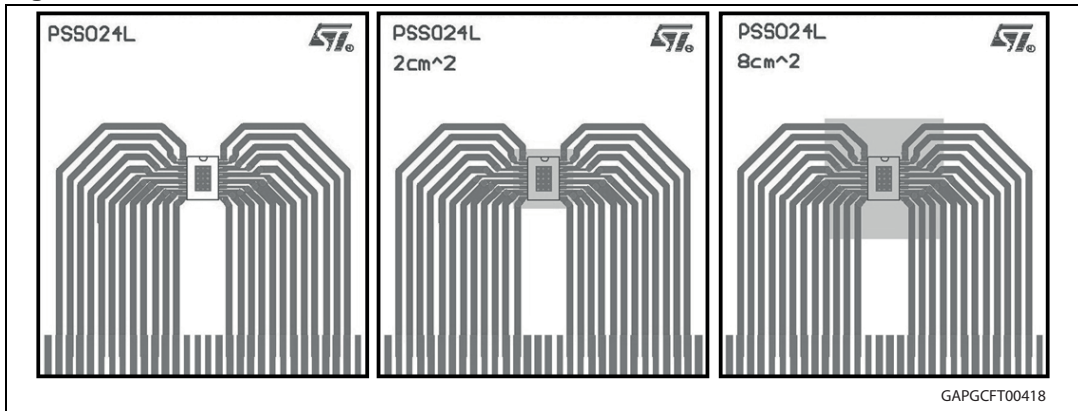


**Table 9. PowerSSO-12 thermal parameter**

<b>Area/island (cm<sup>2</sup>)</b>	<b>Footprint</b>	<b>2</b>	<b>8</b>
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	7		
R4 (°C/W)	10	10	9
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

## 4.2 PowerSSO-24 thermal data

Figure 35. PowerSSO-24 PC board<sup>(1)</sup>



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 $\mu$ m (front and back side) Thermal via separation 1.2 mm, Thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm, Footprint dimension 4.1 mm x 6.5 mm).

Figure 36.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

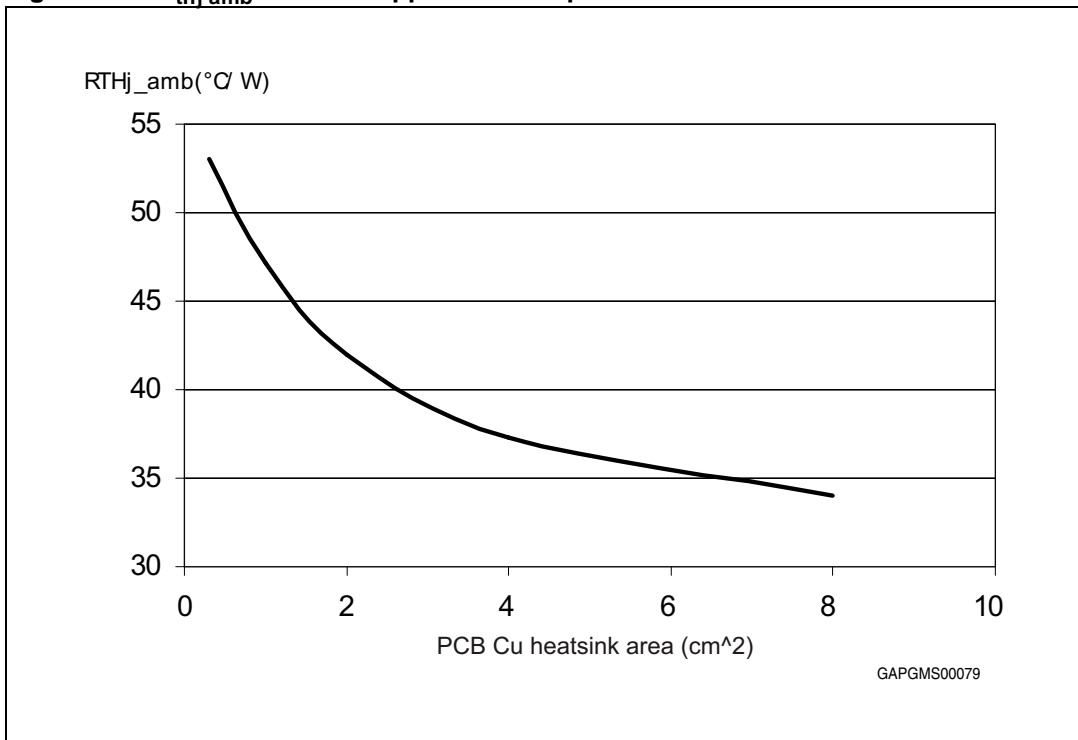
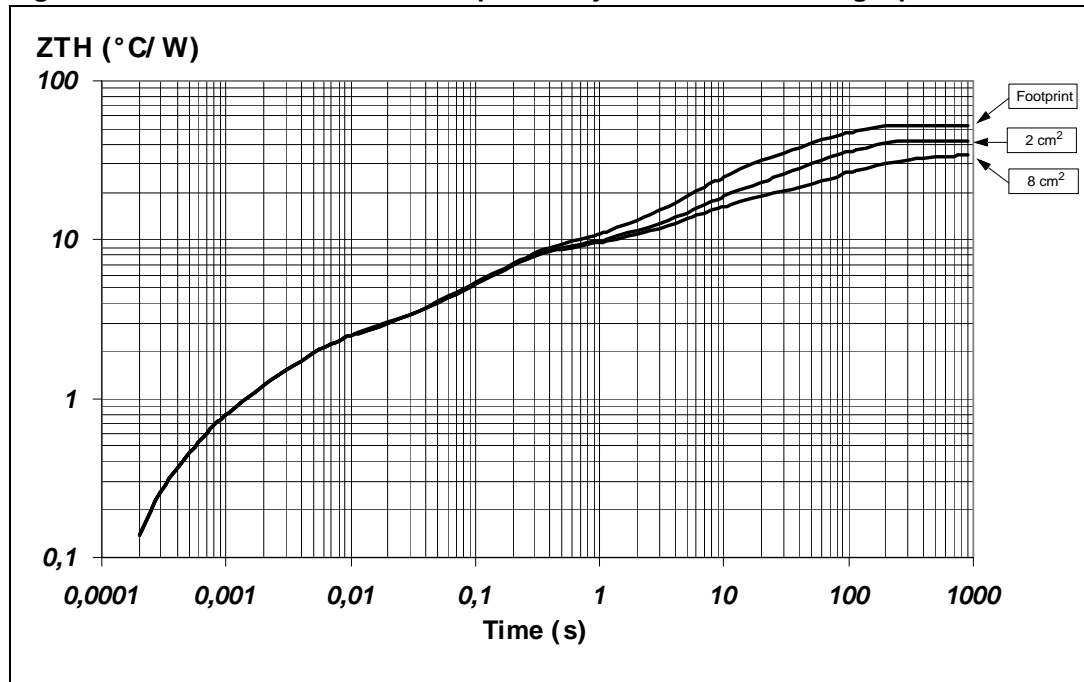


Figure 37. PowerSSO-24 thermal impedance junction ambient single pulse



Equation 5: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 38. Thermal fitting model of  $V_{reg}$  in PowerSSO-24

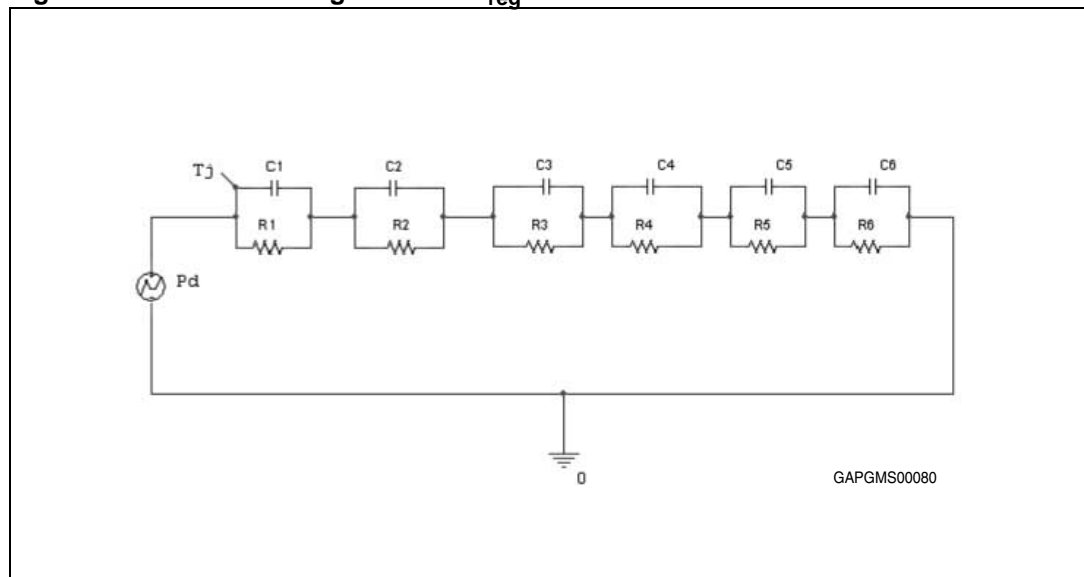




Table 10. PowerSSO-24 thermal parameter

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	0.45		
R2 (°C/W)	1.79		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 39. PowerSSO-12 package dimensions

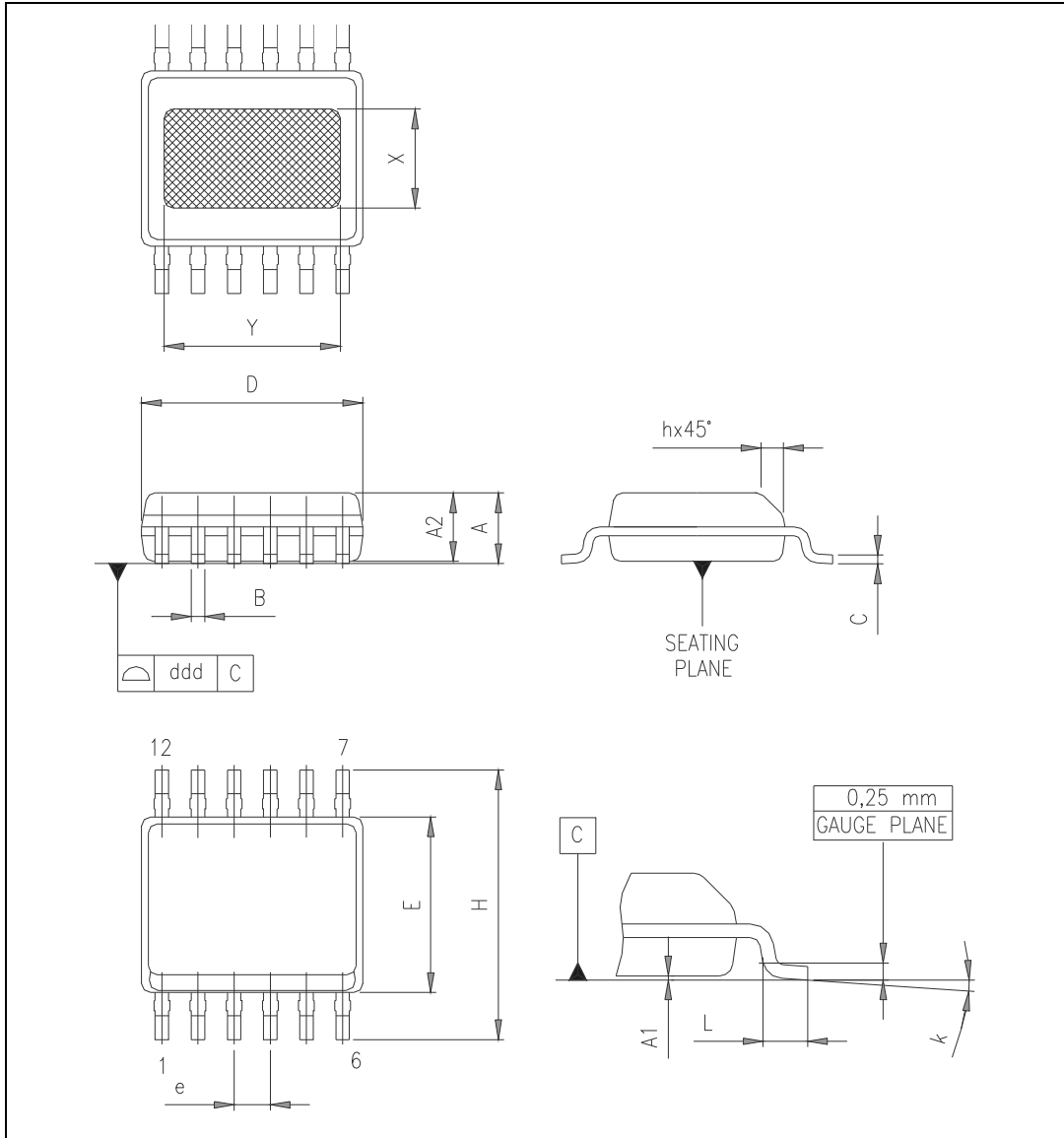


Table 11. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	2.200		2.800
Y	2.900		3.500
ddd			0.100

### 5.2 PowerSSO-24 mechanical data

Figure 40. PowerSSO-24 package dimensions

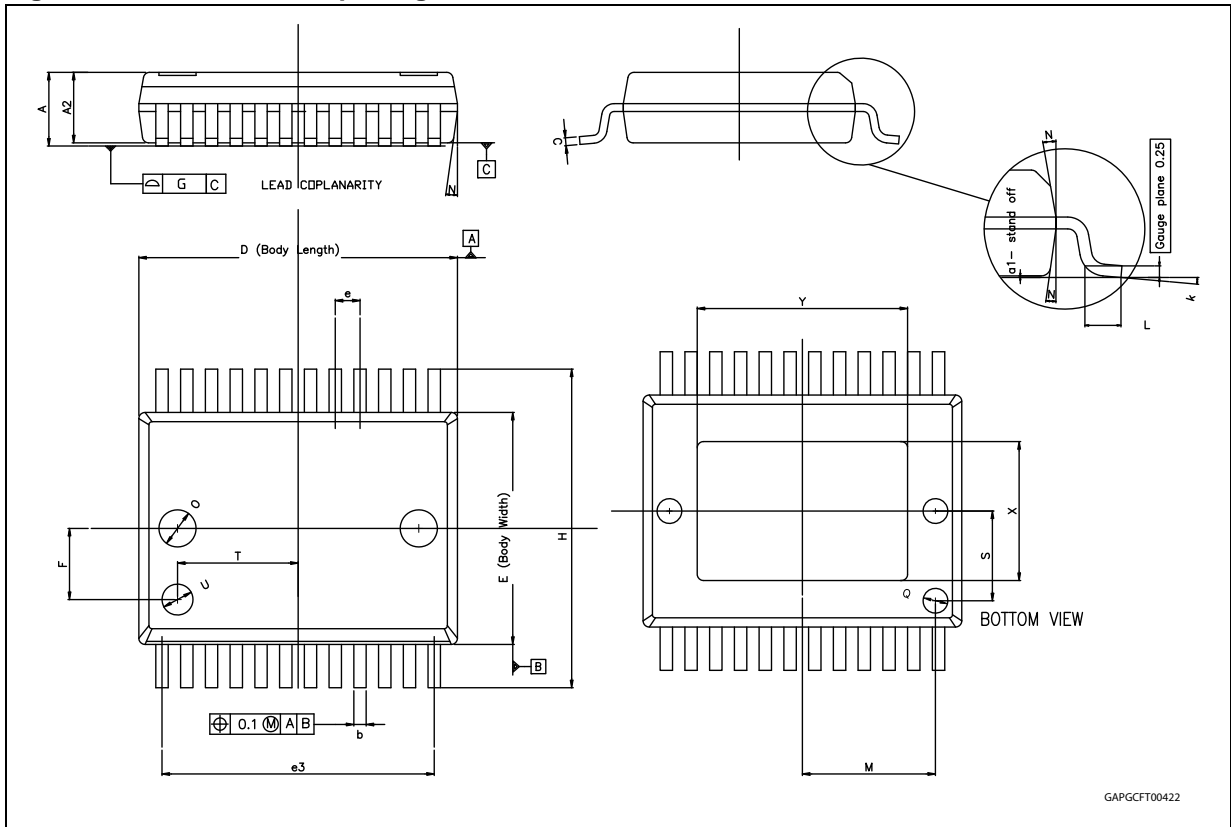


Table 12. PowerSSO-24 mechanical data<sup>(1)(2)</sup>

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.10
b	0.33		0.51
c	0.23		0.32
D <sup>(3)</sup>	10.10		10.50
E <sup>(3)</sup>	7.40		7.60
e		0.8	
e3		8.8	
F		2.3	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
k	0°		8°
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1	
N			10°
X	4.1		4.7
Y	6.5 4.9 <sup>(4)</sup>		7.1 5.5 <sup>(4)</sup>

1. No intrusion allowed inwards the leads.
2. Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
3. "D and E" do not include mold Flash or protusions.  
Mold Flash or protusions shall not exceed 0.15 mm.
4. Variations for small window leadframe option.

### 5.3 PowerSSO-12 packing information

Figure 41. PowerSSO-12 tube shipment (no suffix)

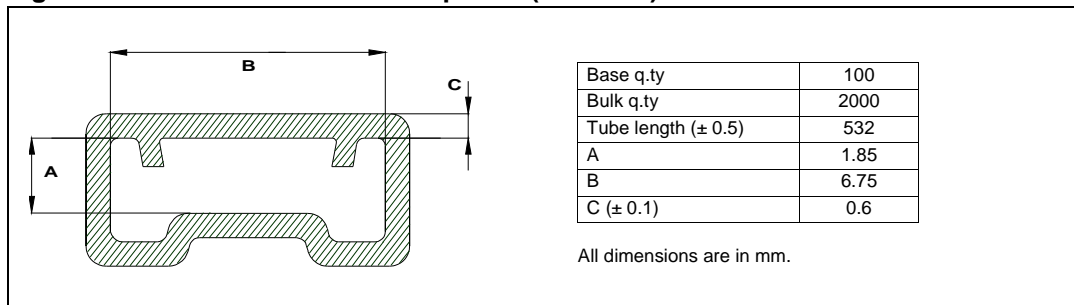
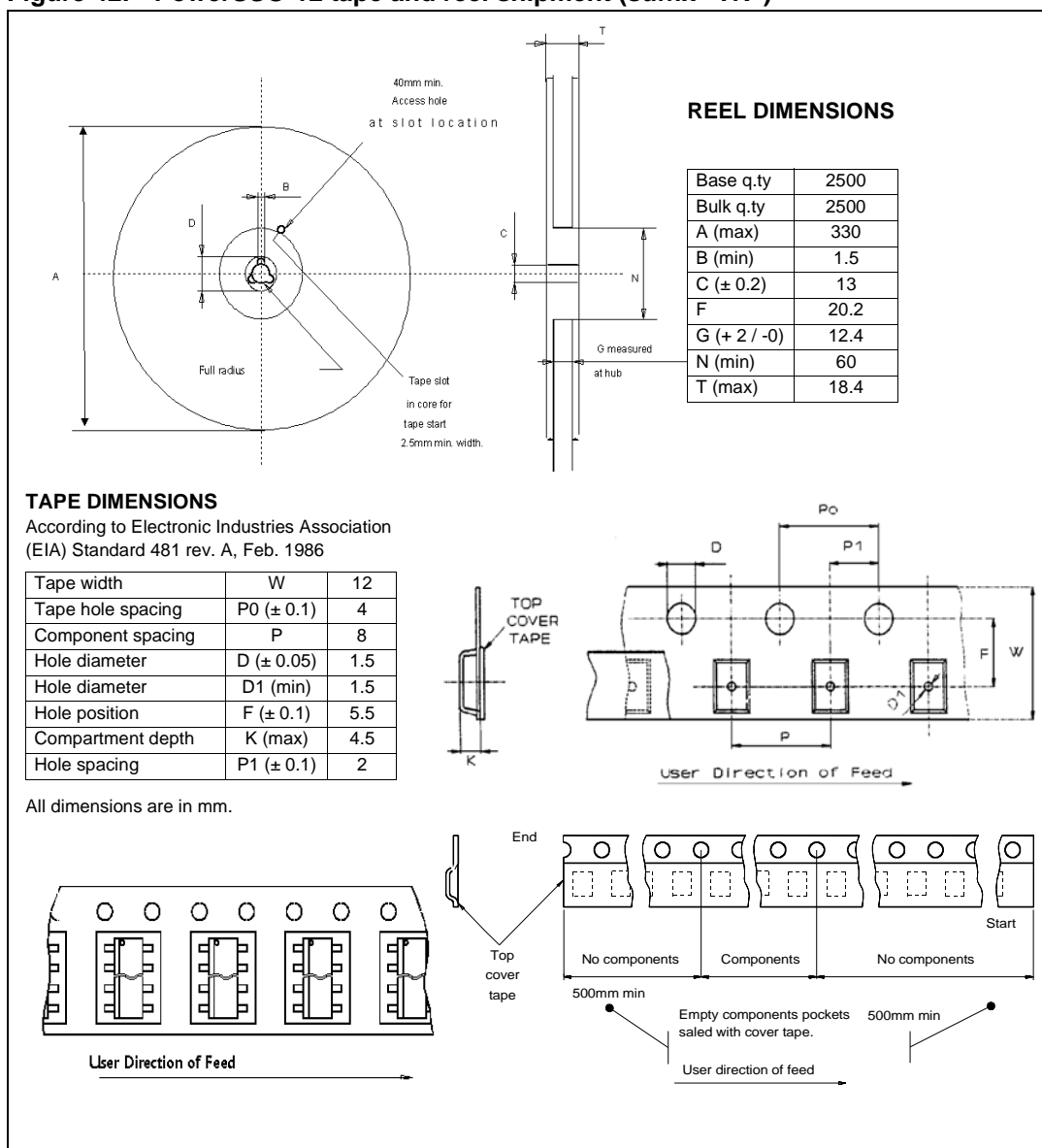


Figure 42. PowerSSO-12 tape and reel shipment (suffix "TR")



### 5.4 PowerSSO-24 packing information

Figure 43. PowerSSO-24 tube shipment (no suffix)

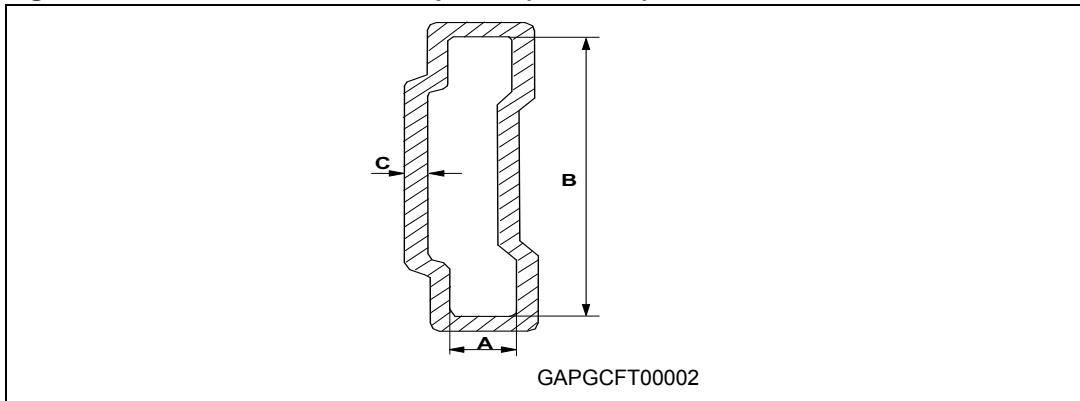
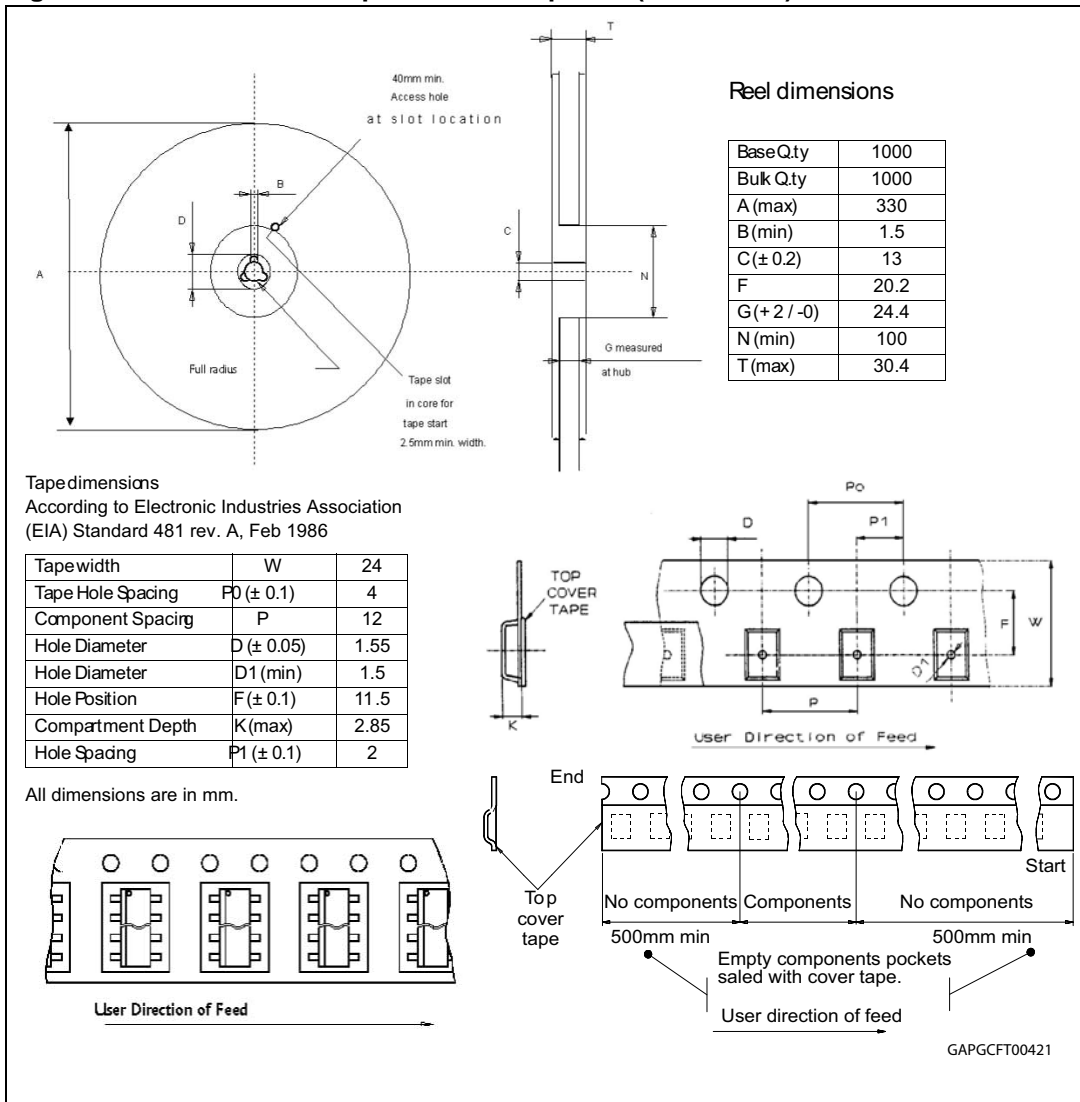


Figure 44. PowerSSO-24 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 13. Document revision history**

Date	Revision	Changes
26-May-2006	1	Initial release.
05-Jan-2007	2	L4995A and L4995R versions added: <i>Features</i> section updated and table added. <i>Table 1</i> updated. <i>Table 5: General</i> , Watchdog Iwi entry updated. <i>Figure 2: Block diagram of L4995A</i> and <i>Figure 3: Block diagram of L4995R</i> added. <i>Table 2: Pins descriptions</i> updated. <i>Table 4: Thermal data</i> updated. <i>List of tables</i> and <i>List of figures</i> added. Packaging information provided in new format. <i>Table 11: PowerSSO-12 mechanical data</i> X and Y values updated. Some sections reformatted for clarity. New disclaimer added.
18-May-2007	3	Updated <i>Table 2: Pins descriptions</i> . Updated <i>Figure 4: Pins configurations (L4995)</i> . <i>Table 1: Device summary</i> changed title.
09-Jul-2007	4	Updated <i>Table 2: Pins descriptions</i> .
09-Aug-2007	5	Updated <i>Table 2: Pins descriptions</i> . Updated <i>Table 12: PowerSSO-24 mechanical data</i> .



Table 13. Document revision history (continued)

Date	Revision	Changes
07-Dec-2007	6	<p>Updated <a href="#">Section 2.2: Thermal data</a>:</p> <ul style="list-style-type: none"> <li>– corrected note changing single layer with double layer.</li> </ul> <p>Updated <a href="#">Table 5: General</a>:</p> <ul style="list-style-type: none"> <li>– changed <math>I_{short}</math> typ. value from 750 to 800 mA</li> <li>– added <math>I_{short}</math> max. value</li> <li>– changed <math>I_{lim}</math> typ. value from 820 to 900 mA</li> <li>– added <math>I_{lim}</math> max. value</li> <li>– added <math>I_{lim}</math> note</li> <li>– added <math>V_{dp}</math> note</li> <li>– changed <math>I_{qn\_1}</math> typ. value from 110 to 90 <math>\mu</math>A</li> <li>– added <math>I_{qn\_1}</math> max. value</li> <li>– added <math>I_{qn\_50}</math> max. value</li> <li>– added <math>I_{qn\_150}</math> max. value</li> <li>– changed <math>I_{qn\_250}</math> typ. value from 1.2 to 1 mA</li> <li>– added <math>I_{qn\_250}</math> max. value</li> <li>– changed <math>I_{qn\_500}</math> typ. value from 2.4 to 2.1 mA</li> <li>– added <math>I_{qn\_500}</math> max. value</li> </ul> <p>Updated <a href="#">Table 6: Reset</a>:</p> <ul style="list-style-type: none"> <li>– changed <math>V_{Rlth}</math> parameter definition from “Reset timing low” to “Reset delay circuit low threshold”</li> <li>– changed <math>V_{Rhth}</math> parameter definition from “Reset timing high” to “Reset delay circuit high threshold”</li> <li>– added <math>T_{rd}</math> min. and max. values</li> </ul> <p>Updated <a href="#">Table 7: Watchdog</a>:</p> <ul style="list-style-type: none"> <li>– added <math>I_{wi}</math> max value</li> </ul> <p>Updated <a href="#">Table 8: Enable</a>:</p> <ul style="list-style-type: none"> <li>– changed Pull down current symbol from <math>R_{En}</math> to <math>I_{En}</math></li> <li>– changed <math>I_{En}</math> typ. value from 2.5 to 10 <math>\mu</math>A</li> <li>– added <math>I_{En}</math> max. value</li> </ul> <p>Added <a href="#">Section 2.4: Electrical characteristics curves</a>.</p> <p>Added <a href="#">Section 2.5: Test circuit and waveforms plot</a>.</p> <p>Added <a href="#">Section 4: Package and PCB thermal data</a></p>
03-Oct-2008	7	<p>Updated PowerSSO-24 information:</p> <ul style="list-style-type: none"> <li>– changed <a href="#">Figure 40: PowerSSO-24 package dimensions</a></li> <li>– changed <a href="#">Table 12: PowerSSO-24 mechanical data</a>.</li> </ul>
19-Mar-2009	8	Updated <a href="#">Table 4: Thermal data</a>
19-May-2009	9	<p>Updated <a href="#">Table 2: Pins descriptions</a>.</p> <p>Updated <a href="#">Figure 4: Pins configurations (L4995)</a></p> <ul style="list-style-type: none"> <li>– Changed GND to substrate</li> </ul>

Table 13. Document revision history (continued)

Date	Revision	Changes
24-Jun-2009	10	<i>Table 12: PowerSSO-24 mechanical data:</i> <ul style="list-style-type: none"><li>– Deleted A (min) value</li><li>– Changed A (max) value from 2.50 to 2.45</li><li>– Changed A2 (max) value from 2.40 to 2.35</li><li>– Updated K row</li><li>– Changed L (min) value from 0.6 to 0.55</li><li>– Changed L (max) value from 1 to 0.85</li></ul>
12-Jul-2010	11	Added <i>Figure 27: Stability region<sup>(1)</sup></i> .
09-Mar-2012	12	Added footnote in <i>Table 3: Absolute maximum ratings</i> .
17-Oct-2012	13	<i>Table 6: Reset:</i> <ul style="list-style-type: none"><li>– <math>T_{rd}</math>: updated min, typ and max values</li></ul>
20-Sep-2013	14	Updated disclaimer.

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