

N-channel 800 V, 0.37  $\Omega$  typ., 12 A SuperMESH™ 5 Power MOSFETs in D<sup>2</sup>PAK, TO-220FP, TO-220 and TO-247 packages

Datasheet - production data

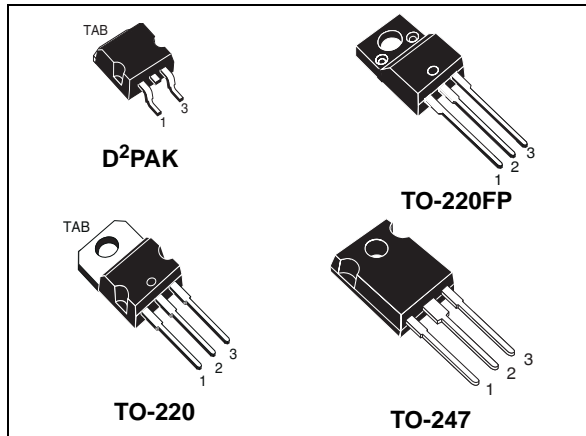
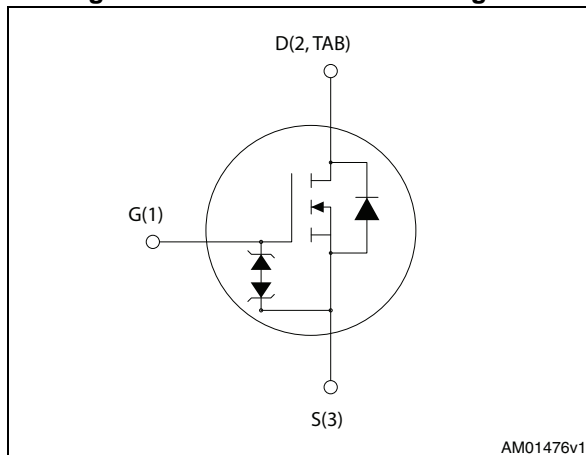


Figure 1. Internal schematic diagram



## Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STB13N80K5	800 V	0.45 $\Omega$	12 A	190 W
STF13N80K5				35 W
STP13N80K5				190 W
STW13N80K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Zener-protected Power MOSFETs realized in SuperMESH™ 5, a revolutionary avalanche-rugged very high voltage Power MOSFET technology based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB13N80K5	13N80K5	D <sup>2</sup> PAK	Tape and reel
STF13N80K5		TO-220FP	Tube
STP13N80K5		TO-220	
STW13N80K5		TO-247	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK, TO-220, TO-247	TO-220FP	
V <sub>GS</sub>	Gate-source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	12	12 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	7.6	7.6 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	48	48 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	190	35	W
I <sub>AR</sub>	Max current during repetitive or single pulse avalanche (pulse width limited by T <sub>jmax</sub> )	4		A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> =I <sub>AS</sub> , V <sub>DD</sub> = 50 V)	148		mJ
V <sub>iso</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)	2500		V
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50		V/ns
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150		°C

- Limited by package.
- Pulse width limited by safe operating area.
- I<sub>SD</sub> ≤ 12 A, di/dt ≤ 100 A/μs, V<sub>Peak</sub> ≤ V<sub>(BR)DSS</sub>
- V<sub>DS</sub> ≤ 640 V

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	TO-220	TO-220FP	TO-247	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.66		3.57		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb max	62.5		50		
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	30				

- When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 800\text{ V}, T_C = 125\text{ °C}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$		0.37	0.45	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	870	-	pF
$C_{oss}$	Output capacitance		-	50	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }640\text{ V}$	-	110	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	43	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}, I_D = 12\text{ A}$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 22</a> )	-	29	-	nC
$Q_{gs}$	Gate-source charge		-	7	-	nC
$Q_{gd}$	Gate-drain charge		-	18	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 6\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 24</a> )	-	16	-	ns
$t_r$	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
$t_f$	Fall time		-	16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		14	A
$I_{SDM}$	Source-drain current (pulsed)		-		56	A
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0$ , $I_{SD} = 12\text{ A}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , (see <a href="#">Figure 23</a> )	-	406		ns
$Q_{rr}$	Reverse recovery charge		-	5.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	28		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 23</a> )	-	600		ns
$Q_{rr}$	Reverse recovery charge		-	7.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	26		A

1. Pulsed: pulse duration =  $300\ \mu\text{s}$ , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK

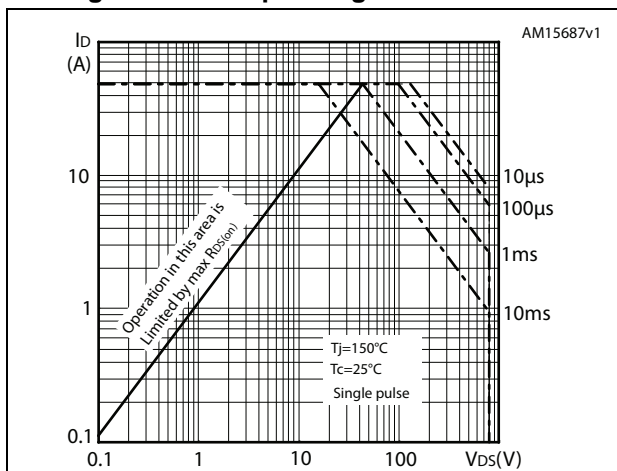


Figure 3. Thermal impedance for D<sup>2</sup>PAK

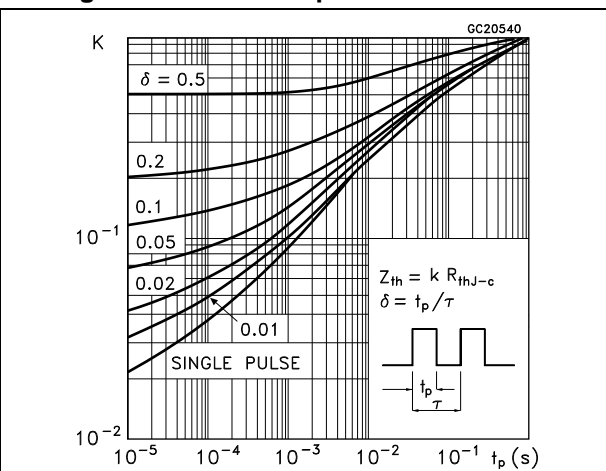


Figure 4. Safe operating area for TO-220FP

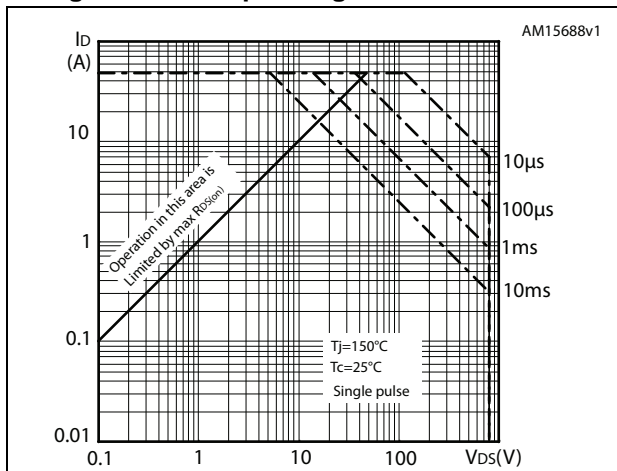


Figure 5. Thermal impedance for TO-220FP

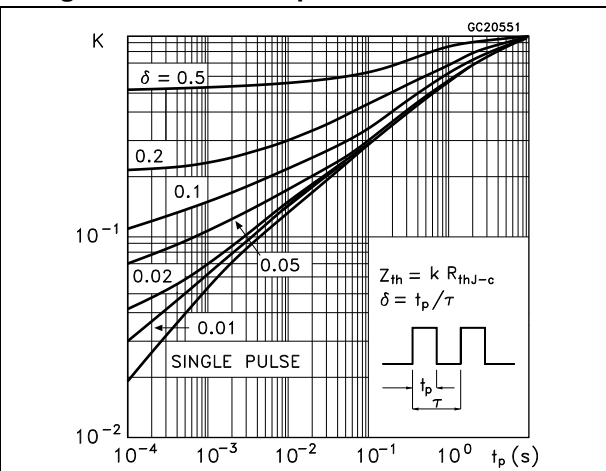


Figure 6. Safe operating area for TO-220

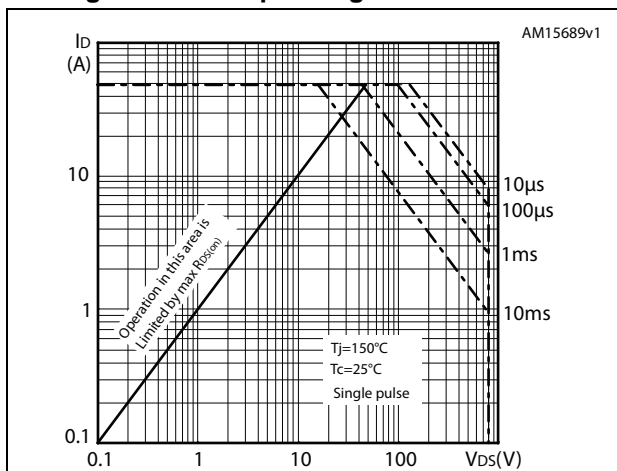


Figure 7. Thermal impedance for TO-220

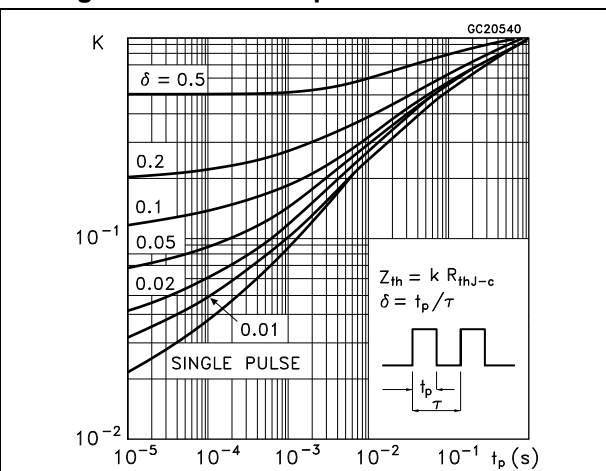


Figure 8. Safe operating area for TO-247

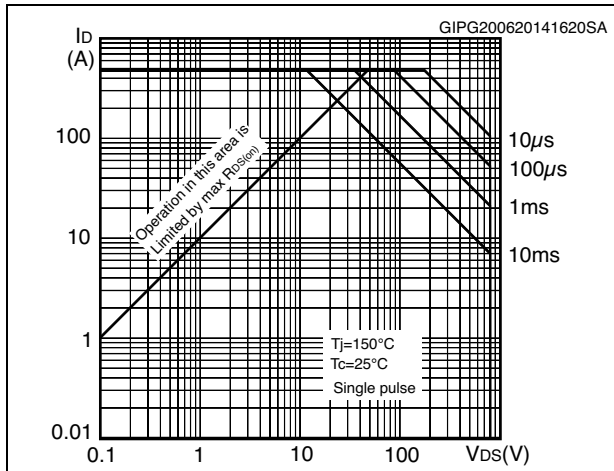


Figure 9. Thermal impedance for TO-247

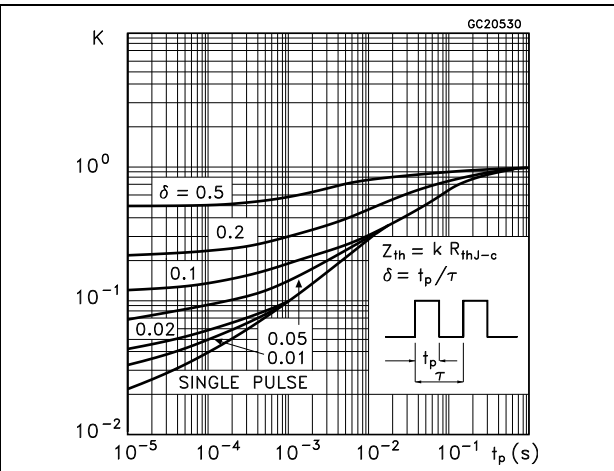


Figure 10. Output characteristics

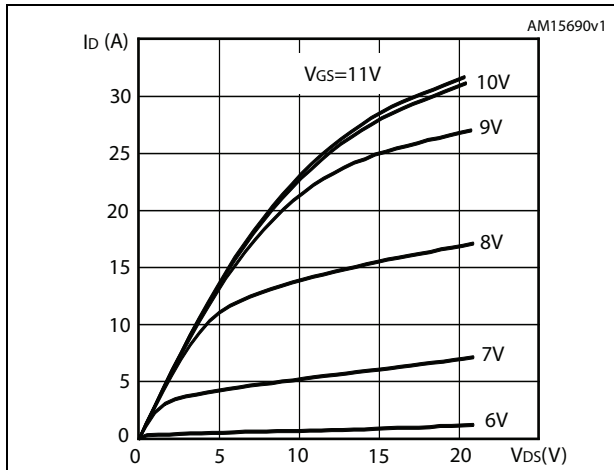


Figure 11. Transfer characteristics

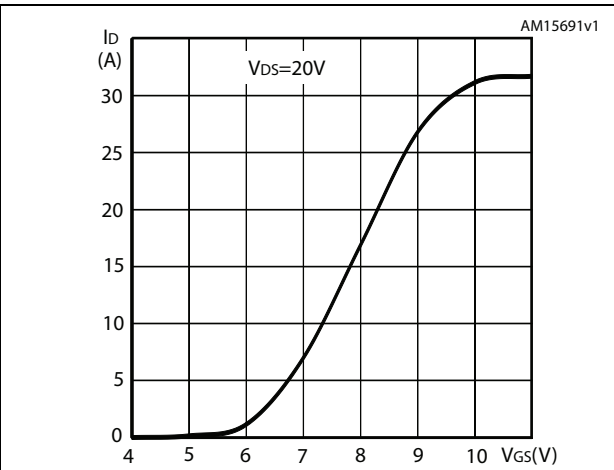


Figure 12. Normalized  $V_{(BR)DSS}$  vs temperature

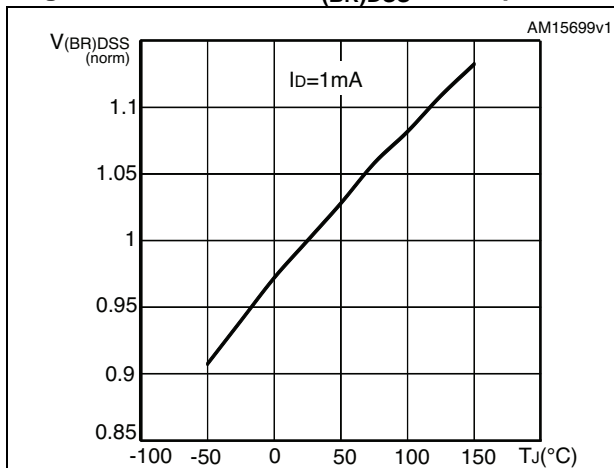


Figure 13. Static drain-source on-resistance

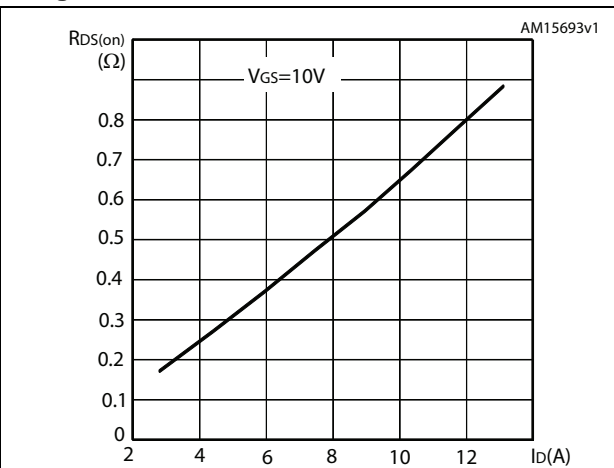


Figure 14. Gate charge vs gate-source voltage

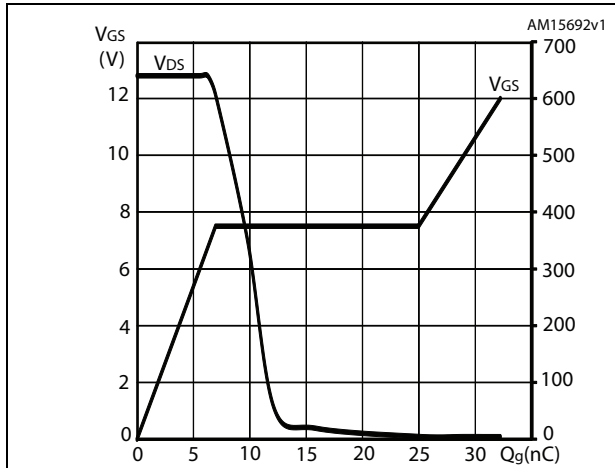


Figure 15. Capacitance variations

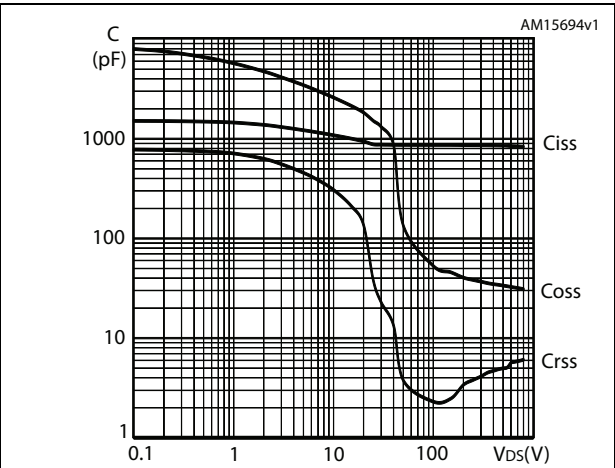


Figure 16. Normalized gate threshold voltage vs temperature

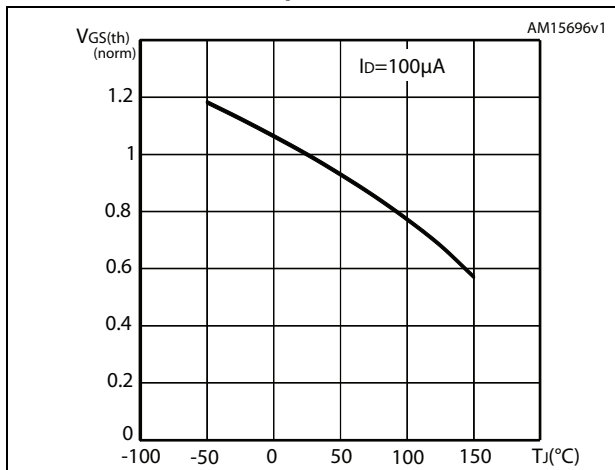


Figure 17. Normalized on-resistance vs temperature

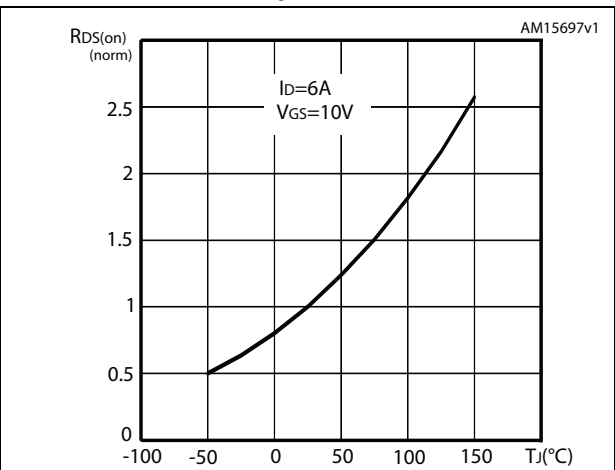


Figure 18. Source-drain diode forward characteristics

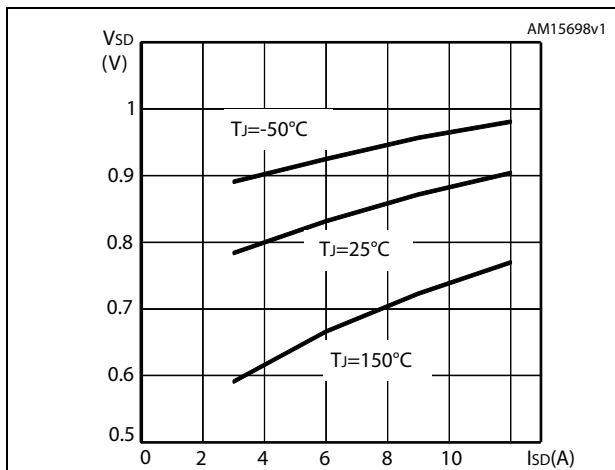


Figure 19. Output capacitance stored energy

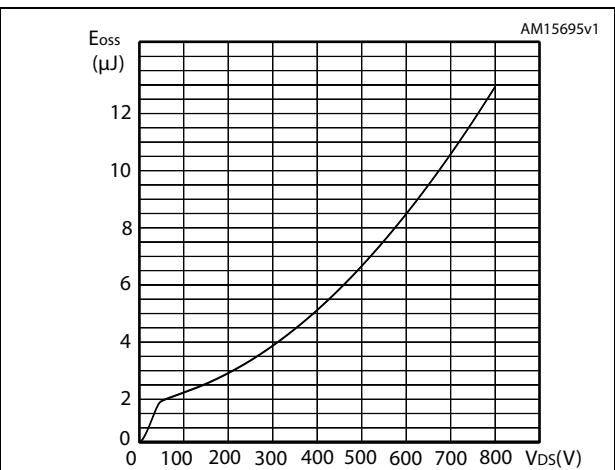
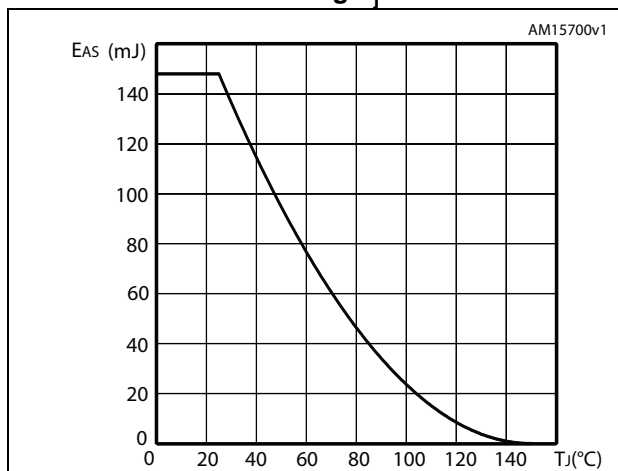


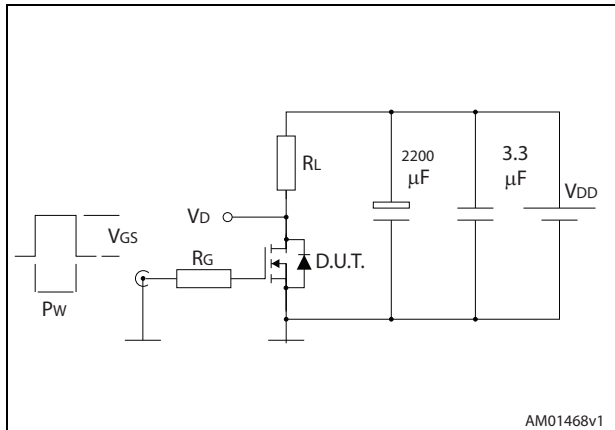


Figure 20. Maximum avalanche energy vs. starting  $T_j$



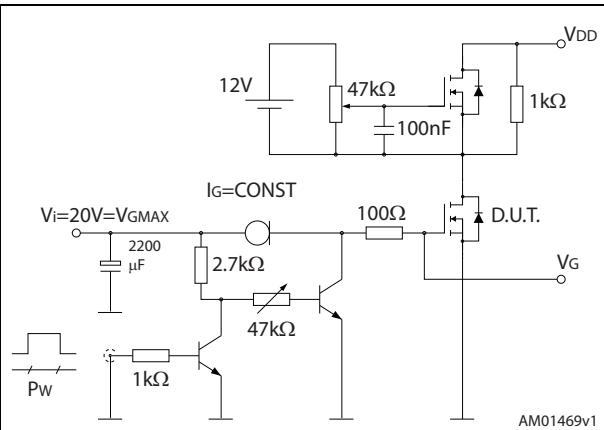
### 3 Test circuits

Figure 21. Switching times test circuit for resistive load



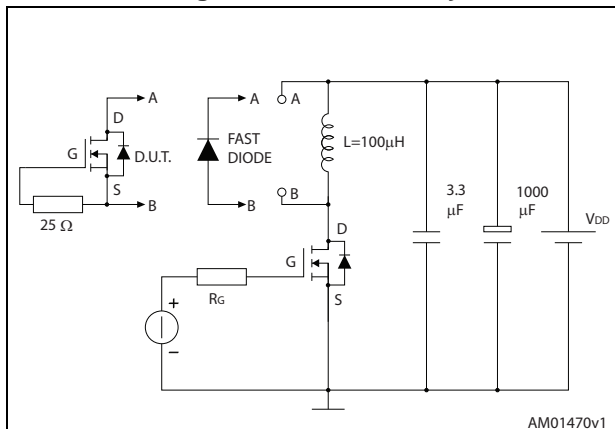
AM01468v1

Figure 22. Gate charge test circuit



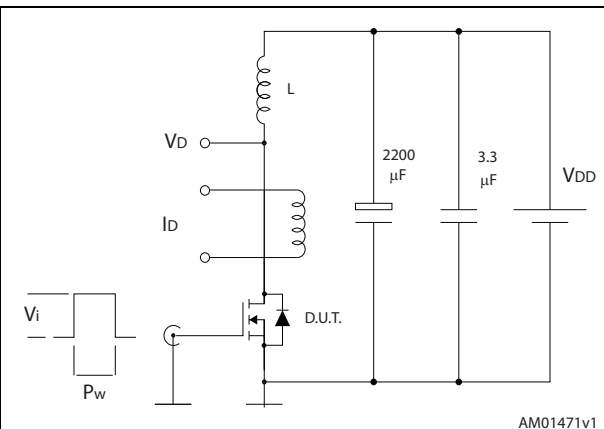
AM01469v1

Figure 23. Test circuit for inductive load switching and diode recovery times



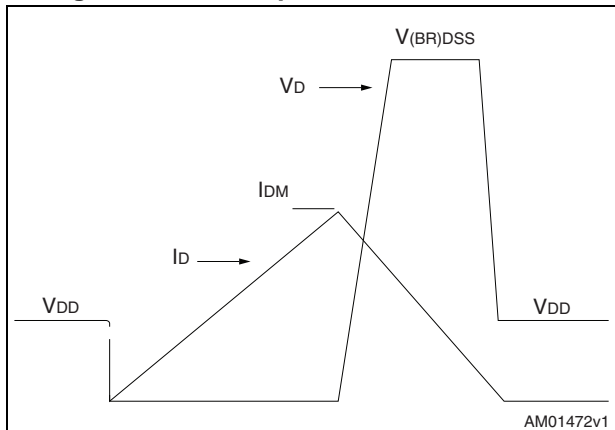
AM01470v1

Figure 24. Unclamped inductive load test circuit



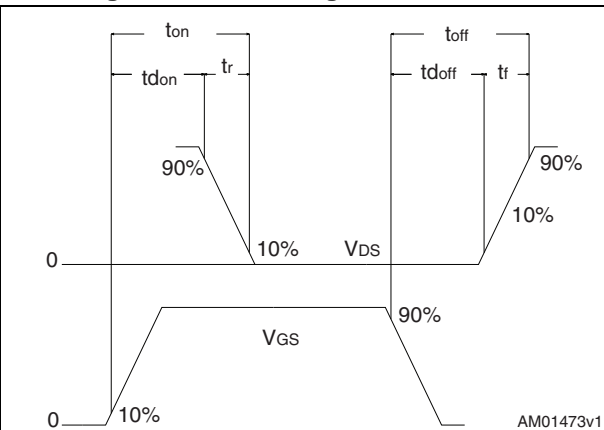
AM01471v1

Figure 25. Unclamped inductive waveform



AM01472v1

Figure 26. Switching time waveform



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

4.1 D<sup>2</sup>PAK, STB13N80K5

Figure 27. D<sup>2</sup>PAK (TO-263) drawing

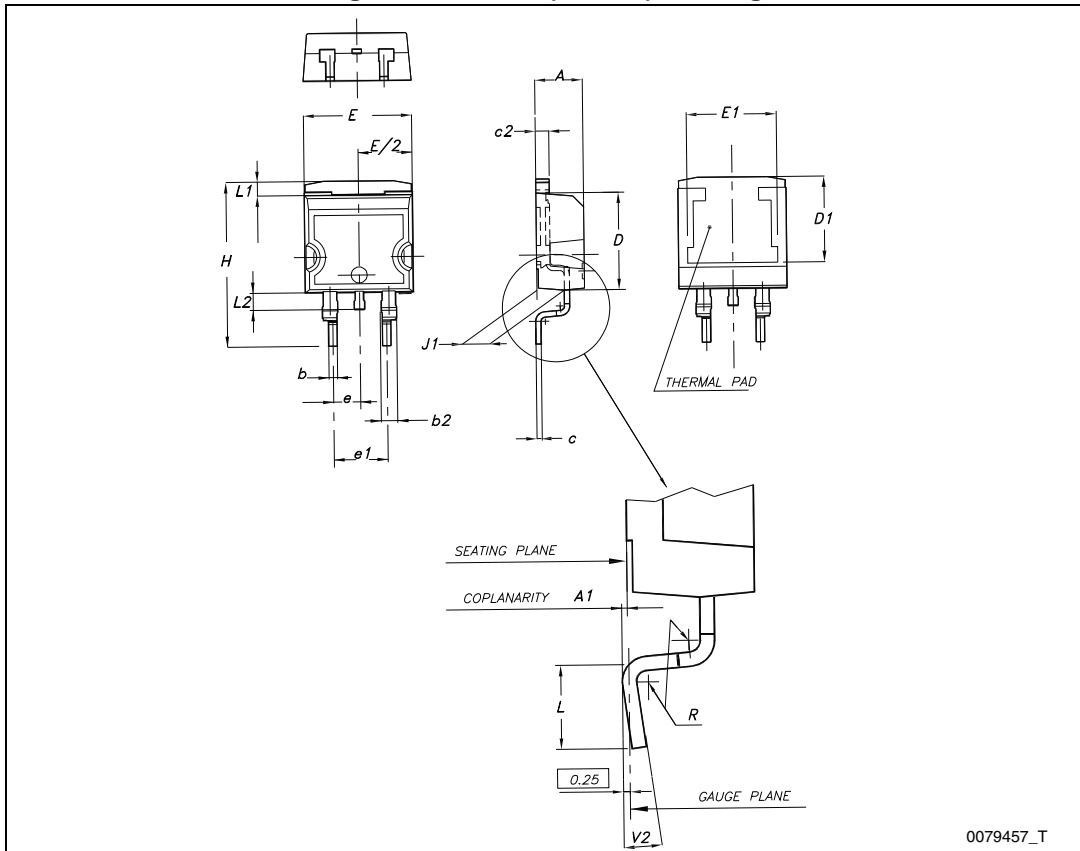
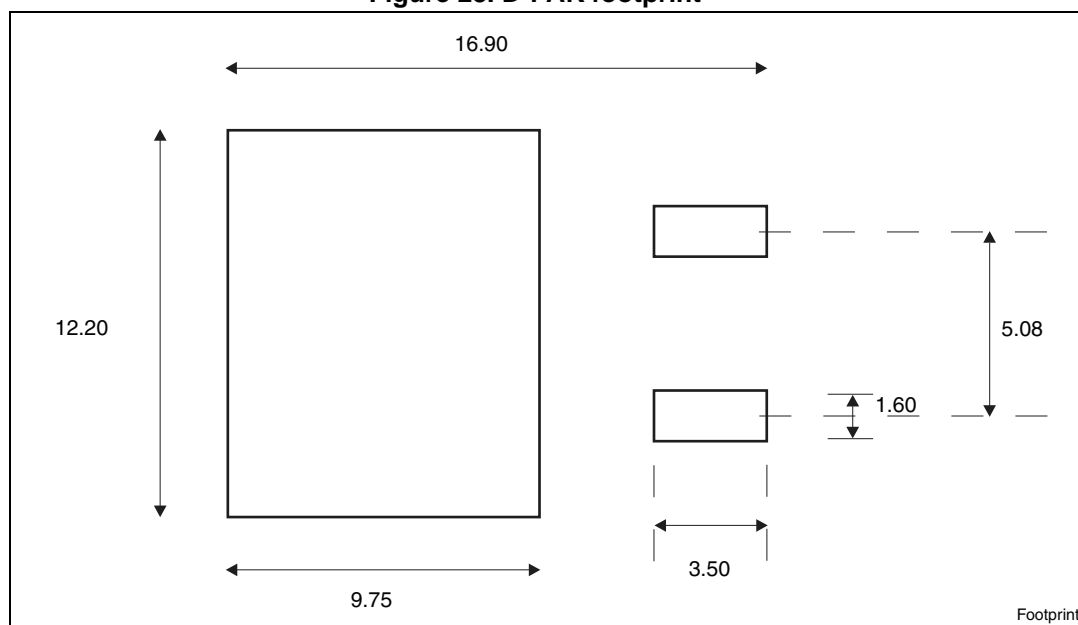


Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

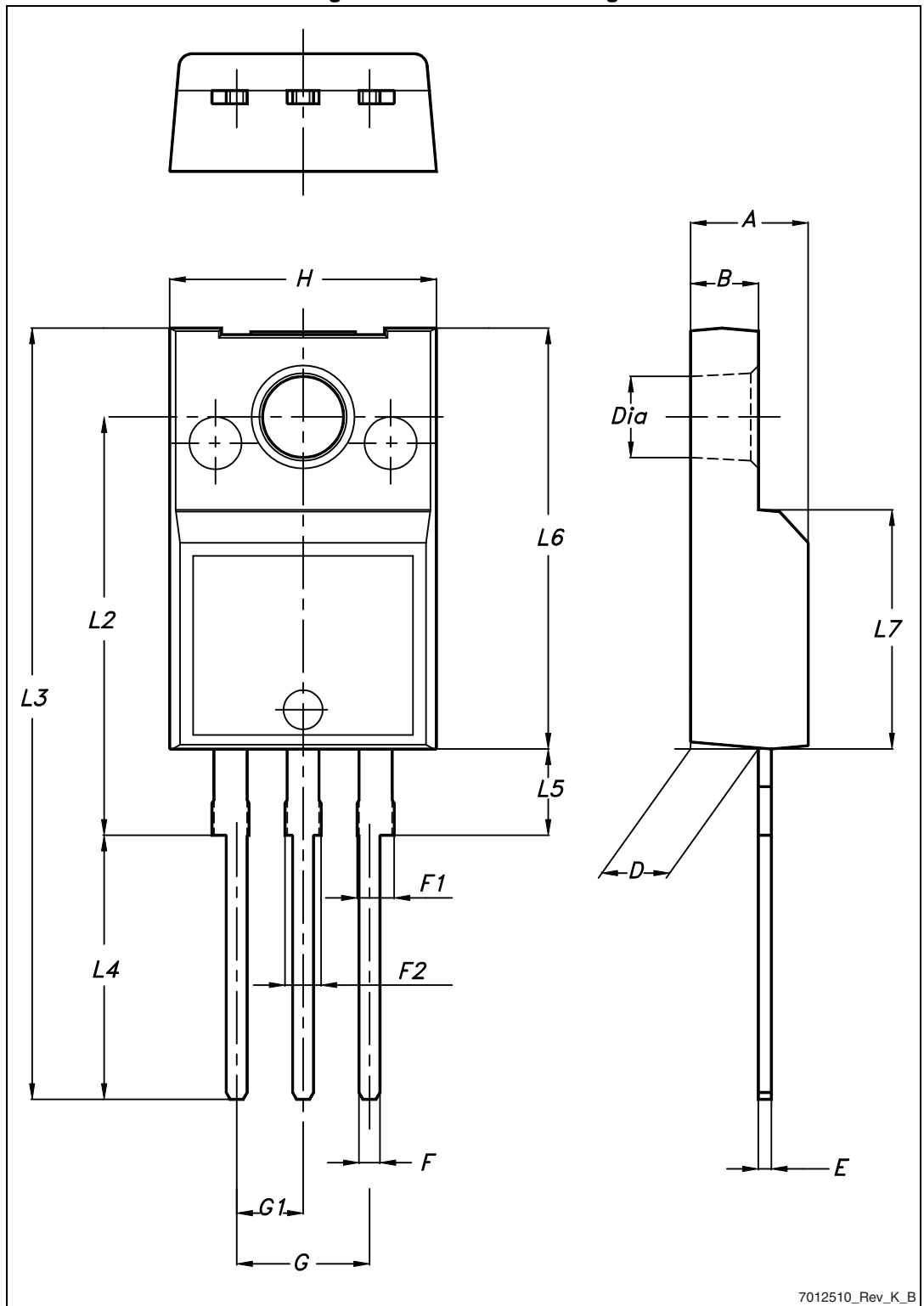
Figure 28. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

### 4.2 TO-220FP, STF13N80K5

Figure 29. TO-220FP drawing



7012510\_Rev\_K\_B

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2



4.3 TO-220, STP13N80K5

Figure 30. TO-220 type A drawing

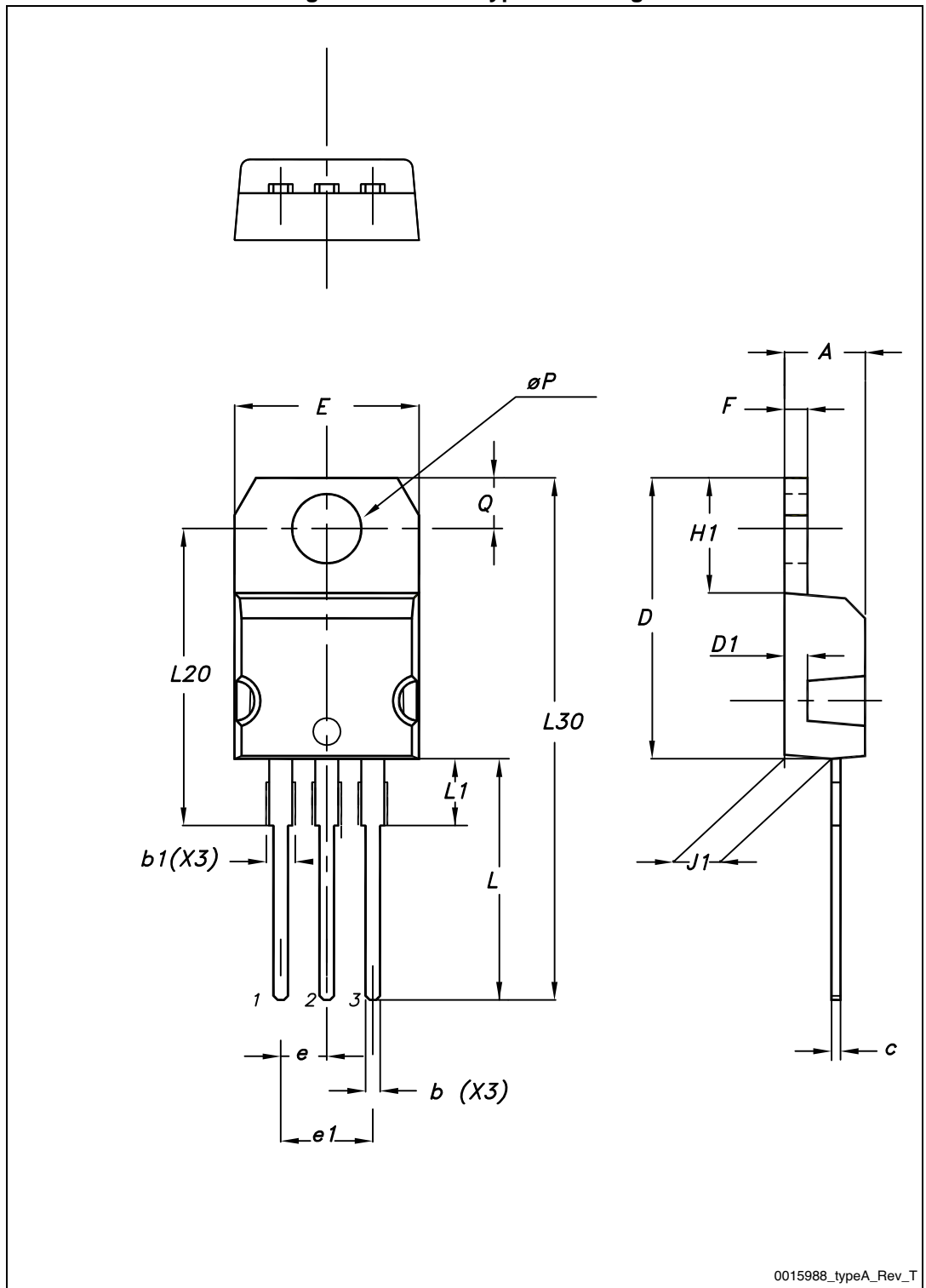


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

### 4.4 TO-247, STW13N80K5

Figure 31. TO-247 drawing

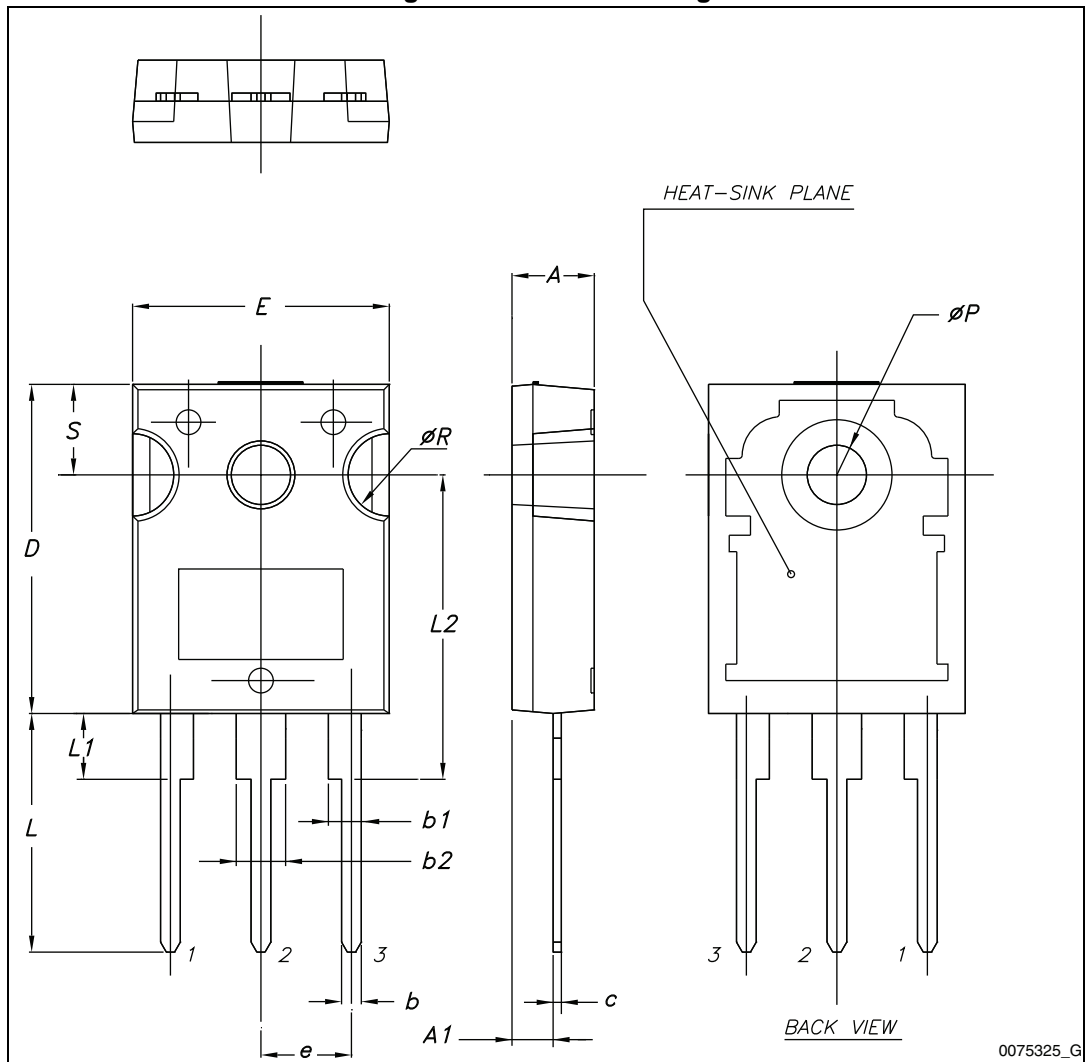


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

# 5 Packaging mechanical data

Figure 32. Tape

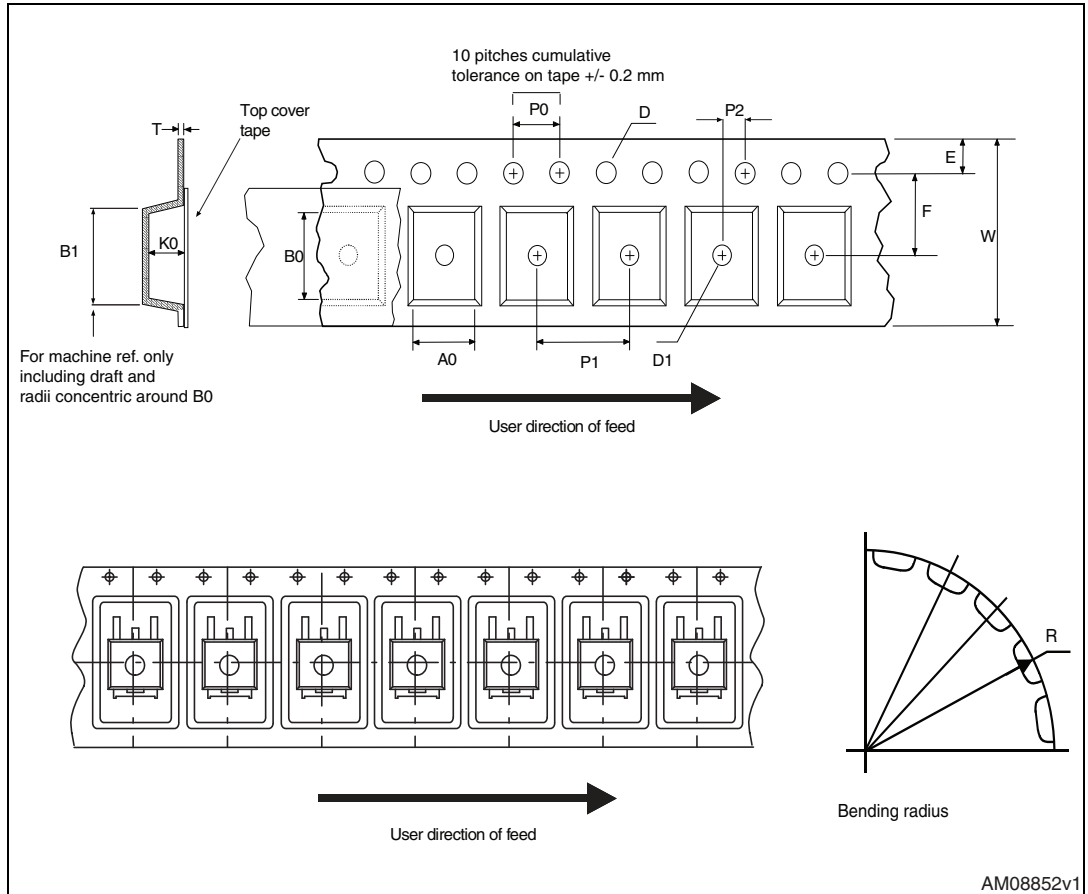
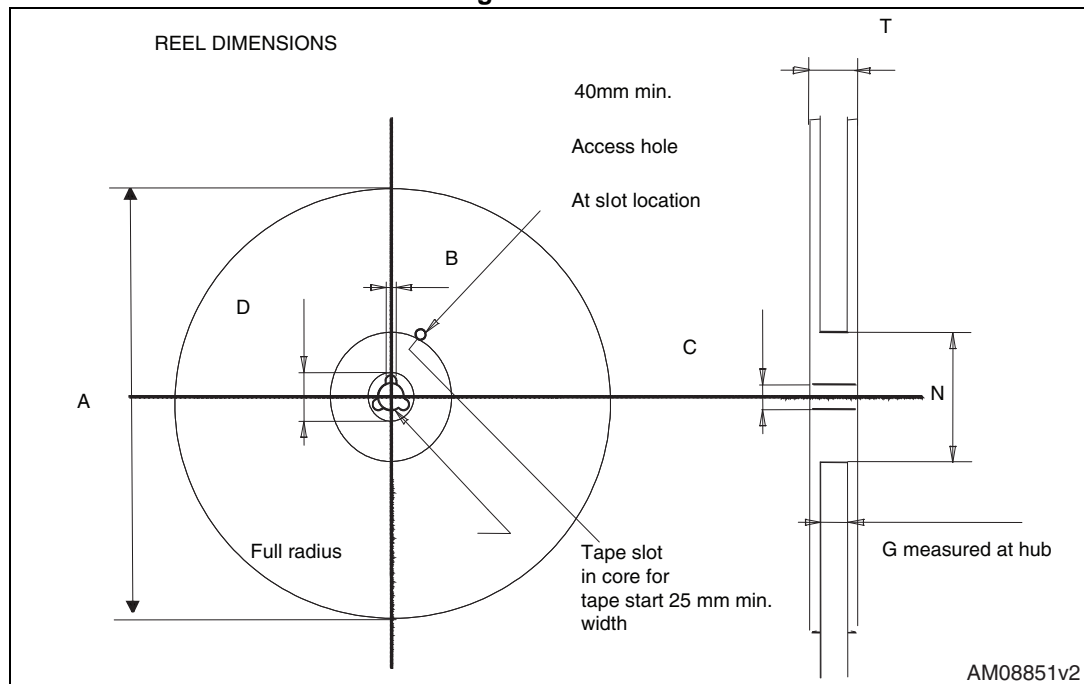


Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 33. Reel



## 6 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
07-Mar-2013	1	Initial release.
27-Mar-2013	2	Updated <a href="#">Figure 1: Internal schematic diagram</a> . Minor text changes. Document status promoted from preliminary data to production data.
15-Apr-2013	3	<ul style="list-style-type: none"> <li>– Modified: <math>E_{AS}</math> value, the entire typical values on <a href="#">Table 5, 6 and 7</a></li> <li>– Inserted: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li> <li>– Minor text changes</li> </ul>
27-Jun-2014	4	<ul style="list-style-type: none"> <li>– Added: TO-247 package</li> <li>– Added: <a href="#">Figure 8 and 9</a></li> <li>– Updated: <a href="#">Section 4: Package mechanical data</a></li> <li>– Minor text changes</li> </ul>

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