STL120N8F7

N-channel 80 V, 3.7 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

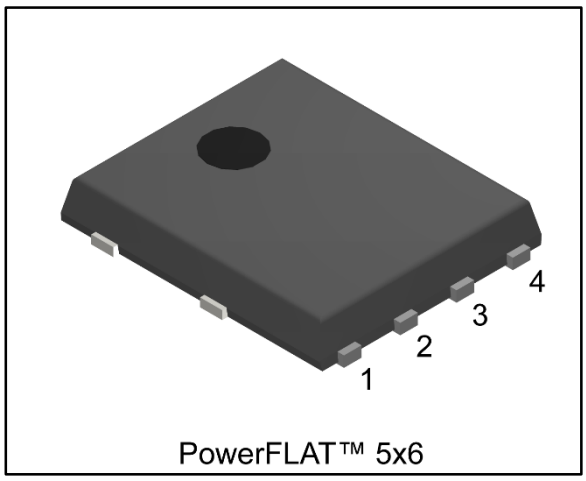
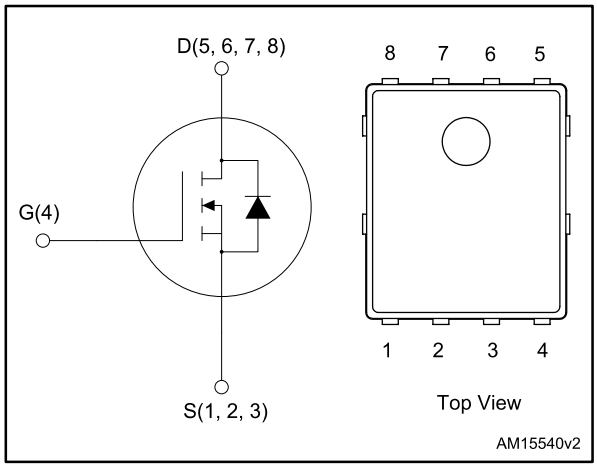


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL120N8F7	80 V	4.4 mΩ	120 A	140 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL120N8F7	120N8F7	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_{case} = 25 °C	120	A
	Drain current (continuous) at T_{case} = 100 °C	90	
I_{DM} (1)(2)	Drain current (pulsed)	480	A
I_D (3)	Drain current (continuous) at T_{pcb} = 25 °C	23	A
	Drain current (continuous) at T_{pcb} = 100 °C	17	
I_{DM} (2)(3)	Drain current (pulsed)	92	A
P_{TOT} (1)	Total dissipation at T_{case} = 25 °C	140	W
P_{TOT} (3)	Total dissipation at T_{pcb} = 25 °C	4.8	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		

Notes:

(1) This value is rated according to $R_{thj\text{-}c}$.

(2) Pulse width is limited by safe operating area.

(3) This value is rated according to $R_{thj\text{-}pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.05	

Notes:

(1) When mounted on a 1-inch² FR-4 board, 2oz Cu, t < 10 s

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	80			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 80 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 11.5 A		3.7	4.4	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 40 V, f = 1 MHz, V_{GS} = 0 V	-	4600	-	pF
C_{oss}	Output capacitance		-	800	-	
C_{rss}	Reverse transfer capacitance		-	64	-	
Q_g	Total gate charge	V_{DD} = 40 V, I_D = 23 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	60	-	nC
Q_{gs}	Gate-source charge		-	24.7	-	
Q_{gd}	Gate-drain charge		-	14.8	-	
R_G	Gate input resistance	I_D = 0 A, gate DC bias = 0 V, f = 1 MHz, magnitude of alternative signal = 20 mV	-		2.0	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 40 V, I_D = 11.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	34.5	-	ns
t_r	Rise time		-	16.8	-	
$t_{d(off)}$	Turn-off delay time		-	60	-	
t_f	Fall time		-	15.4	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 23 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 23 A, di/dt = 100 A/µs, V_{DD} = 64 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	48.6		ns
Q_{rr}	Reverse recovery charge		-	65.6		nC
I_{RRM}	Reverse recovery current		-	2.7		A

Notes:

(1) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

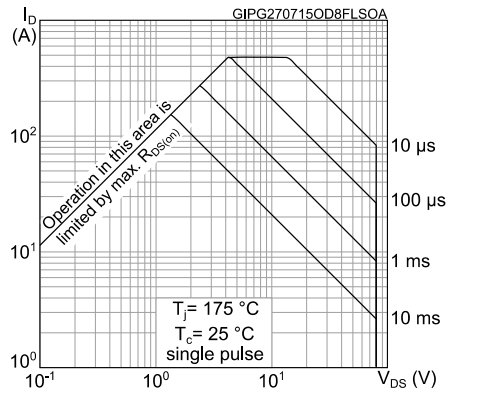


Figure 3: Thermal impedance

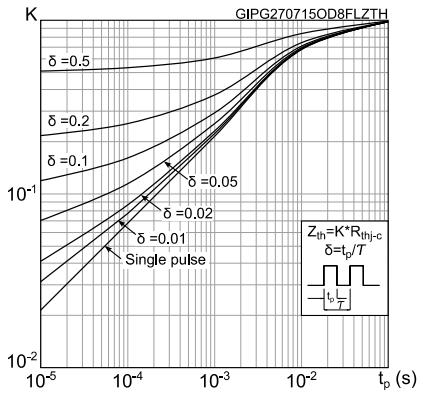


Figure 4: Output characteristics

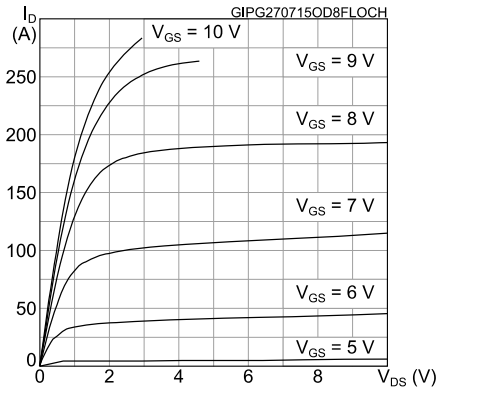


Figure 5: Transfer characteristics

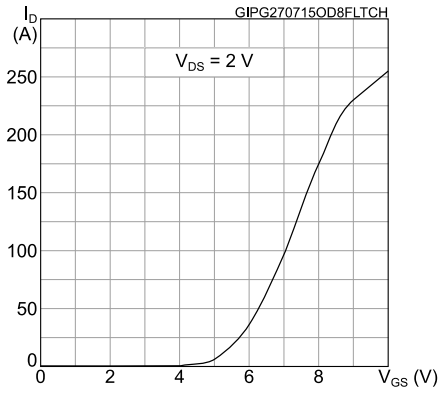


Figure 6: Gate charge vs gate-source voltage

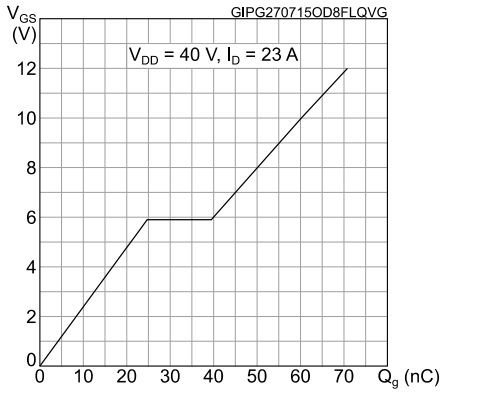


Figure 7: Static drain-source on-resistance

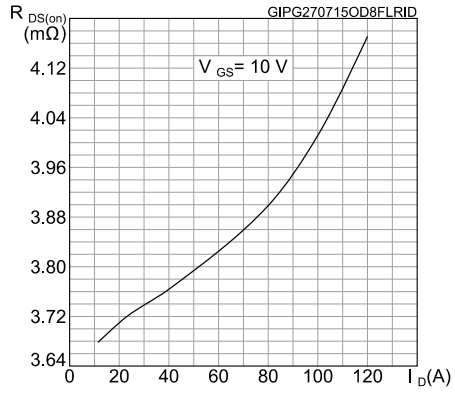


Figure 8: Capacitance variations

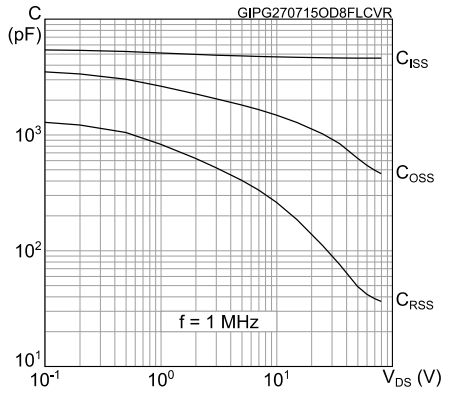


Figure 9: Normalized gate threshold voltage vs temperature

Figure 10: Normalized on-resistance vs temperature

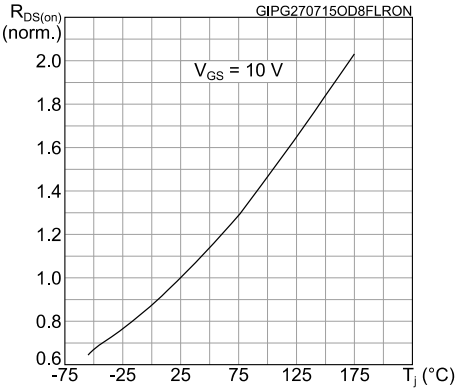


Figure 11: Normalized V(BR)DSS vs temperature

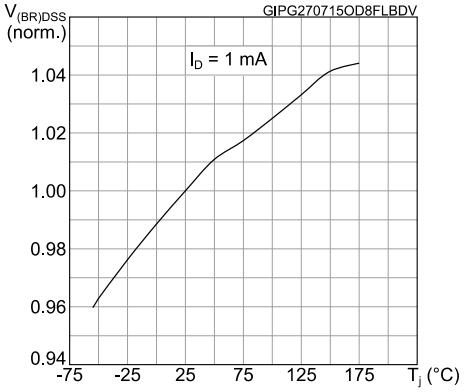
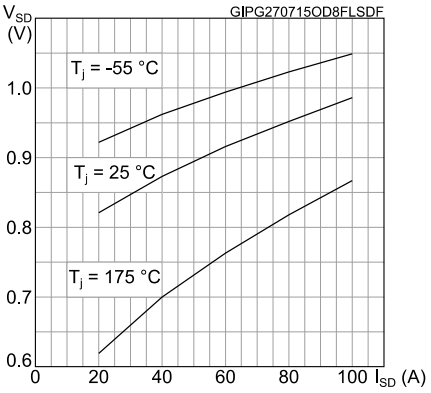


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

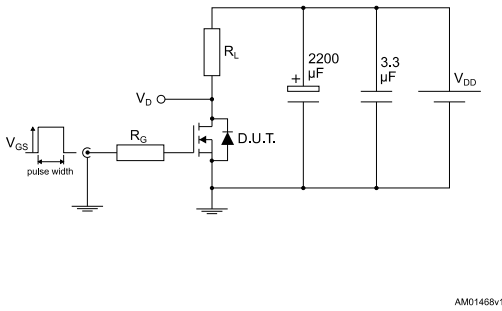


Figure 14: Test circuit for gate charge behavior

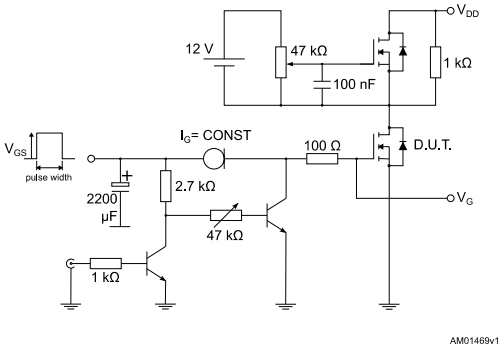


Figure 15: Test circuit for inductive load switching and diode recovery times

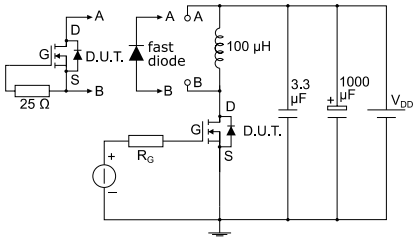


Figure 16: Unclamped inductive load test circuit

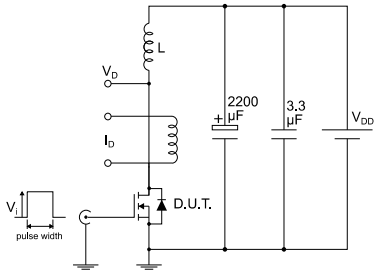


Figure 17: Unclamped inductive waveform

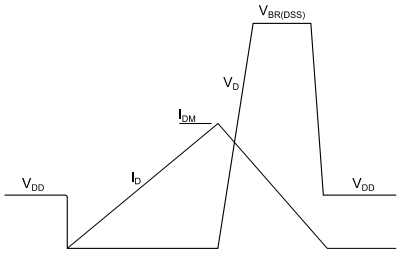
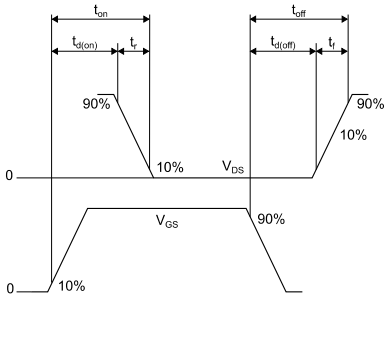


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

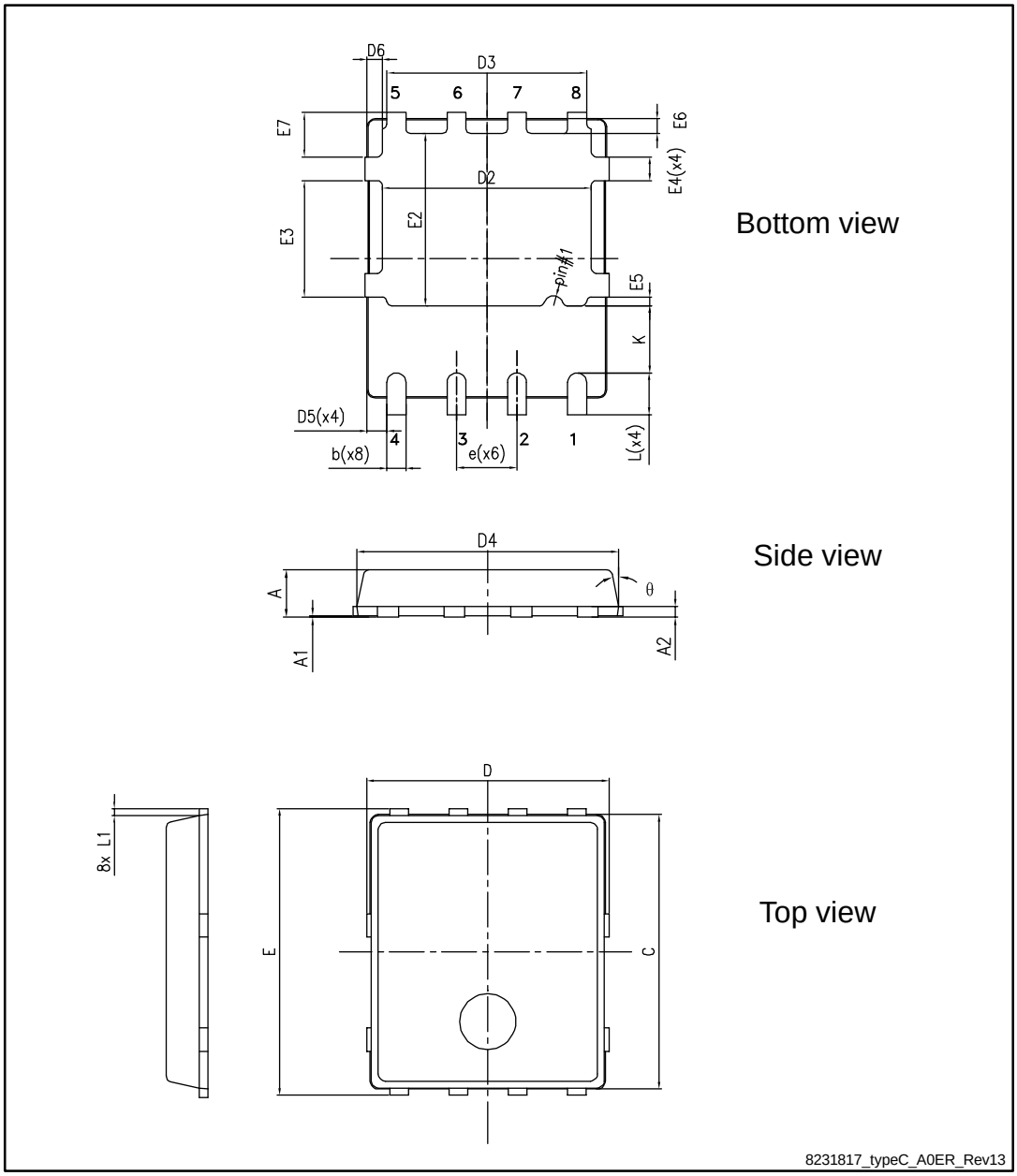
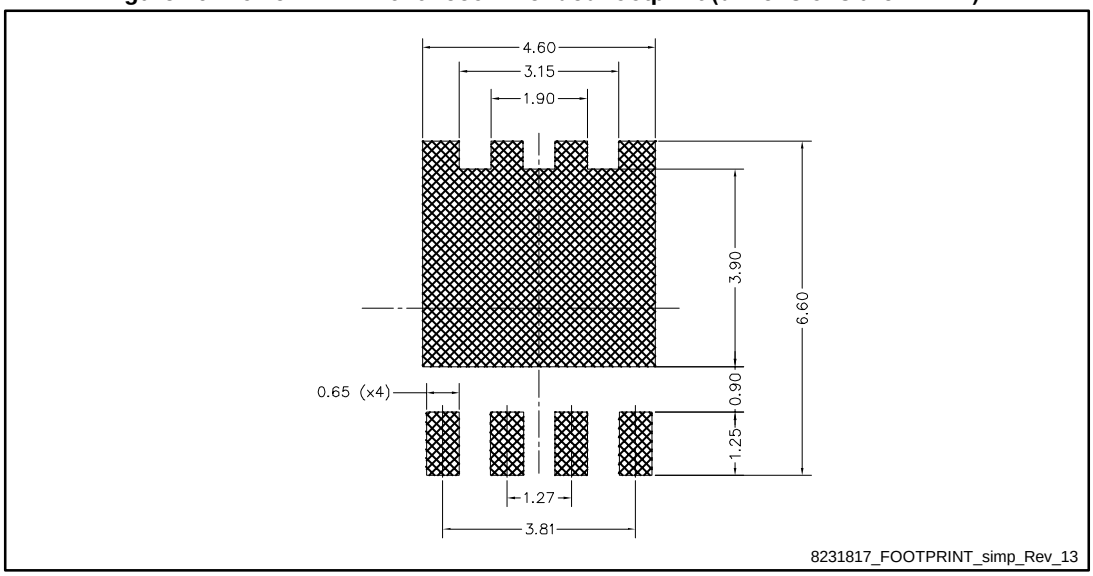


Table 8: PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.450
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.715		1.015
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

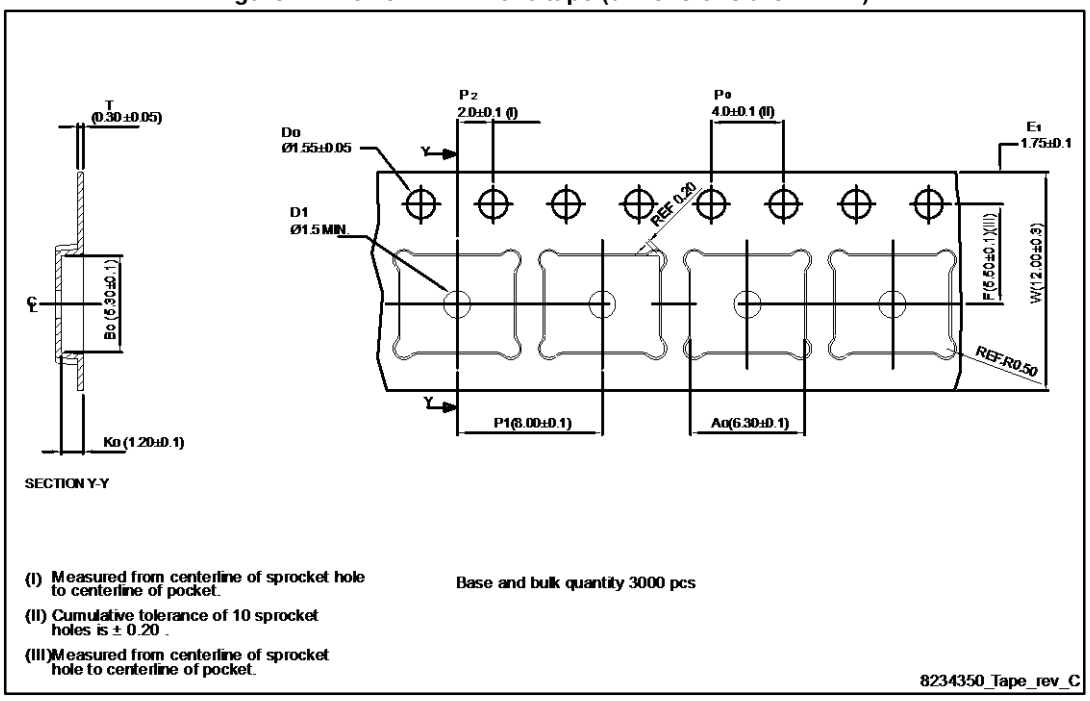


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

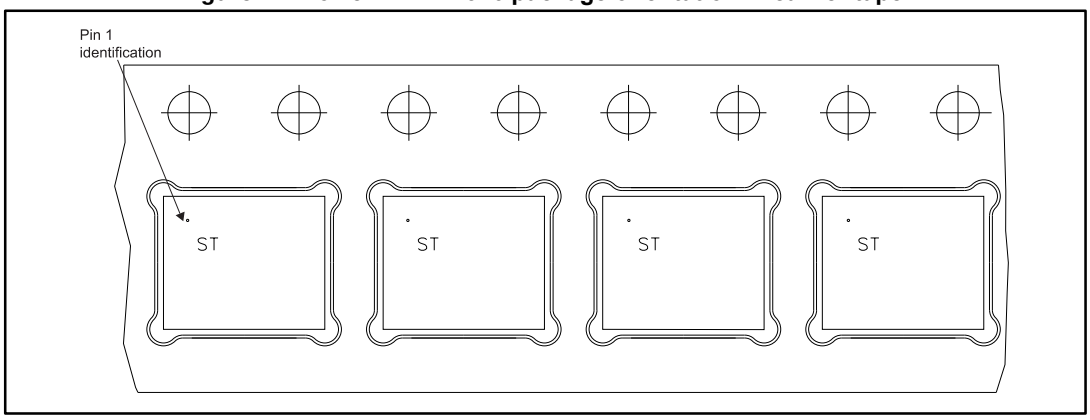
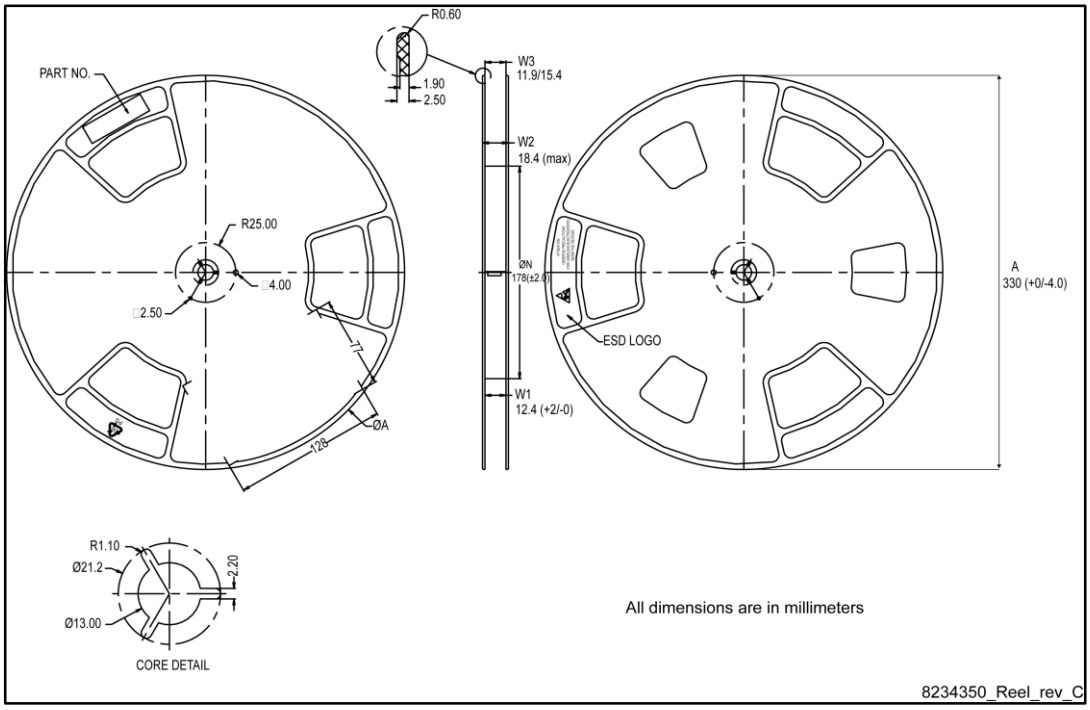


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
09-Dec-2014	1	First release.
27-Jul-2015	2	Text and formatting changes throughout document. Datasheet status promoted from preliminary data to production data. In section Electrical characteristics: - updated tables Dynamic, Switching times and Source-drain diode - added section Electrical characteristics (curves)
25-Jan-2016	3	Inserted R_G parameter in Dynamic.
09-Feb-2016	4	Updated *Table 4: "Static"* and *Section 4.1: "PowerFLAT™ 5x6 type C package information"*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

STMicroelectronics:

STL120N8F7