

P-channel 30 V, 0.024 Ω typ., 6 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 3.3 x 3.3 package

Datasheet - production data

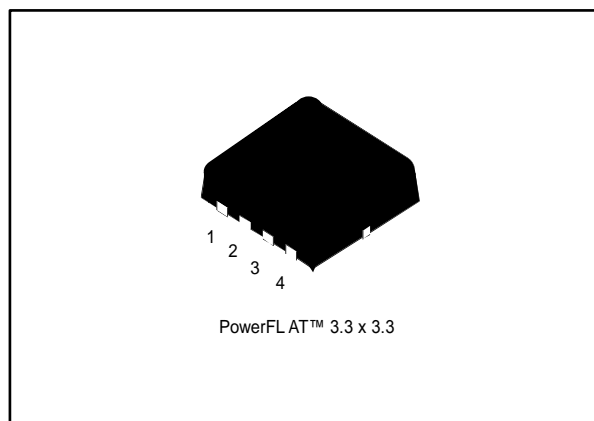
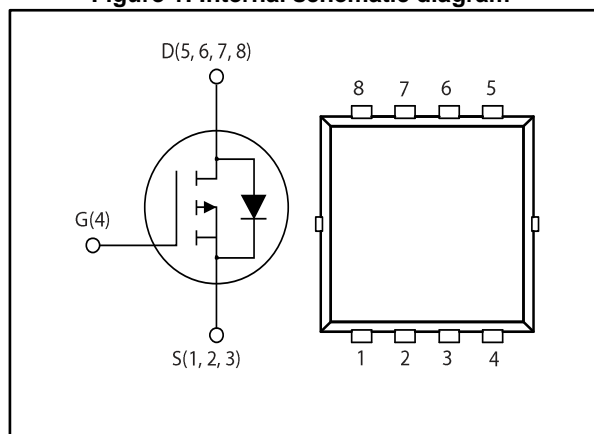


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STL6P3LLH6	30 V	0.03 Ω	6 A	2.9 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications


- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL6P3LLH6	6P3L	PowerFLAT™ 3.3 x 3.3	Tape and reel

 For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves) 6
- 3 Test circuits 8**
- 4 Package mechanical data 9**
 - 4.1 PowerFLAT™ 3.3 x 3.3 type C package information 9
 - 4.2 PowerFLAT™ 3.3 x 3.3 type F package information..... 11
- 5 Revision history 14**



1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.8	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.9	W
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

Notes:

⁽¹⁾The value is rated according $R_{thj-pcb}$.

⁽²⁾Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.50	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	42.8	$^\circ\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1inch², 2oz Cu, t<10 sec.



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 30\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 30\text{ V}$ $T_C = 125\text{ }^\circ\text{C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		0.024	0.03	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 3\text{ A}$		0.038	0.05	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$	-	1450	-	pF
C_{oss}	Output capacitance		-	178	-	pF
C_{rss}	Reverse transfer capacitance		-	120	-	pF
Q_g	Total gate charge	$V_{DD} = 24\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 4.5\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load")	-	12	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}, I_D = 3\text{ A}$ $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	21	-	ns



For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	$I_{SD} = 6 \text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 6 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 16 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	15		ns
Q_{rr}	Reverse recovery charge		-	6.5		nC
I_{RRM}	Reverse recovery current		-	0.9		A

2.1 Electrical characteristics (curves)

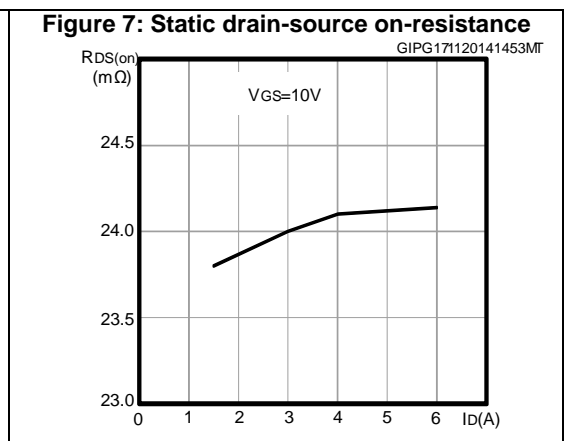
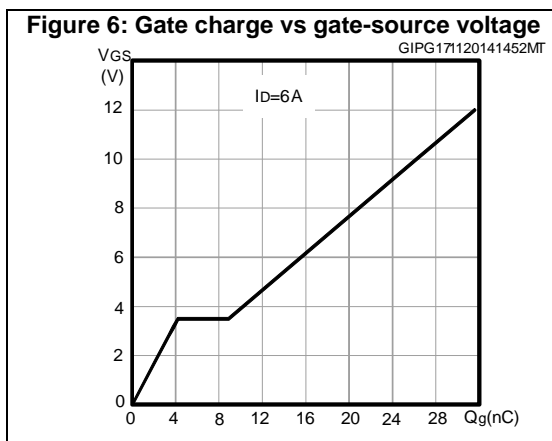
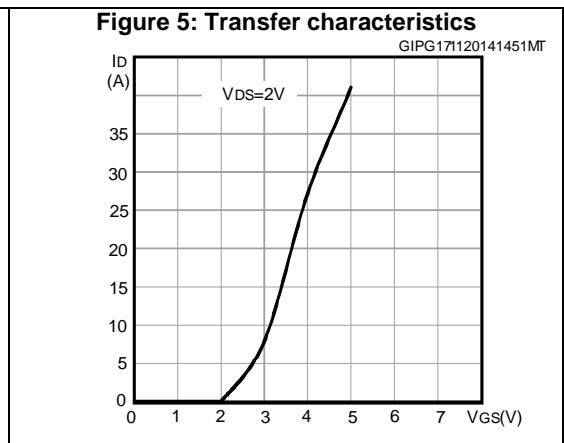
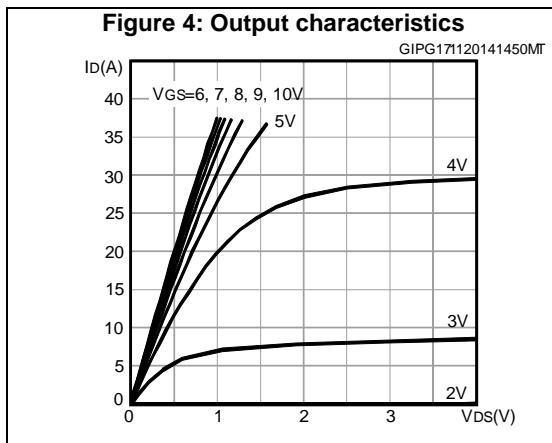
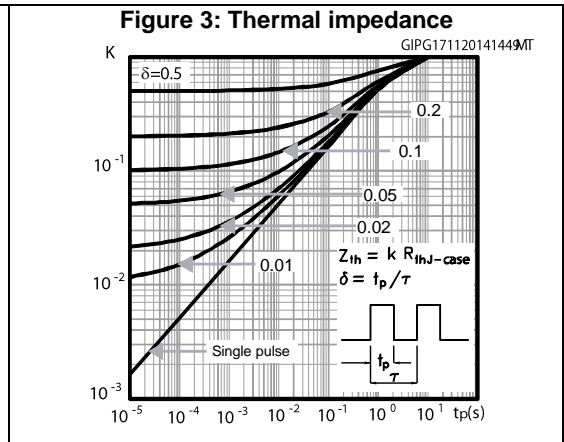
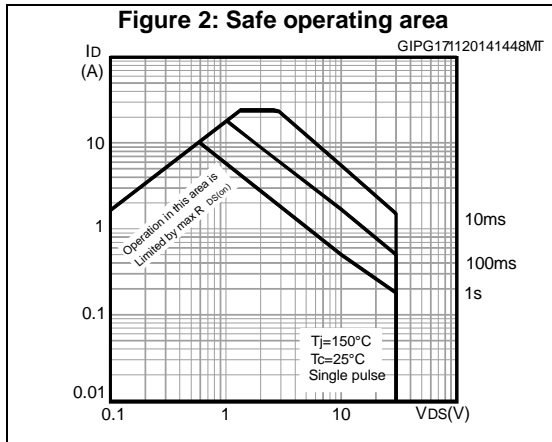


Figure 8: Capacitance variations

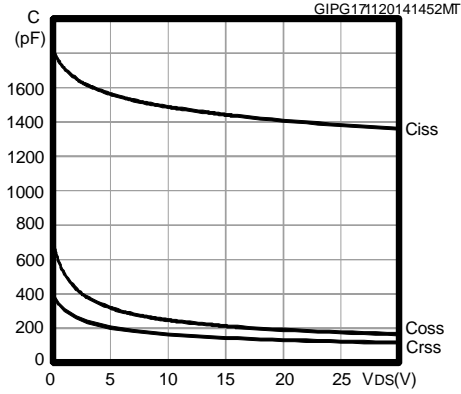


Figure 9: Normalized gate threshold voltage vs temperature

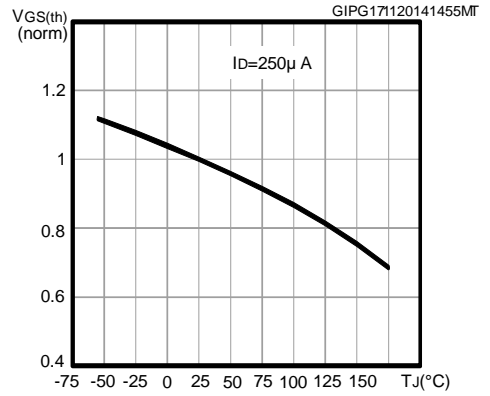


Figure 10: Normalized on-resistance vs temperature

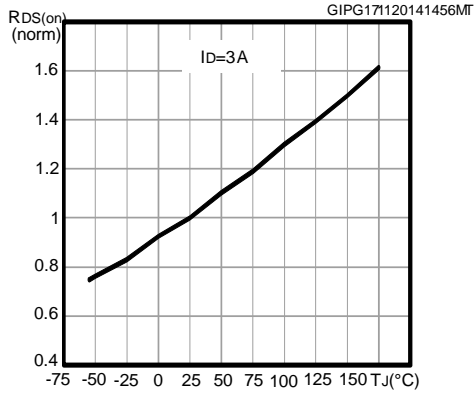


Figure 11: Normalized VDS vs temperature

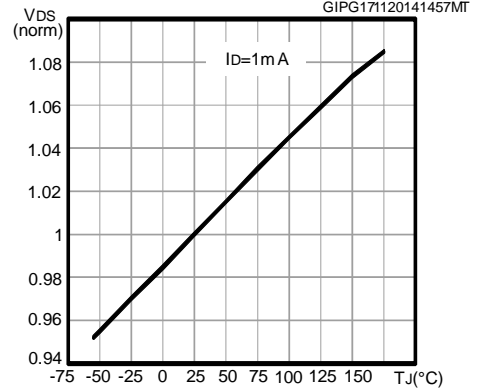
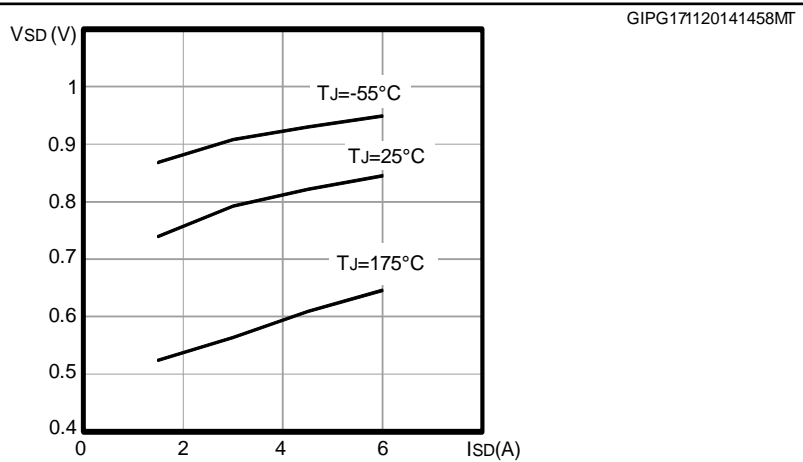


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

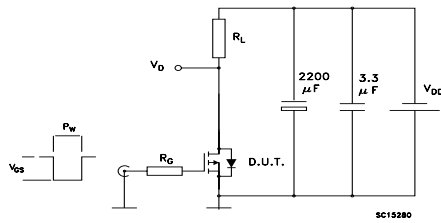


Figure 14: Gate charge test circuit

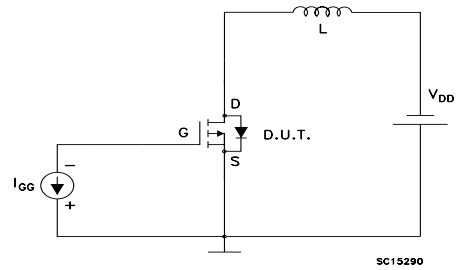
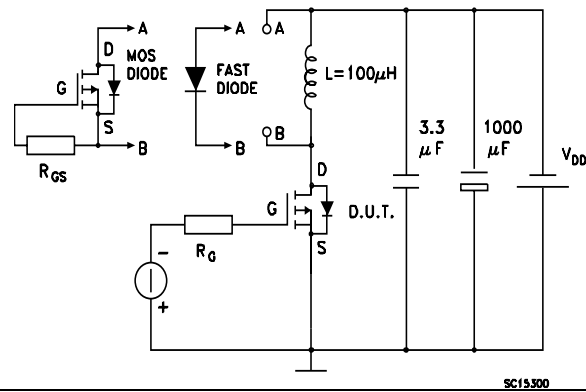


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 3.3 x 3.3 type C mechanical data

Figure 16: PowerFLAT™ 3.3 x 3.3 type C drawing

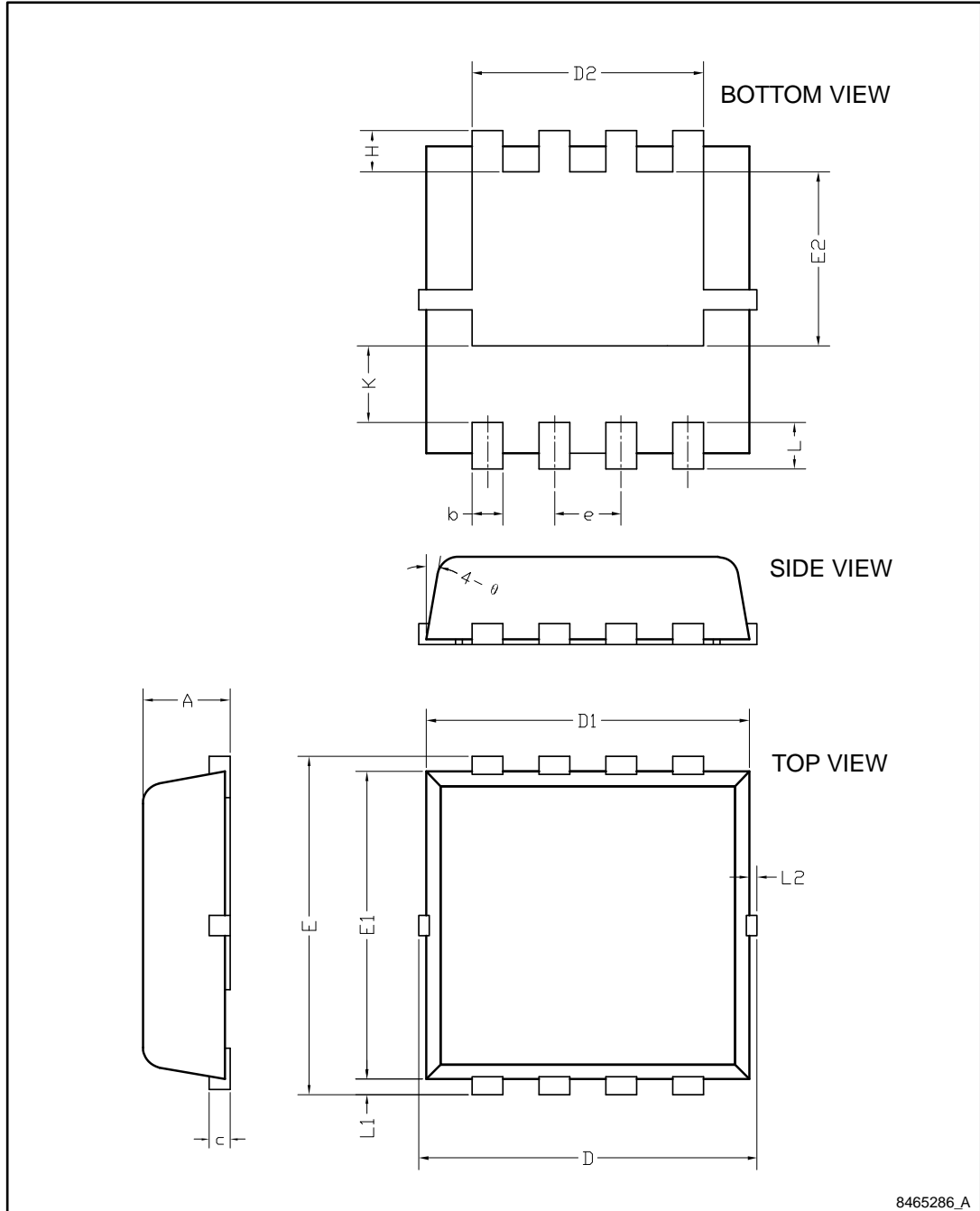
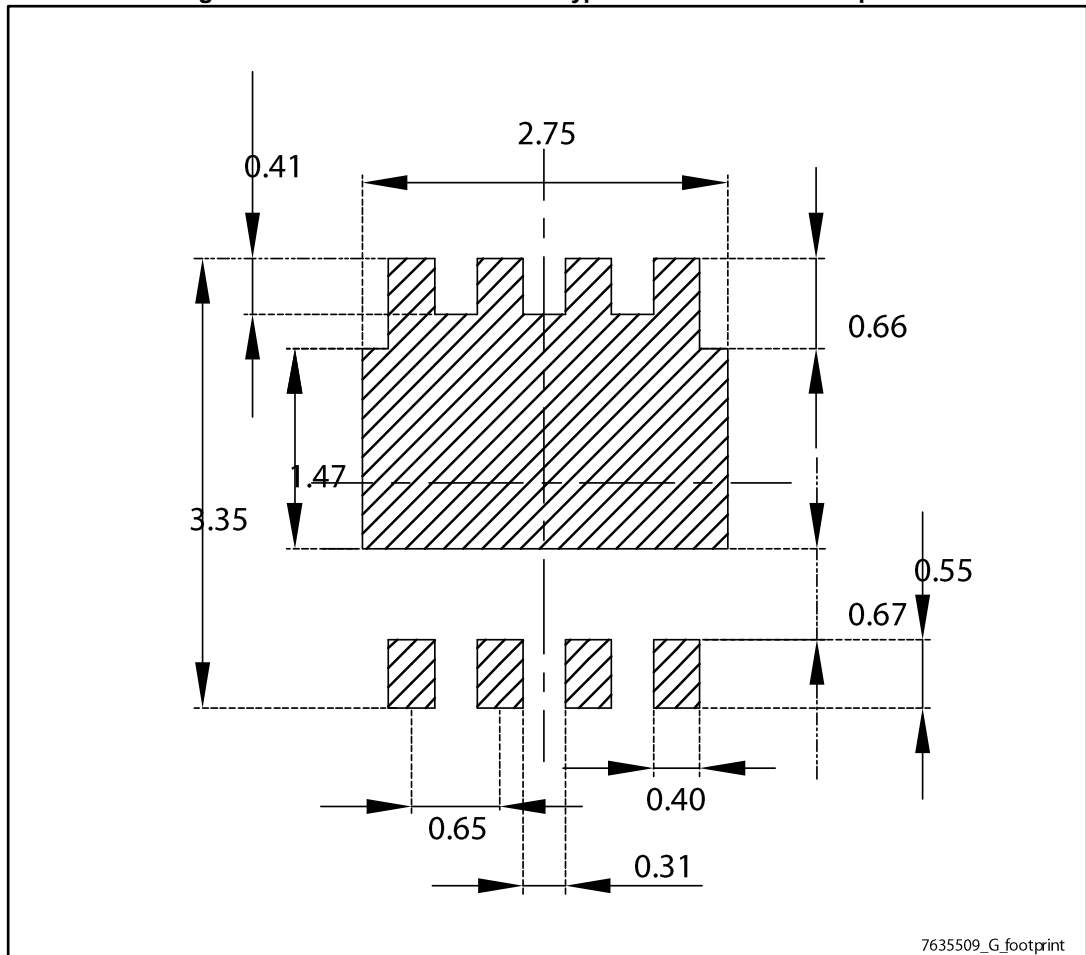


Table 8: PowerFLAT™ 3.3 x 3.3 type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A3		0.20	
b	0.23		0.38
D	3.20	3.30	3.40
D2	2.50		2.75
E	3.20	3.30	3.40
E2	1.25		1.50
e		0.65	
L	0.30		0.50

Figure 17: PowerFLAT™ 3.3 x 3.3 type C recommended footprint



4.2 PowerFLAT™ 3.3 x 3.3 type F mechanical data

Figure 18: PowerFLAT™ 3.3 x 3.3 type F drawing

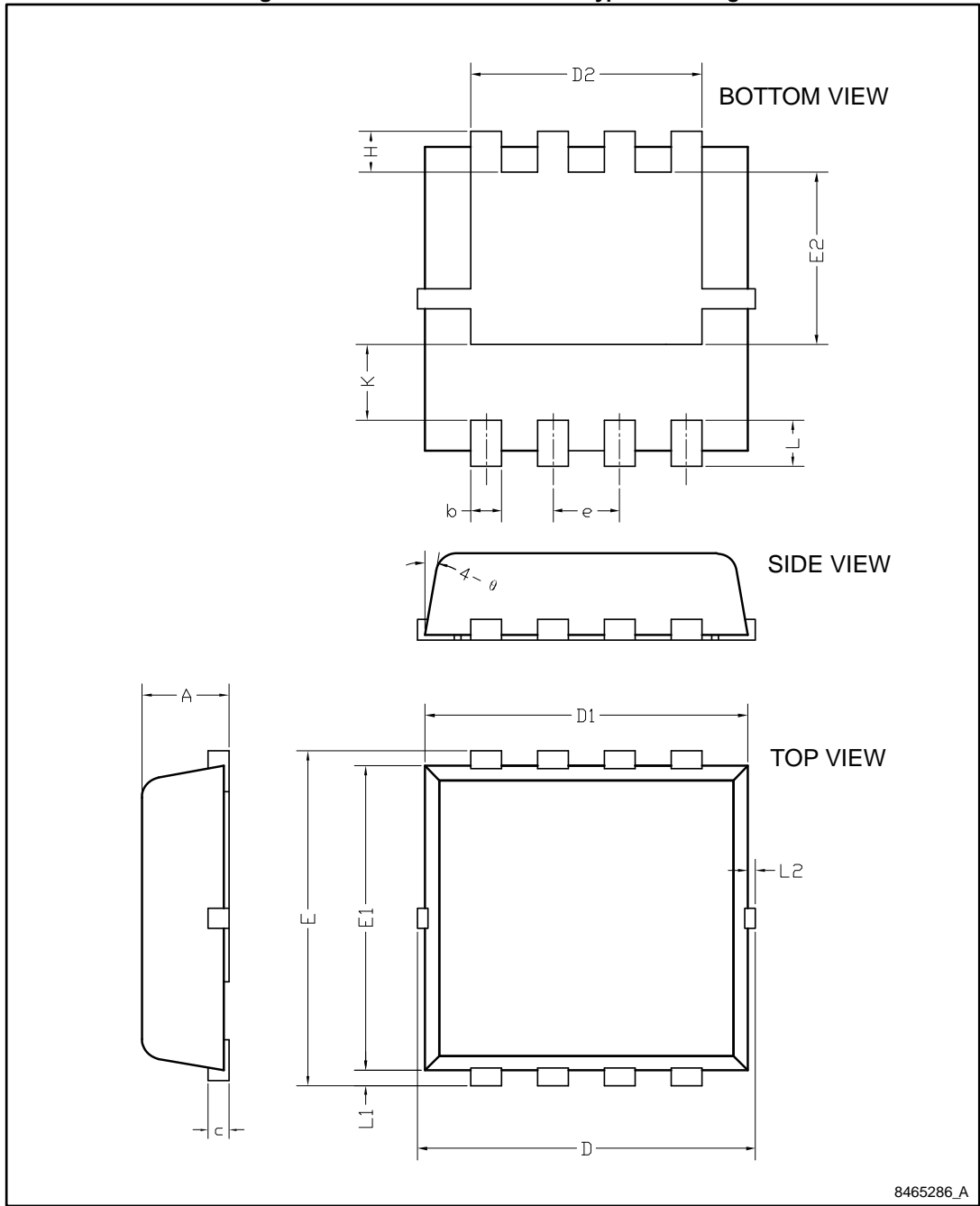
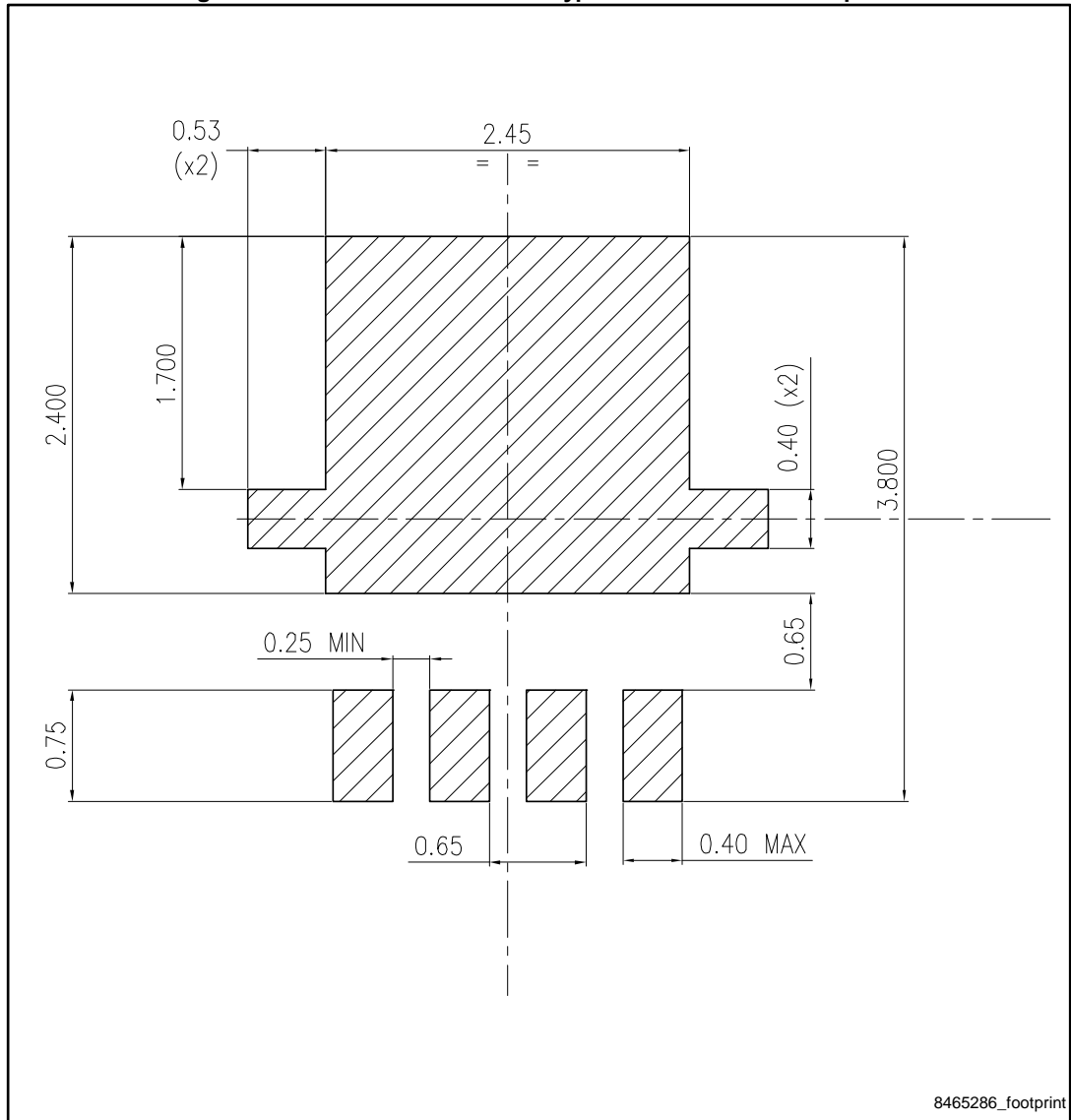


Table 9: PowerFLAT™ 3.3 x 3.3 type F mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
J	8°	10°	12°

Figure 19: PowerFLAT™ 3.3 x 3.3 type F recommended footprint



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
04-Mar-2013	1	First release.
28-Nov-2013	2	<ul style="list-style-type: none"> • Modified: P_{TOT} value, silhouette and not found in cover page • Modified: V_{GS} and P_{TOT} values in not found • Modified: $R_{thj-pcb}$ value and note ⁽¹⁾ in Table 3: "Thermal data" • Modified: I_{GSS} test conditions value • Modified: Q_g in Table 5: "Dynamic" • Added: Table 9: "PowerFLAT™ 3.3 x 3.3 type F mechanical data", Figure 18: "PowerFLAT™ 3.3 x 3.3 type F drawing" and Figure 19: "PowerFLAT™ 3.3 x 3.3 type F recommended footprint" • Minor text changes
26-Nov-2014	3	<p>Updated Figure 1: "Internal schematic diagram".</p> <p>Added Section 4.1: "PowerFLAT™ 3.3 x 3.3 type C package information" and Section 4.2: "PowerFLAT™ 3.3 x 3.3 type F package information".</p> <p>Minor text changes.</p>

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