



STP75NS04Z

N-channel Clamped - 7mΩ - 80A - TO-220
Fully protected MESH Overlay™ III Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STP75NS04Z	Clamped	< 11mΩ	80A

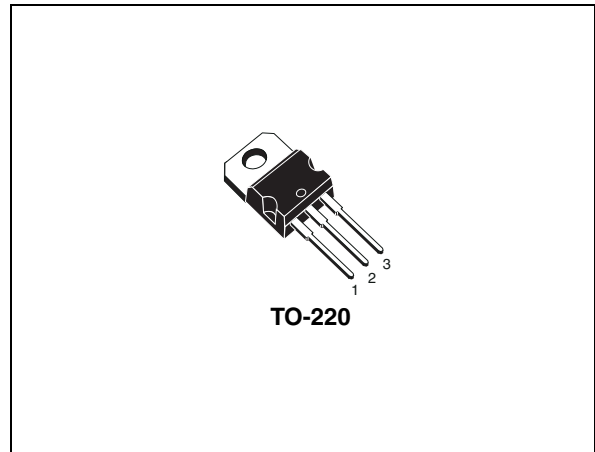
- Low capacitance and gate charge
- 100% avalanche tested
- 175°C maximum junction temperature

Description

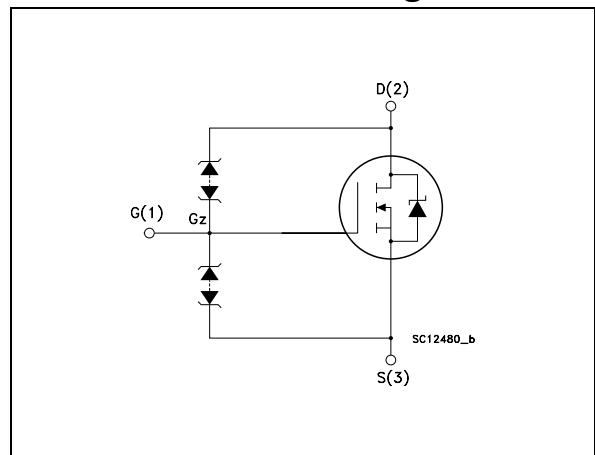
This fully clamped MOSFET is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout. The inherent benefits of a new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encoured in power tools. Any other application requiring extra ruggedness is also recommended.

Applications

- Switching application
- Power tools



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP75NS04Z	P75NS04Z	TO-220	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	Clamped	V
V_{DG}	Drain-gate voltage ($V_{GS} = 0$)	Clamped	V
V_{GS}	Gate-source voltage	Clamped	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	63	A
I_{DG}	Drain gate current (continuous)	± 50	mA
I_{GS}	Gate source current (continuous)	± 50	mA
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
	Derating factor	0.73	W/ $^\circ\text{C}$
V_{ESD}	Gate-source ESD (HBM-C=100pF, R=1.5K Ω)	± 8	kV
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Current limited by wire bonding
2. Pulse with limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	1.36	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=25\text{V}$)	470	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	33			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 16V$			1	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 10V$			2	μA
V_{GSS}	Gate threshold breakdown voltage	$I_{GS} = \pm 100\mu A$	18			V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 40A$		7	11	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 15A$		50		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 MHz,$ $V_{GS} = 0$		1860		pF
C_{oss}	Output capacitance			628		pF
C_{rss}	Reverse transfer capacitance			196		pF
Q_g	Total gate charge	$V_{DD} = 20V, I_D = 80 A,$		50		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10 V$		14		nC
Q_{gd}	Gate-drain charge	(see Figure 13)		16		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching on/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=20V, I_D=40A$ $R_G=4.7\ \Omega, V_{GS}=10V,$ (see Figure 12)		16 248		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=20V, I_D=40A$ $R_G=4.7\ \Omega, V_{GS}=10V,$ (see Figure 12)		53 85		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=80A, V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=80A, di/dt = 100A/\mu s,$		53		ns
Q_{rr}	Reverse recovery charge	$V_{DD}=30V, T_j=150^\circ C$		91		nC
I_{RRM}	Reverse recovery current	(see Figure 17)		3.4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

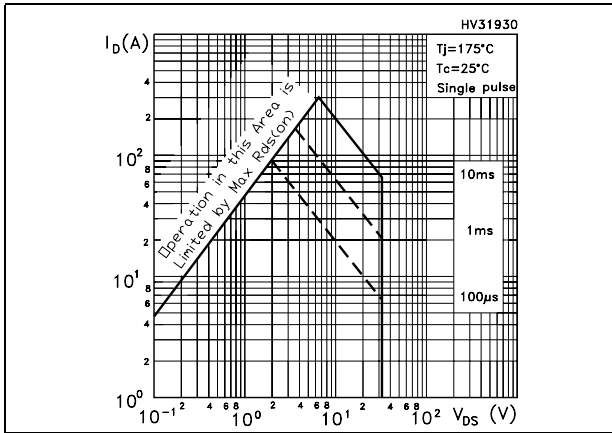


Figure 2. Thermal impedance

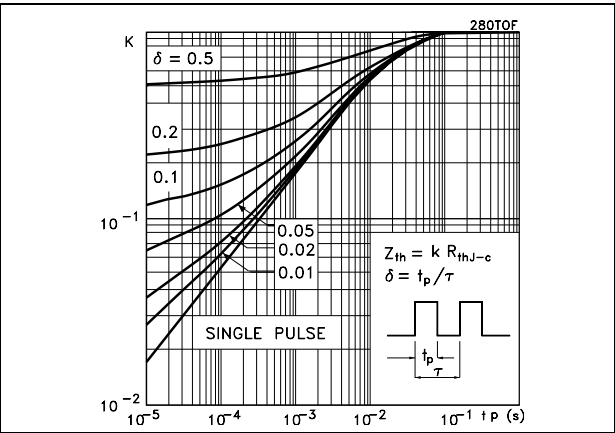


Figure 3. Output characteristics

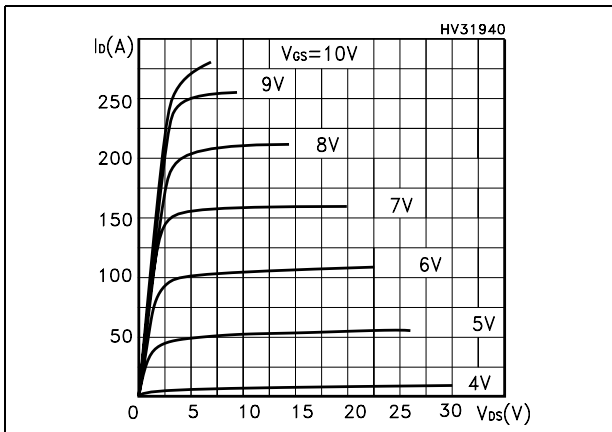


Figure 4. Transfer characteristics

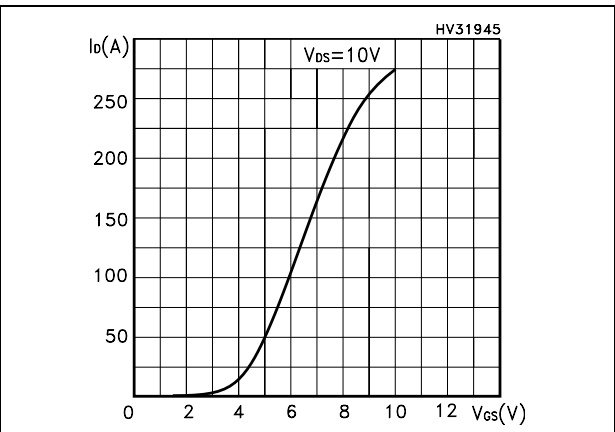


Figure 5. Normalized $B_{V_{DS}}$ vs temperature

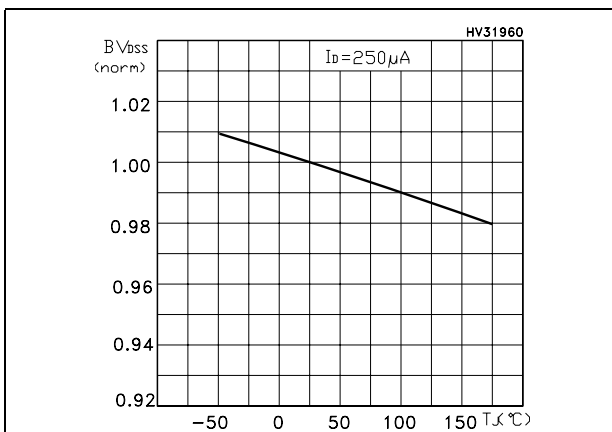


Figure 6. Static drain-source on resistance

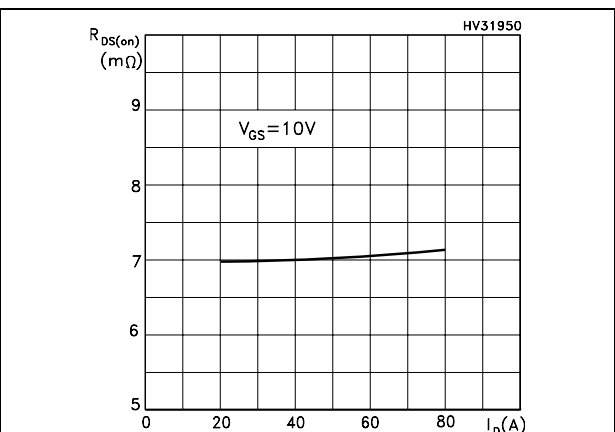


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

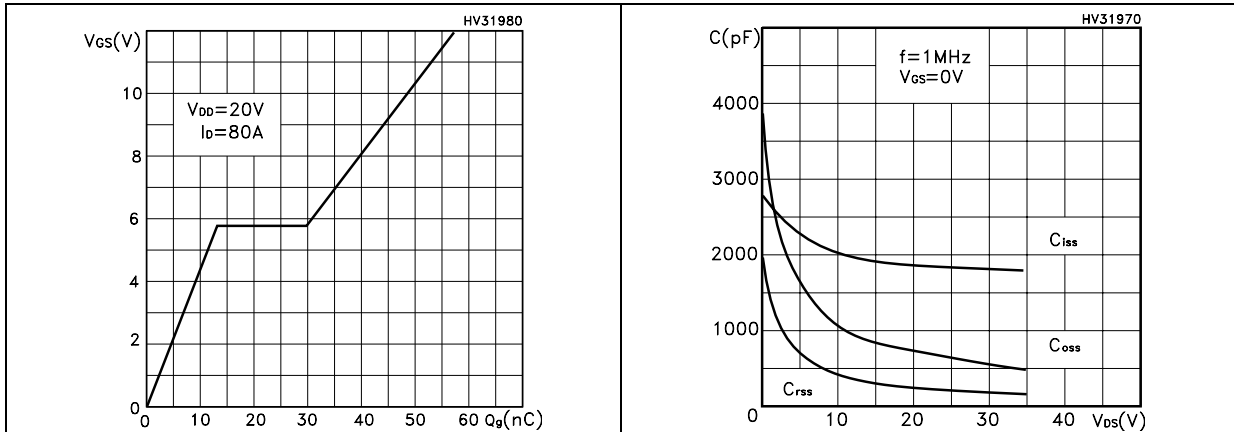


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

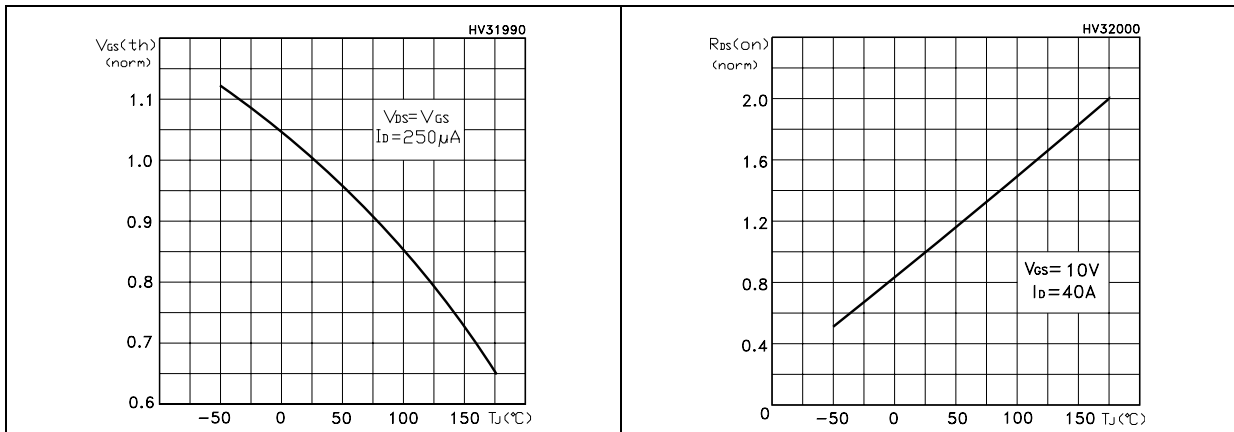
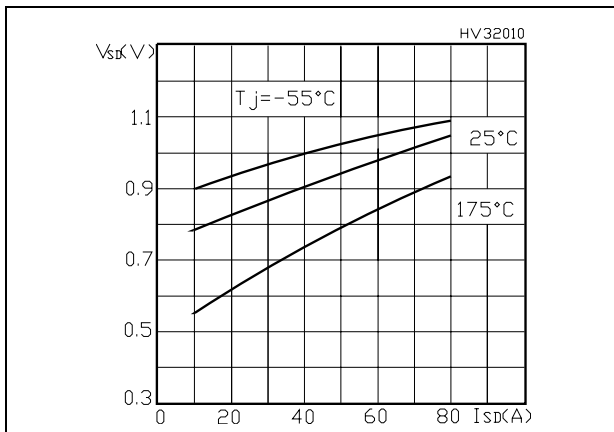


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

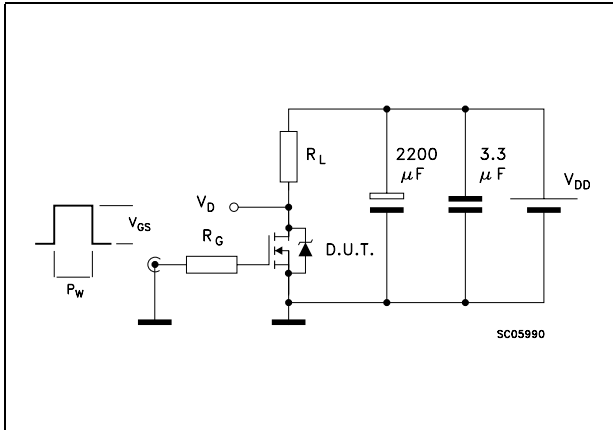


Figure 13. Gate charge test circuit

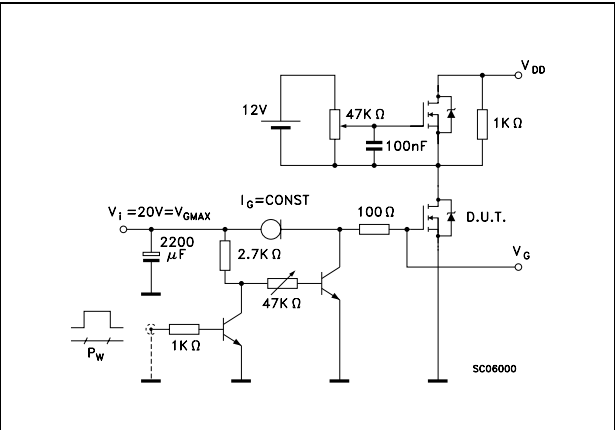


Figure 14. Test circuit for inductive load switching and diode recovery times

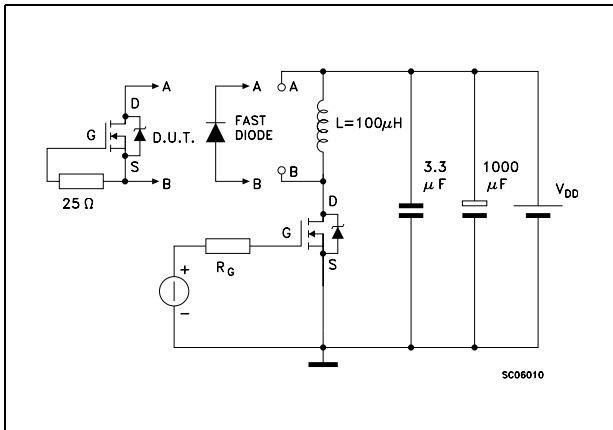


Figure 15. Unclamped inductive load test circuit

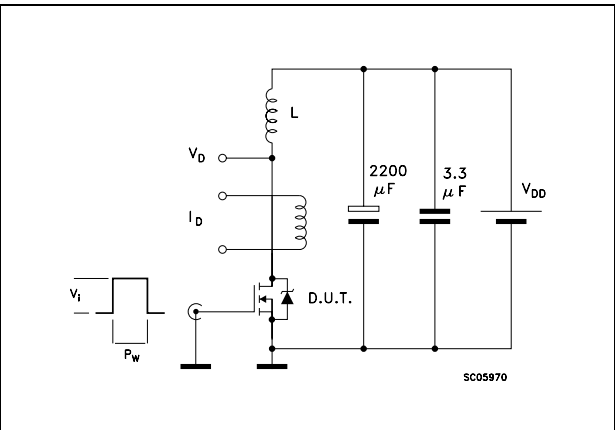


Figure 16. Unclamped inductive waveform

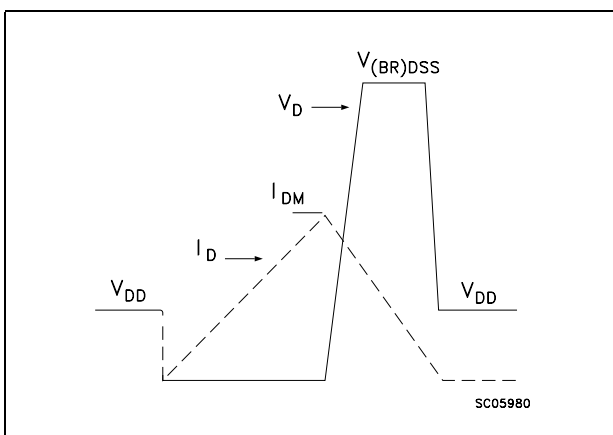
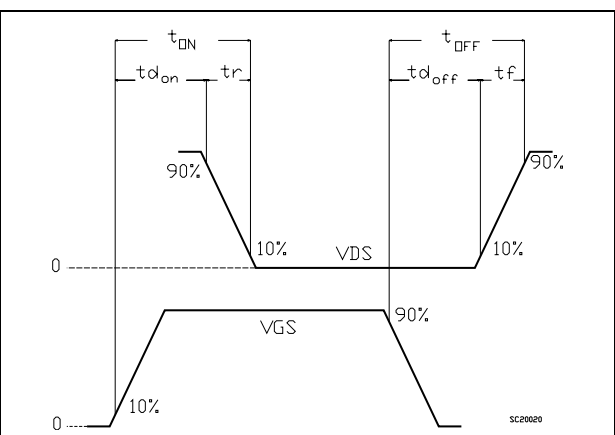


Figure 17. Switching time waveform

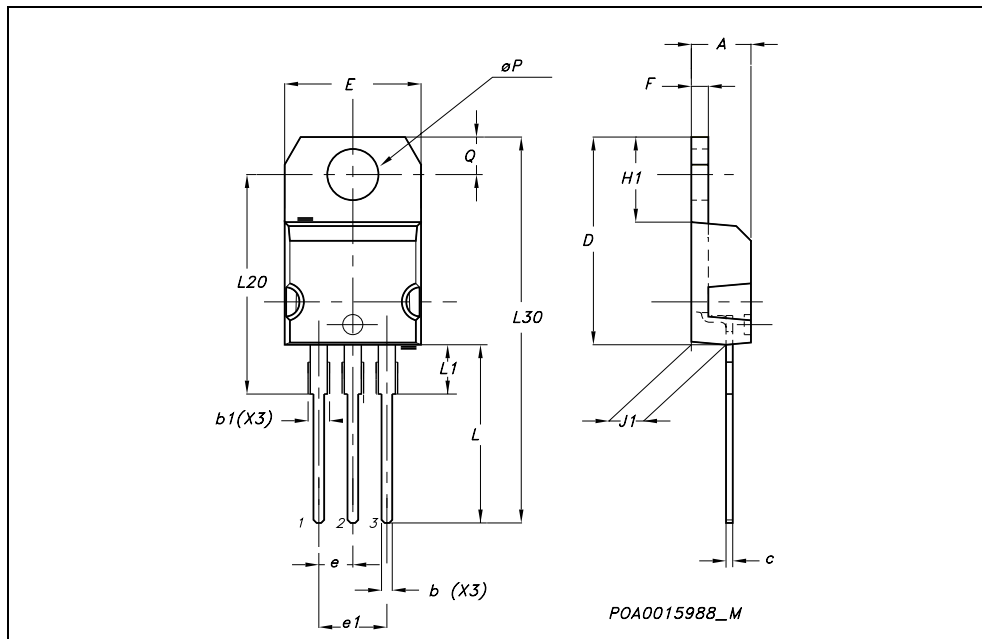


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision history

Table 8. Revision history

Date	Revision	Changes
06-Jun-2006	1	First release

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