



STP90N55F4

N-channel 55 V, 0.0064 Ω , 90 A, TO-220
STripFET™ DeepGATE™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STP90N55F4	55 V	< 0.008 Ω	90 A

- Exceptional dv/dt capability
- Extremely low on-resistance R_{DS(on)}
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using ST's STripFET™ DeepGATE™ technology. The device has a new gate structure and is specially designed to minimize on-state resistance to provide superior switching performance.

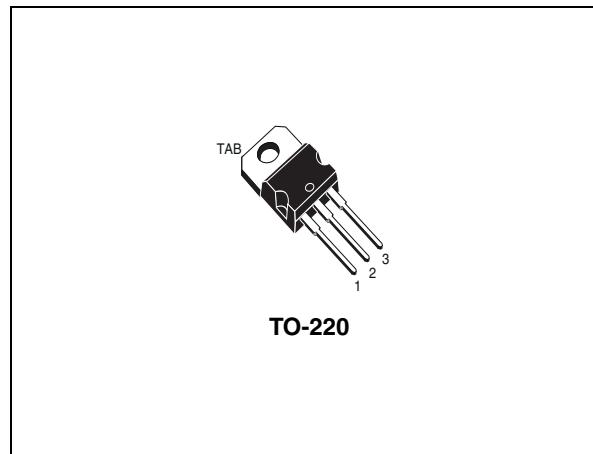


Figure 1. Internal schematic diagram

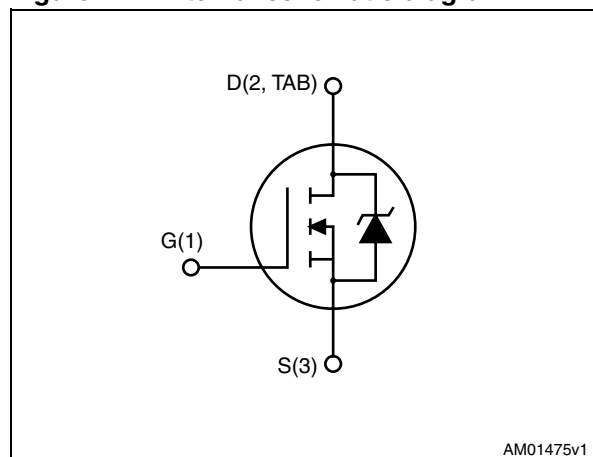


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STP90N55F4	90N55F4	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	55	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	90	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	65	A
$I_{DM}^{(1)}$	Drain current (pulsed)	360	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
	Derating factor	1	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	290	mJ
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 32.5\text{ A}$, $V_{DD} = 45\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage ($V_{GS} = 0$)	$I_D = 250\ \mu A$	55			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = 55\text{ V}$ $V_{DS} = 55\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 45\text{ A}$		0.0064	0.008	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			4800		pF
C_{oss}	Output capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	350	-	pF
C_{rss}	Reverse transfer capacitance			210		pF
Q_g	Total gate charge	$V_{DD} = 27.5\text{ V}, I_D = 90\text{ A},$ $V_{GS} = 10\text{ V}$		90		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$ <i>Figure 14</i>		25		nC
Q_{gd}	Gate-drain charge			26		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 27.5\text{ V}, I_D = 90\text{ A}$ $R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$ <i>Figure 13</i>		20		ns
t_r	Rise time			60		ns
$t_{d(off)}$	Turn-off-delay time	$V_{DD} = 27.5\text{ V}, I_D = 90\text{ A},$ $R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$ <i>Figure 13</i>		55		ns
t_f	Fall time			30		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		90	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		360	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 90 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 90 \text{ A}$, $V_{DD} = 44 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ Figure 15	-	50		ns
Q_{rr}	Reverse recovery charge			105		nC
I_{RRM}	Reverse recovery current			4		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

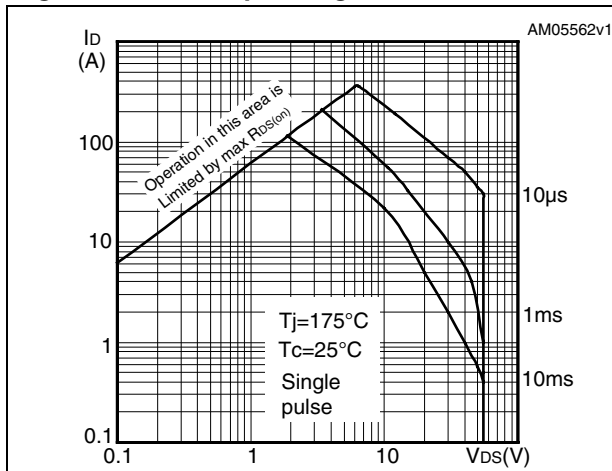


Figure 3. Thermal impedance

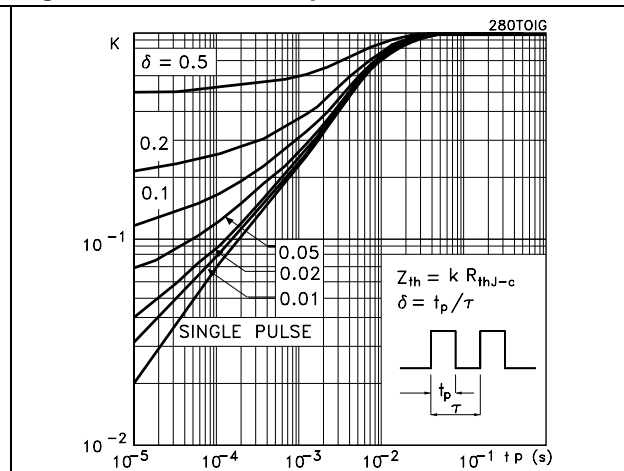


Figure 4. Output characteristics

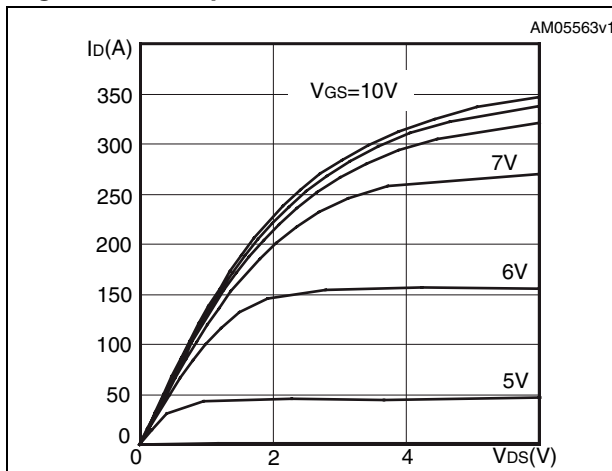


Figure 5. Transfer characteristics

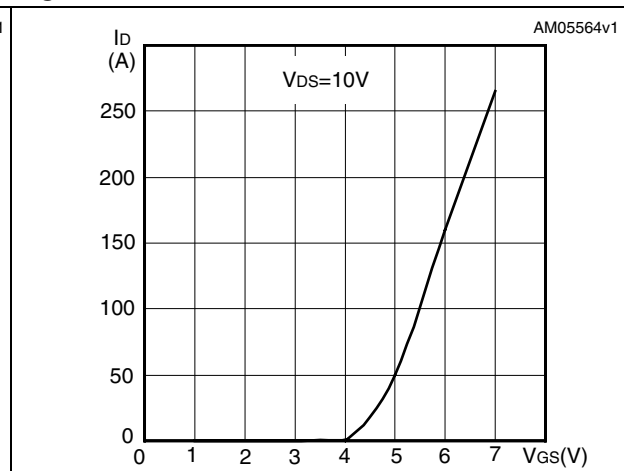


Figure 6. Normalized BV_{DSS} vs temperature

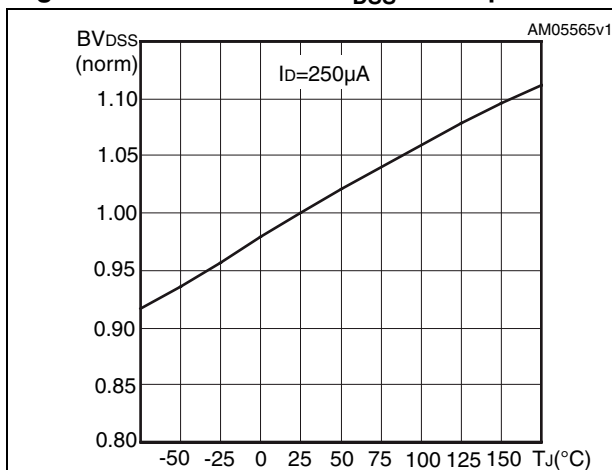


Figure 7. Static drain-source on resistance

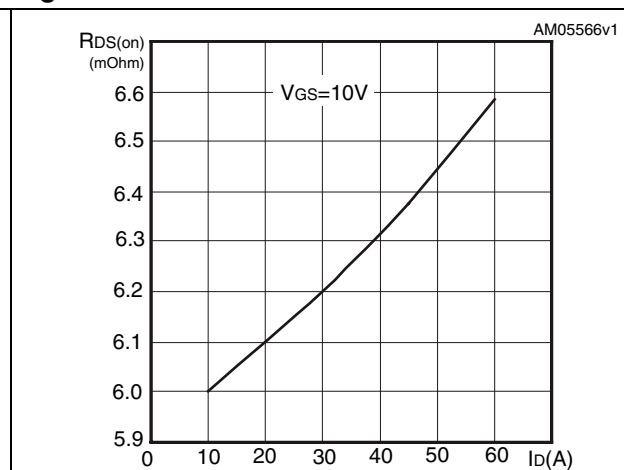


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

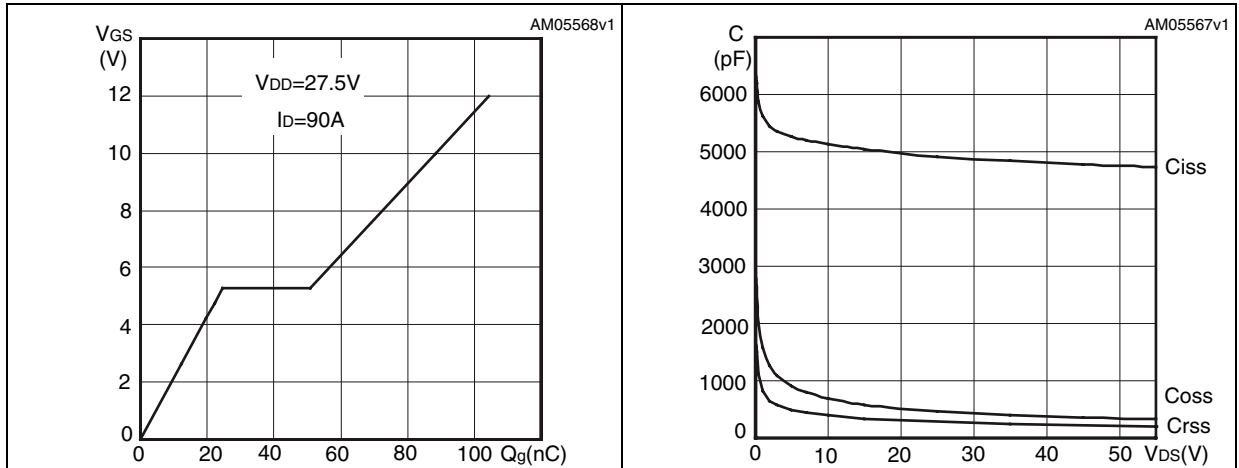


Figure 10. Normalized on resistance vs temperature

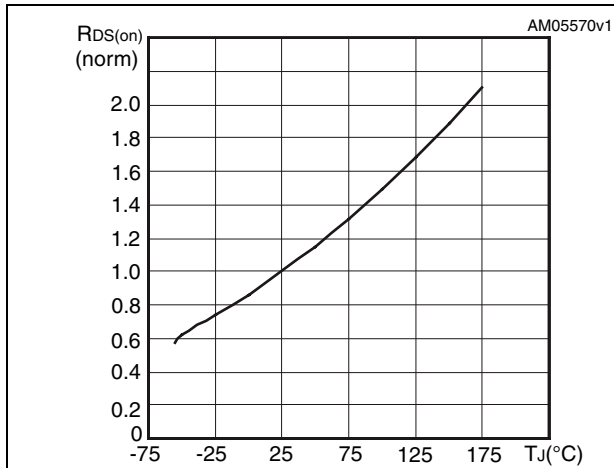


Figure 11. Normalized gate threshold voltage vs temperature

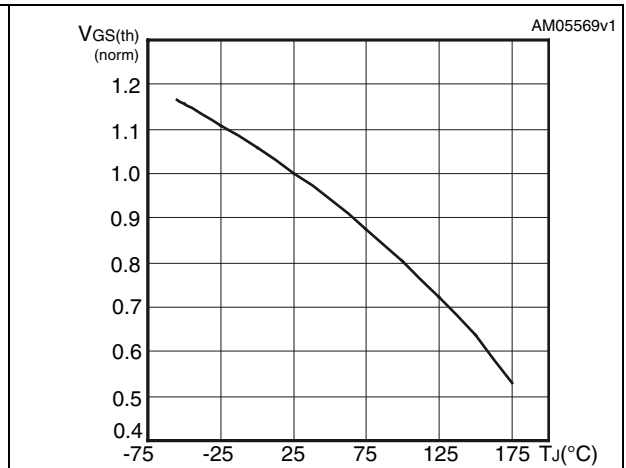
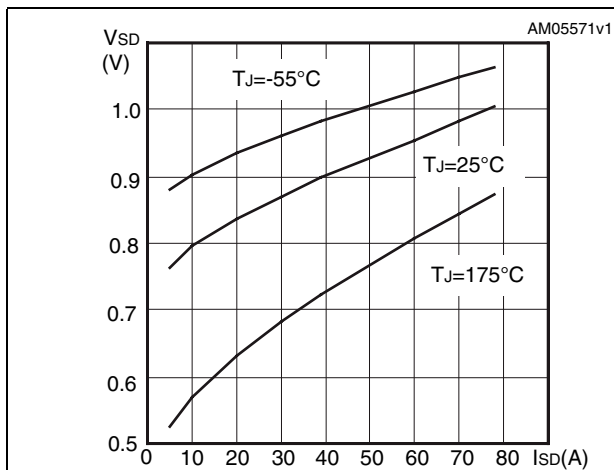


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

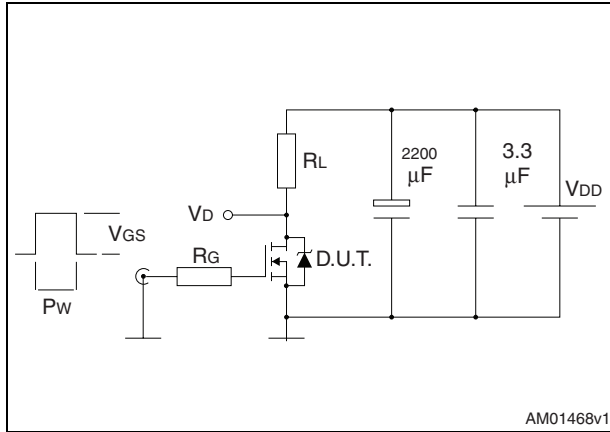


Figure 14. Gate charge test circuit

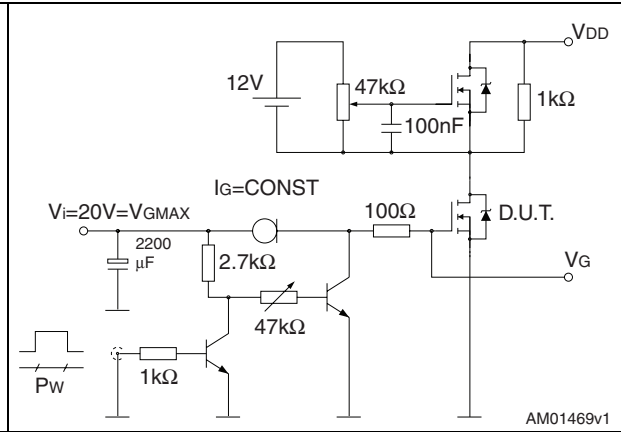


Figure 15. Test circuit for inductive load switching and diode recovery times

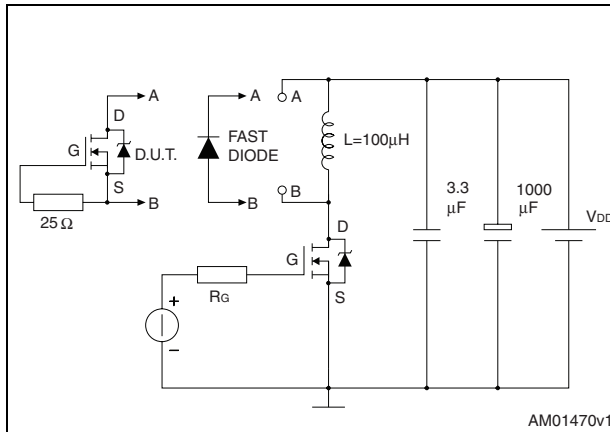


Figure 16. Unclamped inductive load test circuit

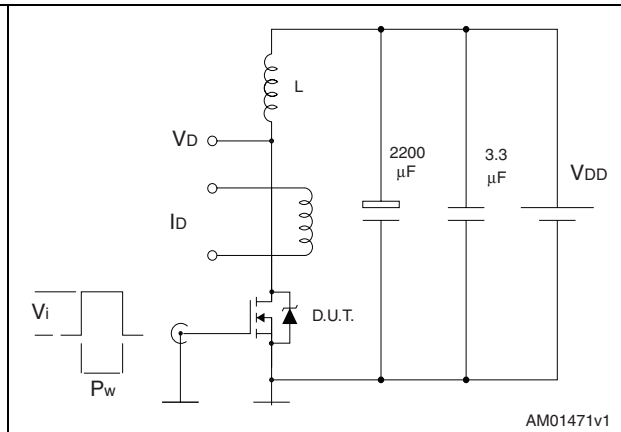


Figure 17. Unclamped inductive waveform

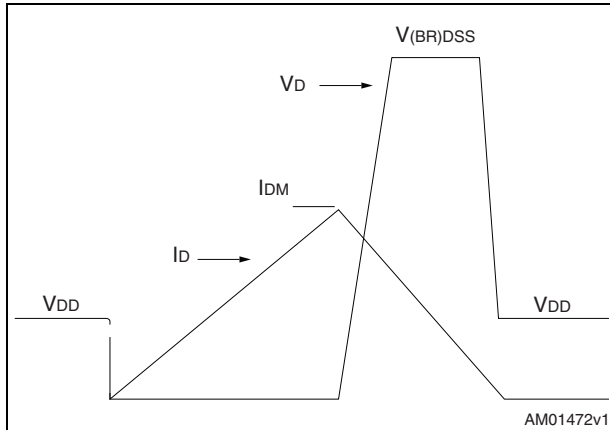
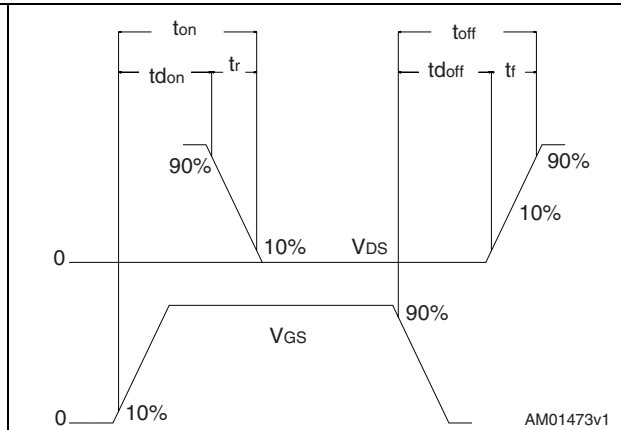


Figure 18. Switching time waveform



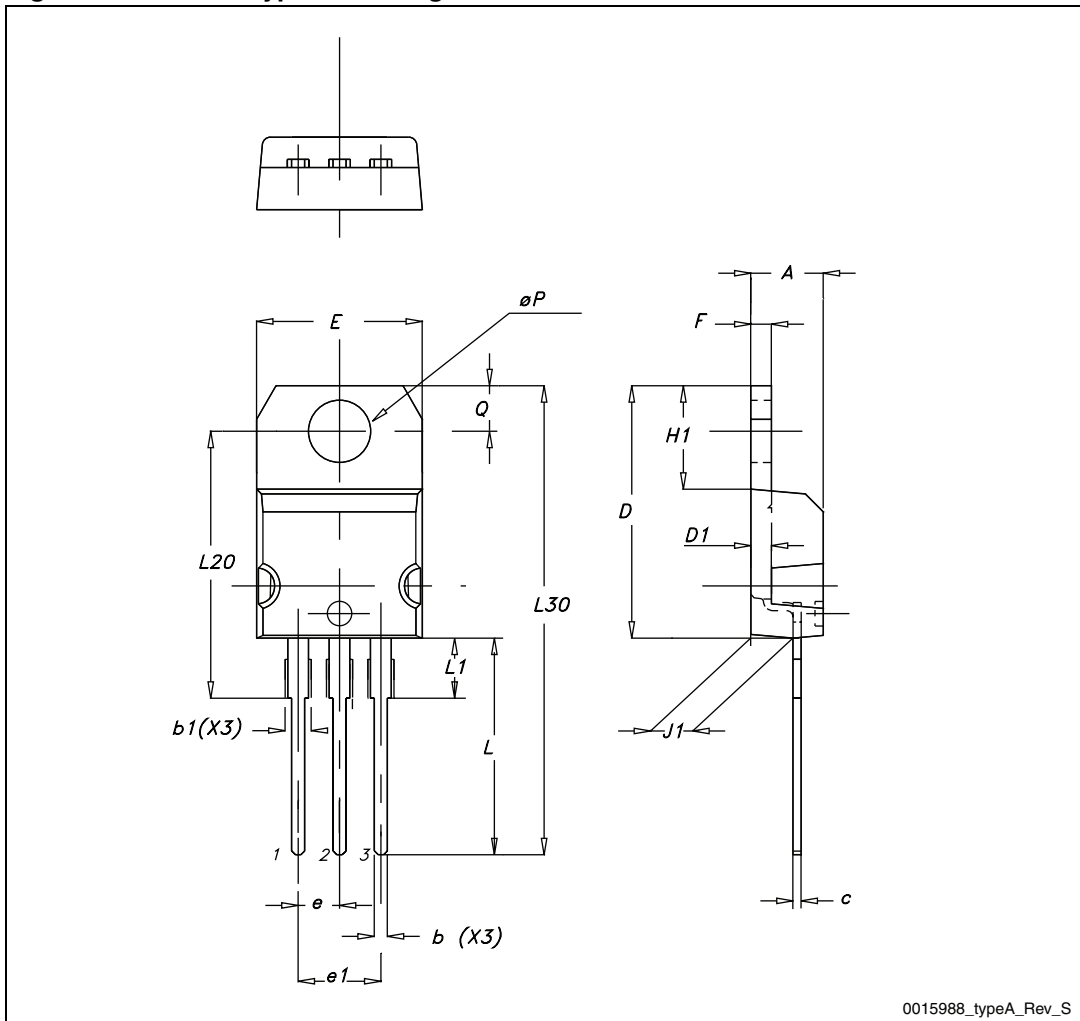
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 19. TO-220 type A drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Aug-2011	1	First release

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