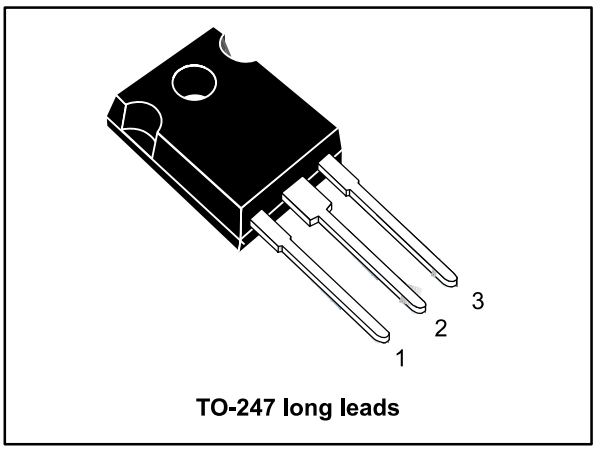
# STWA48N60M2

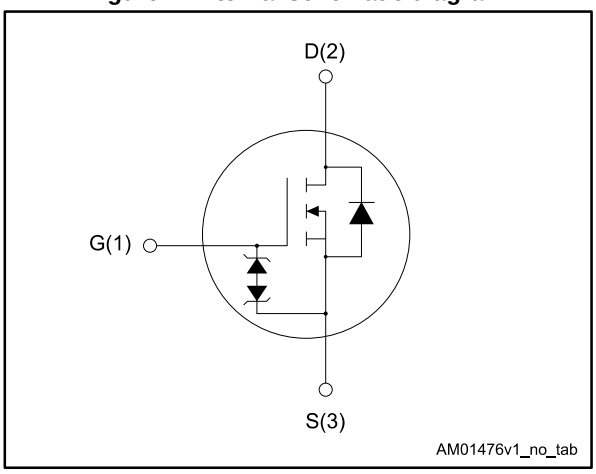
## N-channel 600 V, 0.06 Ω typ., 42 A MDmesh™ M2 Power MOSFET in a TO-247 long leads package

Datasheet - production data




**TO-247 long leads**

**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ @ $T_{Jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STWA48N60M2 | 650 V | 0.07 Ω | 42 A |

- Extremely low gate charge
- Excellent output capacitance ($C_{OSS}$) profile
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

**Table 1: Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STWA48N60M2 | 48N60M2 | TO-247 long leads | Tube |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 42 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 26 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 168 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 300 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt (3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Operating junction temperature | | |

**Notes:**

(1)Pulse width limited by safe operating area.

(2)$I_{SD}$ ≤ 42 A, di/dt ≤ 400 A/µs; $V_{DSpeak}$ < $V_{(BR)DSS}$, $V_{DD}$=400 V.

(3)$V_{DS}$ ≤ 480 V

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.42 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 50 | °C/W |

**Table 4: Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 7 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$=25°C, $I_D$= $I_{AR}$; $V_{DD}$=50) | 4500 | mJ |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 5: On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0, $I_D$ = 1 mA | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0, $V_{DS}$ = 600 V | | | 1 | µA |
| | | $V_{GS}$ = 0, $V_{DS}$ = 600 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0, $V_{GS}$ = ± 25 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 21 A | | 0.06 | 0.07 | Ω |

**Table 6: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0, $V_{DS}$ = 100 V, f = 1 MHz, | - | 3060 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 143 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 4.3 | - | pF |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{GS}$ = 0, $V_{DS}$ = 0 to 480 V | - | 630 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 | - | 4.6 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 42 A, $V_{GS}$ = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*) | - | 70 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 10.5 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 31 | - | nC |

**Notes:**

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 21 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for resistive load switching times"*) | - | 18.5 | - | ns |
| $t_r$ | Rise time | | - | 17 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 13 | - | ns |
| $t_f$ | Fall time | | - | 119 | - | ns |

**Table 8: Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 42 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 168 | A |
| $V_{SD}$(2) | Forward on voltage | $V_{GS}$ = 0, $I_{SD}$ = 21 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 42 A, di/dt = 100 A/µs $V_{DD}$ = 60 V (see *Figure 17: "Unclamped inductive load test circuit"*) | - | 487 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 9.1 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 37.5 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 42 A, di/dt = 100 A/µs $V_{DD}$ = 60 V, $T_j$ = 150 °C (see *Figure 17: "Unclamped inductive load test circuit"*) | - | 605 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 12.5 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 41.5 | | A |

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

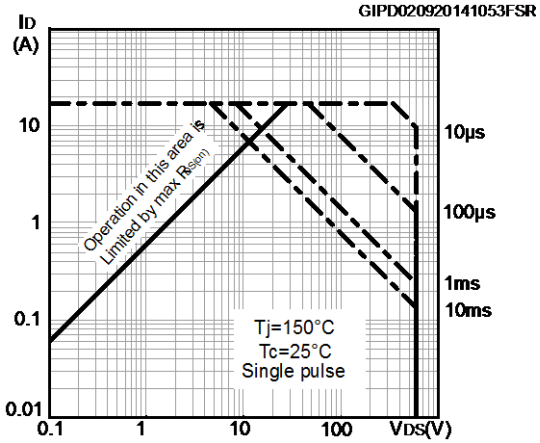



**Figure 3: Thermal impedance**

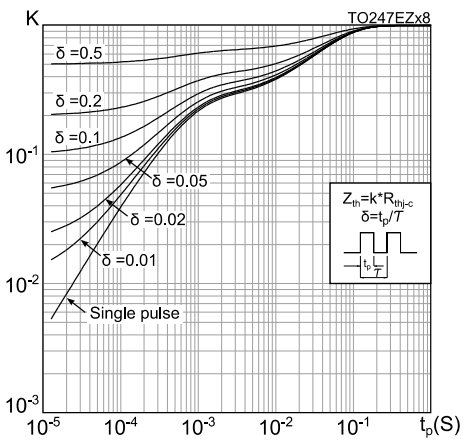



**Figure 4: Output characteristics**

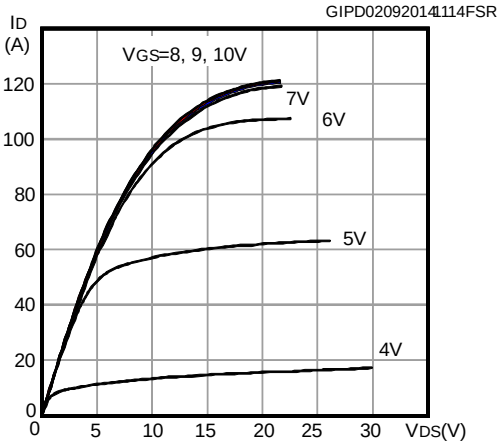



**Figure 5: Tranfer characteristics**

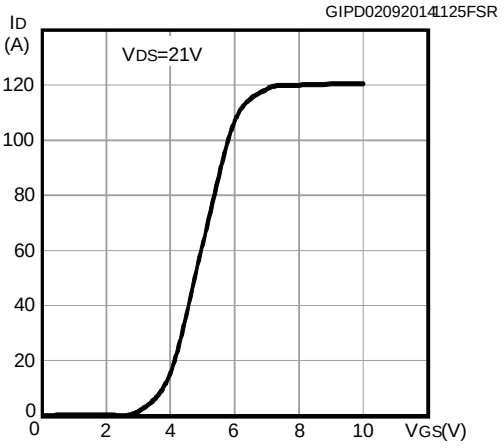



**Figure 6: Gate charge vs gate-source voltage**

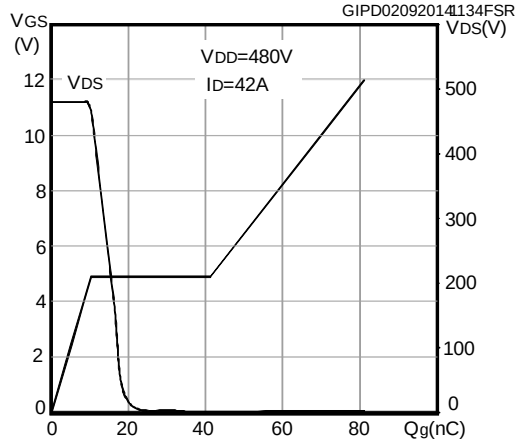



**Figure 7: Static drain-source on-resistance**

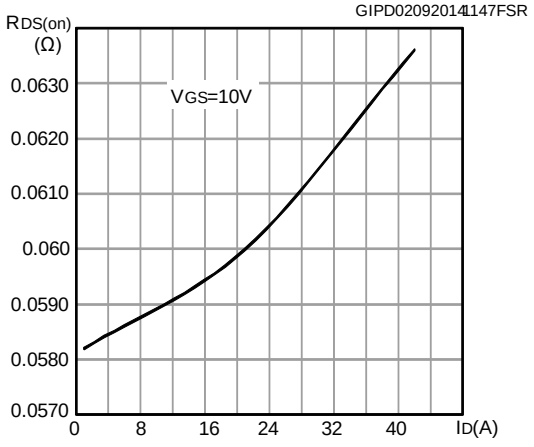


**Figure 8: Capacitance variations**

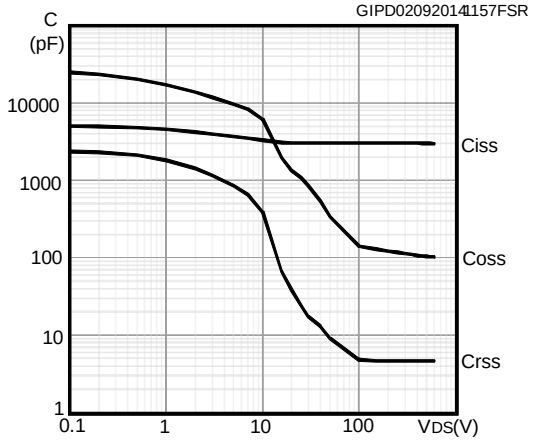



**Figure 9: Output capacitance stored energy**

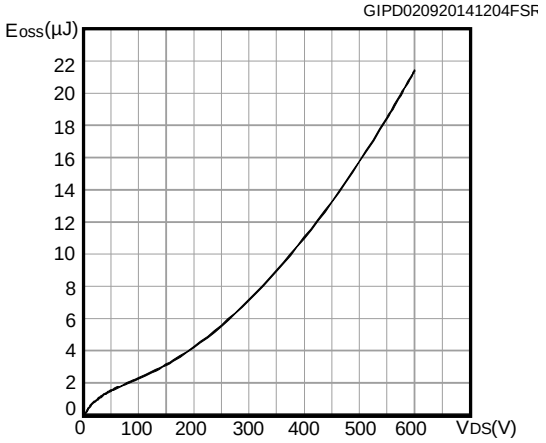



**Figure 10: Normalized gate threshold voltage vs temperature**

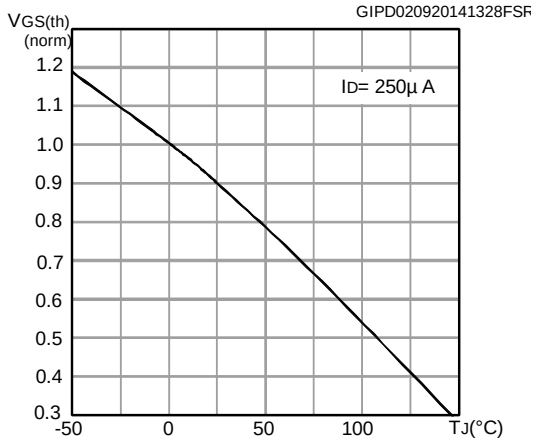



**Figure 11: Normalized on-resistance vs temperature**

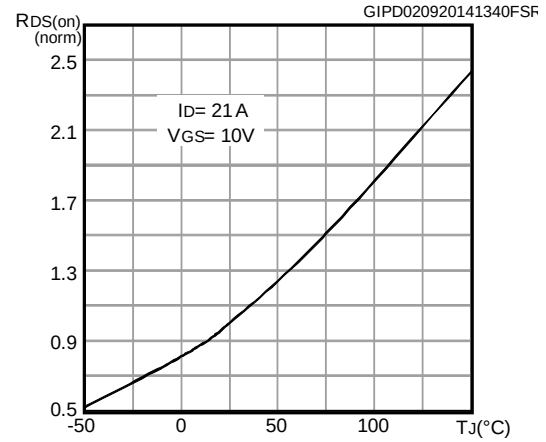



**Figure 12: Normalized V(BR)DSS vs temperature**

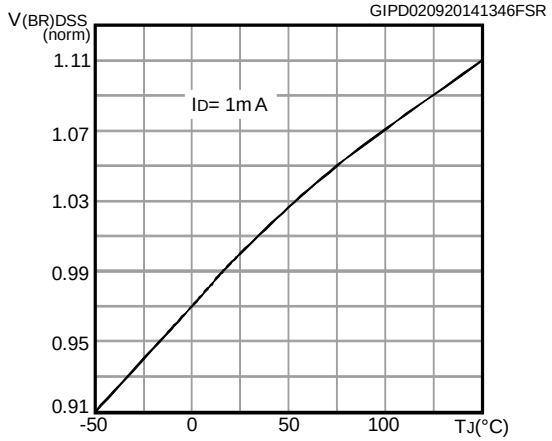
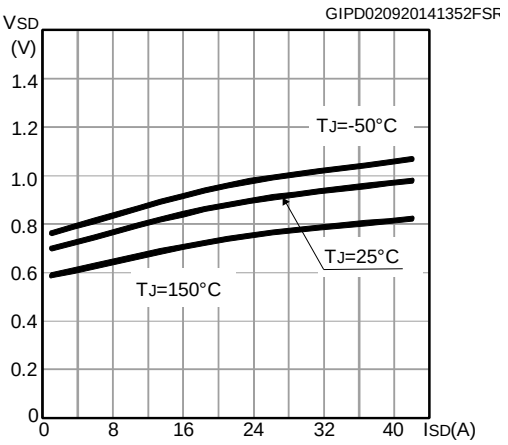



**Figure 13: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**

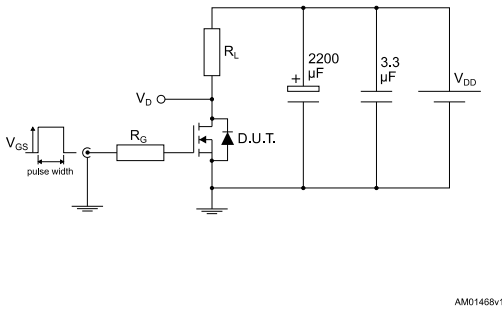



**Figure 15: Test circuit for gate charge behavior**

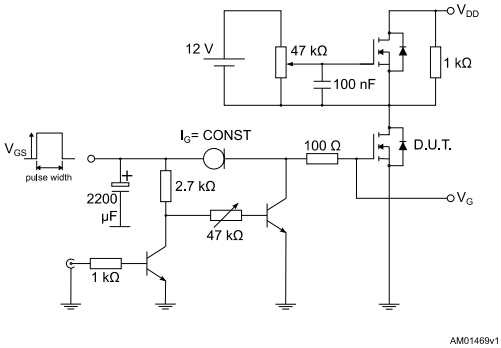



**Figure 16: Test circuit for inductive load switching and diode recovery times**

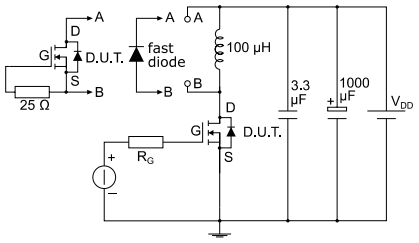



**Figure 17: Unclamped inductive load test circuit**

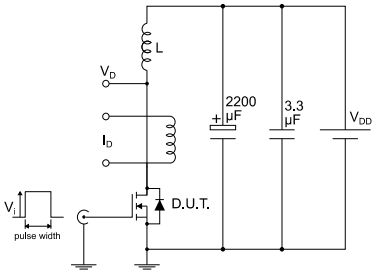



**Figure 18: Unclamped inductive waveform**

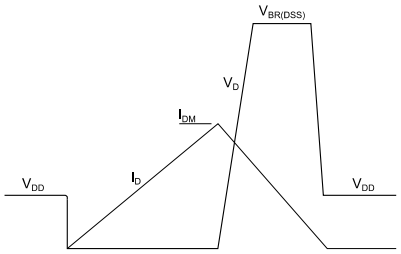
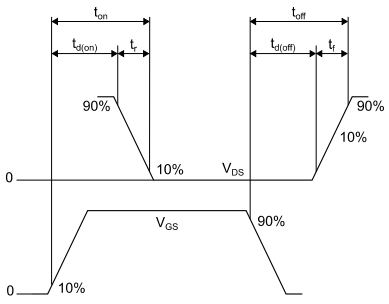



**Figure 19: Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 TO-247 long leads package information

**Figure 20: TO-247 long leads package outline**

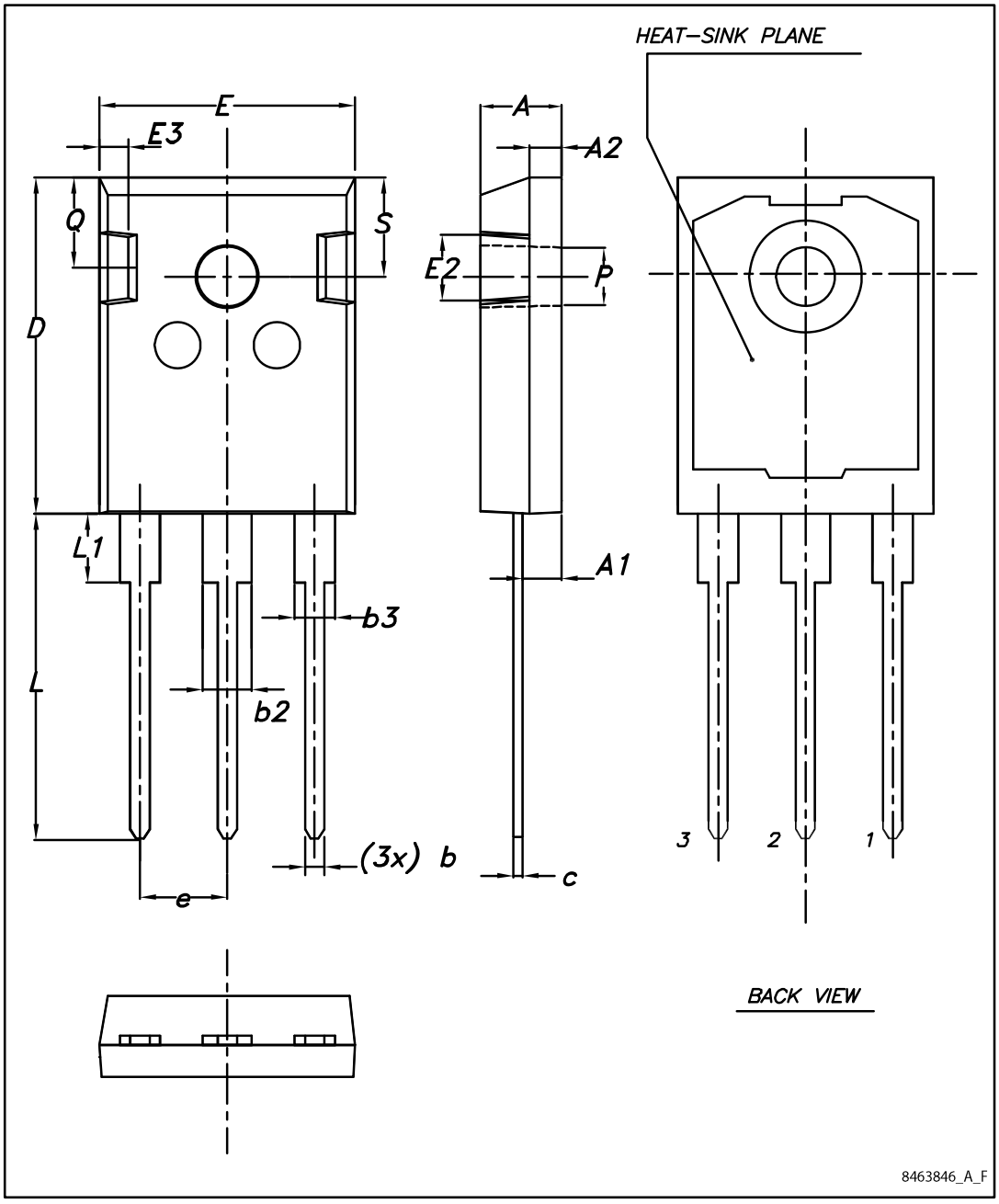


**Table 9: TO-247 long leads package mechanical data**

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.90 | 5.00 | 5.10 |
| A1 | 2.31 | 2.41 | 2.51 |
| A2 | 1.90 | 2.00 | 2.10 |
| b | 1.16 | | 1.26 |
| b2 | | | 3.25 |
| b3 | | | 2.25 |
| c | 0.59 | | 0.66 |
| D | 20.90 | 21.00 | 21.10 |
| E | 15.70 | 15.80 | 15.90 |
| E2 | 4.90 | 5.00 | 5.10 |
| E3 | 2.40 | 2.50 | 2.60 |
| e | 5.34 | 5.44 | 5.54 |
| L | 19.80 | 19.92 | 20.10 |
| L1 | | | 4.30 |
| P | 3.50 | 3.60 | 3.70 |
| Q | 5.60 | | 6.00 |
| S | 6.05 | 6.15 | 6.25 |

# 5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 01-Dec-2015 | 1 | First release. |

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