Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.85
Q_g (Max.) (nC)	63	
Q_{gs} (nC)	11	
Q_{gd} (nC)	30	
Configuration	Single	

TO-247AC

N-Channel MOSFET
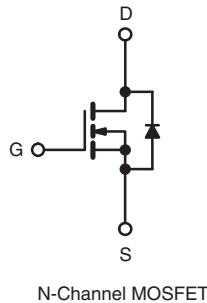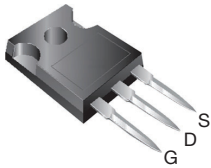
FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

Pb Available

RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP440PbF
	SiHFP440-E3
SnPb	IRFP440
	SiHFP440
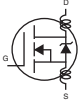
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	8.8	A
		T_C = 100 °C		5.6	
Pulsed Drain Current[a]			I_{DM}	35	
Linear Derating Factor				1.2	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	480	mJ
Repetitive Avalanche Current[a]			I_{AR}	8.8	A
Repetitive Avalanche Energy[a]			E_{AR}	15	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	150	W
Peak Diode Recovery dV/dt[c]			dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 11 mH, R_g = 25 Ω, I_{AS} = 8.8 A (see fig. 12).
c. I_{SD} ≤ 8.8 A, dI/dt ≤ 100 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.83	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.78	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 5.3 A[b]	-	-	0.85	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 5.3 A[b]		5.3	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V,		-	1300	-	pF
Output Capacitance	C_{oss}	V_{DS} = 25 V,		-	310	-	
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz, see fig. 5		-	120	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 8.0 A, V_{DS} = 400 V see fig. 6 and 13[b]	-	-	63	nC
Gate-Source Charge	Q_{gs}			-	-	11	
Gate-Drain Charge	Q_{gd}			-	-	30	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 8.0 A, R_g = 9.1 Ω, R_D = 31 Ω, see fig. 10[b]		-	14	-	ns
Rise Time	t_r			-	23	-	
Turn-Off Delay Time	$t_{d(off)}$			-	49	-	
Fall Time	t_f			-	20	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L_S			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8.8	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	35	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 8.8 A, V_{GS} = 0 V[b]		-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 8.0 A, dl/dt = 100 A/µs[b]		-	460	970	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.5	7.6	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
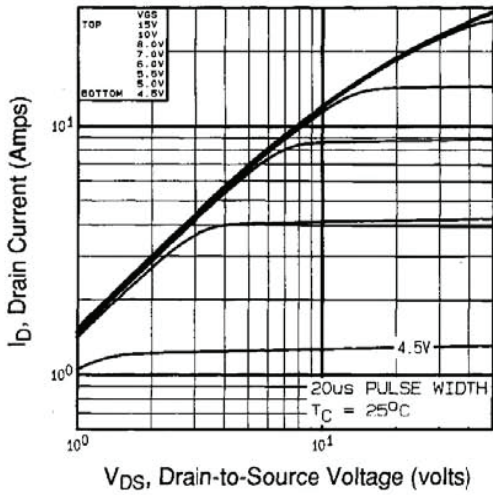
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
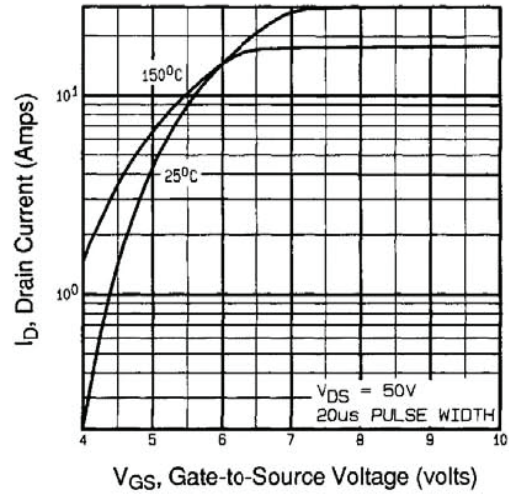

Fig. 1 - Typical Output Characteristics, T_C = 25 °C

Fig. 3 - Typical Transfer Characteristics

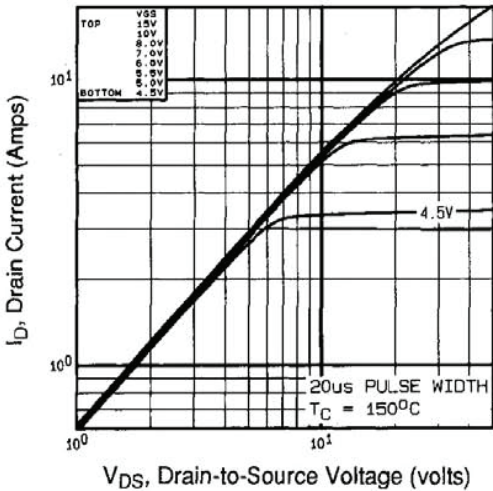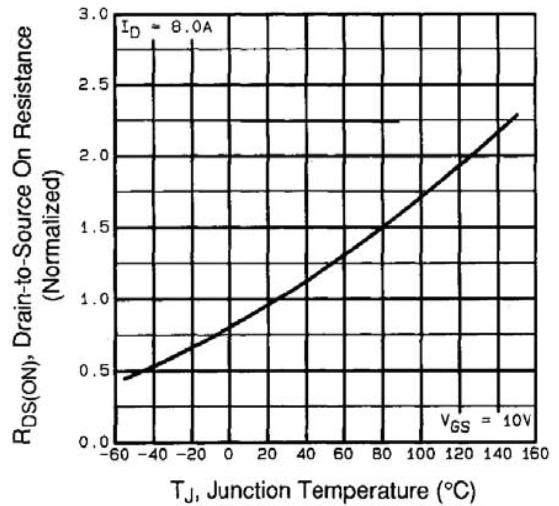Fig. 2 - Typical Output Characteristics, T_C = 150 °C

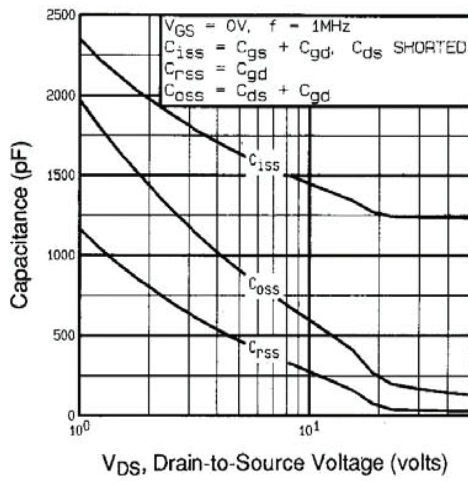Fig. 4 - Normalized On-Resistance vs. Temperature

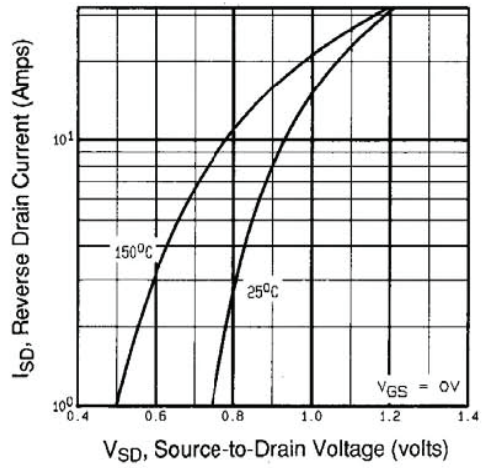**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

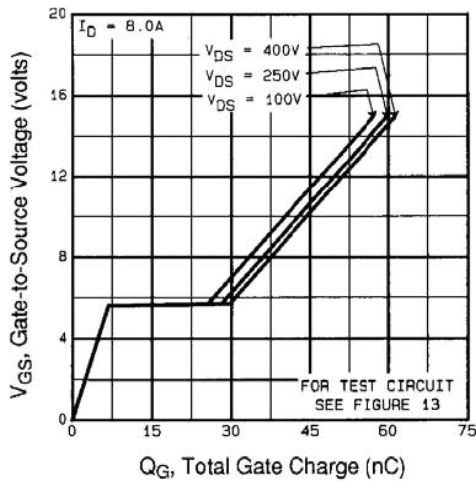**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

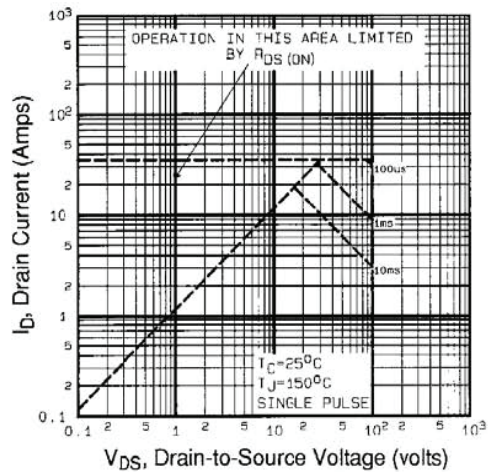**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

Fig. 8 - Maximum Safe Operating Area
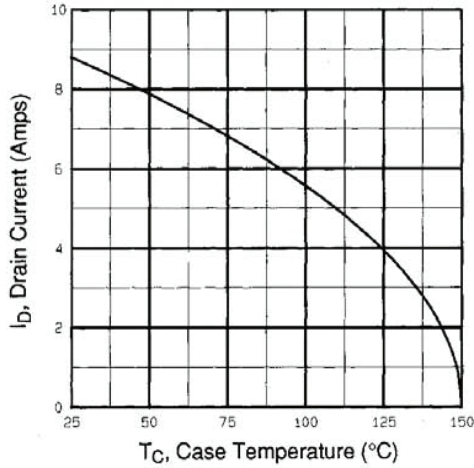
Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Pulse width ≤ 1 µs
Duty factor ≤ 0.1 %

Fig. 10b - Switching Time Waveforms

NOTES:
1. DUTY FACTOR, D=t1/t2
2. PEAK $T_j = P_{DM} \times Z_{thjc} + T_c$
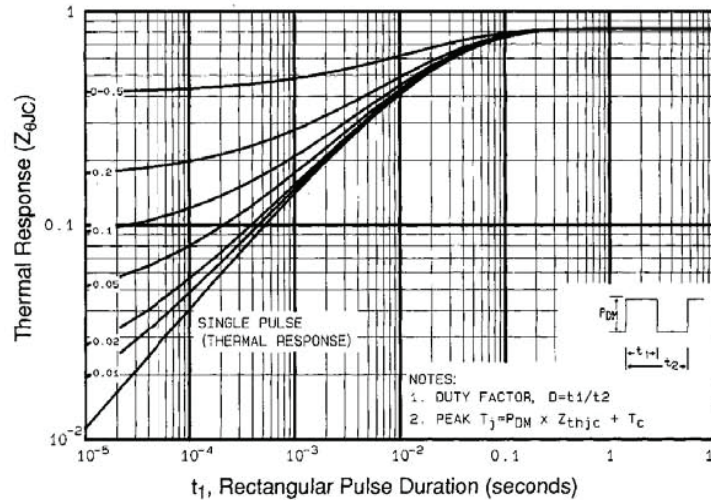
SINGLE PULSE
(THERMAL RESPONSE)

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case
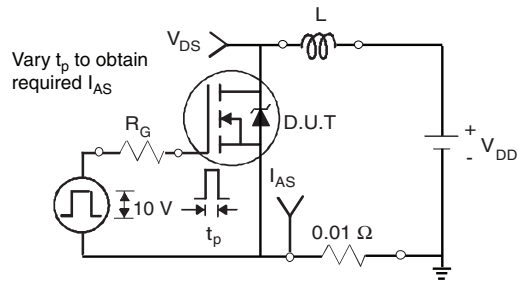
Fig. 12a - Unclamped Inductive Test Circuit
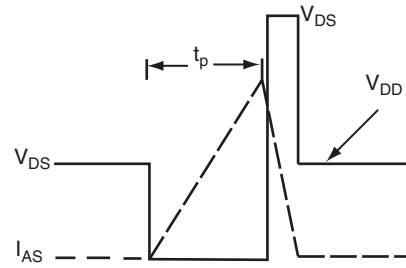

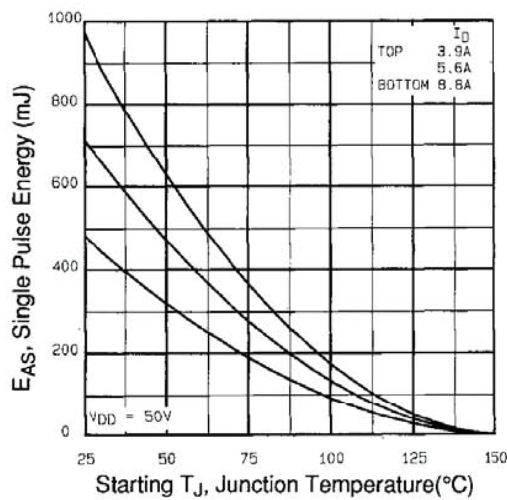**Fig. 12b - Unclamped Inductive Waveforms**

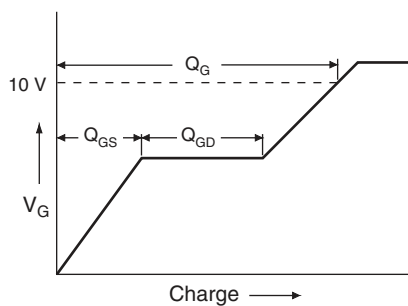**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

Fig. 13a - Basic Gate Charge Waveform
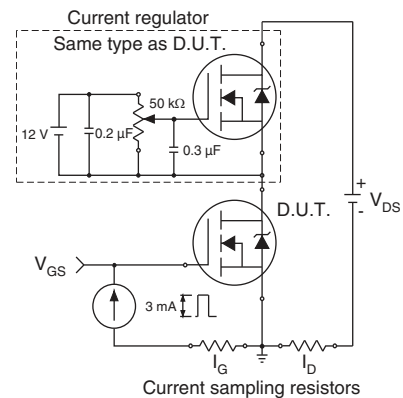
Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

D.U.T.

③

Circuit layout considerations
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

②

④

①

R_g

- dV/dt controlled by R_g
- Driver same type as D.U.T.
- I_{SD} controlled by duty factor "D"
- D.U.T. - device under test

V_{DD}

① Driver gate drive

P.W.

Period

$D = \dfrac{P.W.}{Period}$

$V_{GS} = 10$ V[a]

② D.U.T. I_{SD} waveform

Reverse recovery current

Body diode forward current

dI/dt

③ D.U.T. V_{DS} waveform

Diode recovery dV/dt

V_{DD}

Re-applied voltage

Body diode forward drop

④ Inductor current

Ripple ≤ 5 %

I_{SD}

Note

a. $V_{GS} = 5$ V for logic level devices

Fig.14 - For N-Channel

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TO-247AC (High Voltage)

Lead Assignments
1. Gate
2. Drain
3. Source
4. Drain

See view B

View A - A

Thermal pad

View B

Planting — (b1, b3, b5) — Base metal

Section C - C, D - D, E - E
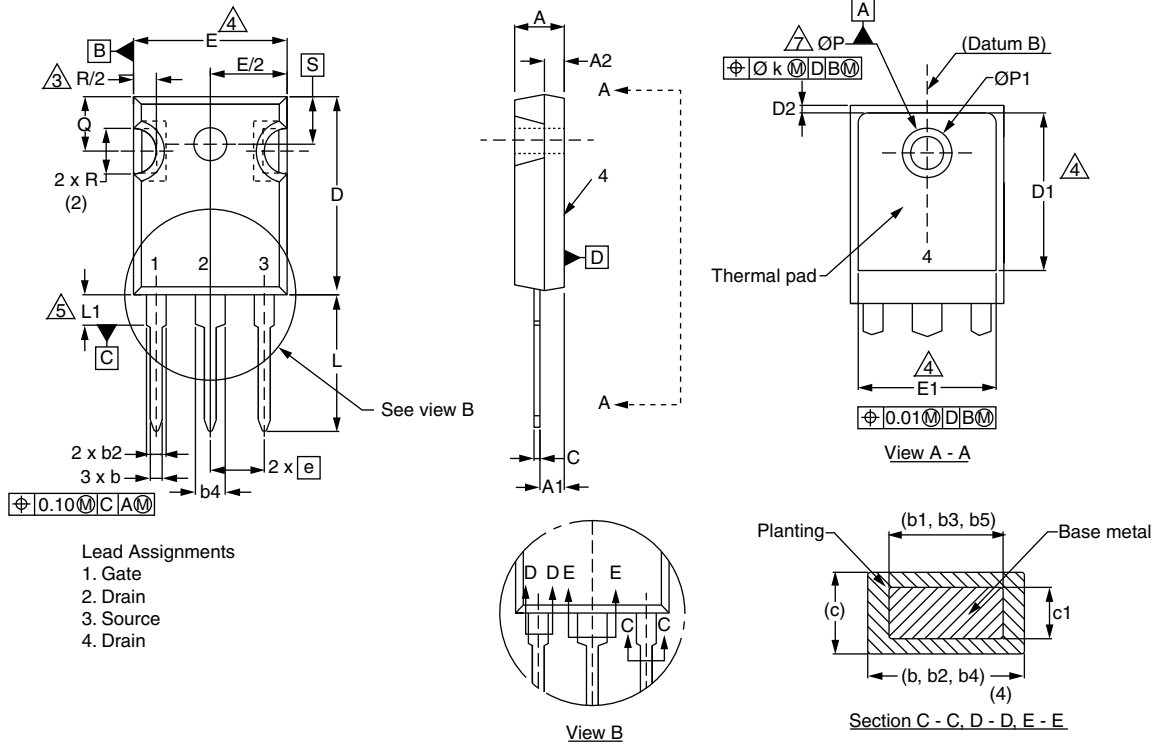
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0103-Rev. D, 01-Jul-13
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.

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